Memory Testing Introduction
Contents

• Memory Devices Introduction
• Memory Testing Methodology
• Memory ATE & Integration
• Memory Testing Challenges
• Q&A
Memory device type

- **Volatile** - the memory array loses its contents when power is removed - SRAM, DRAM

- **Non-Volatile** - It doesn’t lose data after power is turned off - ROM, EPROM, EEPROM, Flash
## Memory Summary

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>(p)SRAM</th>
<th>NOR</th>
<th>NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mainstream Density</strong></td>
<td>512M-1G</td>
<td>32-64M</td>
<td>128-512M</td>
<td>2-8G</td>
</tr>
<tr>
<td><strong>Cell</strong></td>
<td>T+C</td>
<td>4-6T</td>
<td>Floating Gate</td>
<td>Floating Gate</td>
</tr>
<tr>
<td><strong>Addr Interface</strong></td>
<td>Row, Column</td>
<td>Logic Addr</td>
<td>Logic Addr, A/D Multiplex</td>
<td>IOx bus</td>
</tr>
<tr>
<td><strong>IO Bits</strong></td>
<td>x8, x16</td>
<td>x16(U,L)</td>
<td>x16</td>
<td>x8, x16</td>
</tr>
<tr>
<td><strong>Control Bits</strong></td>
<td>CSn, RASn, CASn, WEn</td>
<td>CEn, WEn, OEn</td>
<td>CEn, WEn, OEn</td>
<td>CEn, WEn, REn, CLE, ALE</td>
</tr>
<tr>
<td><strong>Access Mode</strong></td>
<td>Burst</td>
<td>As, Burst</td>
<td>As, Burst</td>
<td>As</td>
</tr>
<tr>
<td><strong>Access Time</strong></td>
<td>xxx ps</td>
<td>xx ns</td>
<td>xx ns</td>
<td>xx us</td>
</tr>
<tr>
<td><strong>Partition</strong></td>
<td>Bank, Row, Col</td>
<td>Row, Col</td>
<td>Sect, Row, Col,(Partition)</td>
<td>Block, Page, Column</td>
</tr>
<tr>
<td><strong>Embedded Controller</strong></td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td><strong>Major Vendors</strong></td>
<td>S, H, M, Q, E</td>
<td>DH, IDM</td>
<td>S, I, ST</td>
<td>S, H, T, I, M, R</td>
</tr>
<tr>
<td><strong>Main Application</strong></td>
<td>PC</td>
<td>Cellular</td>
<td>iPod</td>
<td></td>
</tr>
</tbody>
</table>
Memory Testing

Memory Features

- Updateable
- Nonvolatile
- High Speed
- High Density

EPROM
EEPROM
ROM
FLASH
DRAM
SRAM

Source: Intel
Memory Testing Methodology
Characterization vs. Production Test

- **Characterization Test**
  - To identify the design and process window.
  - To finalize the datasheet specification.
  - Failure analysis and process debugging
  - Use many tools to get device characterization data, such as bitmap, shmoo, Specs search, thermal stress.
  - Test time is not a issue

- **Production Test**
  - Acceptance test or go/ no-go test
  - Wafer sort, final test, burn in test, speed test, reliability test.
  - Test time = Cost.
Basic Memory Test Items

• Continuity test – open/short
• DC parameter test
  – Input leakage test
  – Output leakage test
  – Output voltage test
  – Output short circuit test
  – Static/Dynamic Idd test
  – ODT (DDRII)
• AC Functional test
  – Timing test ( Taa, Toe, Tce, Trc, etc)
  – Memory pattern test ( March, Diagonal, Checkerboard, Galloping…)
  – Special test mode( stress, $V_{th}$, Icell, marginal test, data retention...)
• Redundancy & Repair test (optional)
Memory Backend Flow

CP 1
- Bake 24 hrs at 250c

CP 2

Data Retention

Laser Repair

CP 3
- DRAM Only

Assembly

FT 1/ 25 C
- Burn In

FT 2/ 85 C
- QC / 70c
- Mark & Pack
Purpose of Burn-In

High voltage, High temperature (125°C)  
– to screen out infant mortalities
Access (R/W) Memory core 1/2
Access (R/W) Memory core 2/2

<table>
<thead>
<tr>
<th>X=0</th>
<th>Y=0</th>
<th>Y=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
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</table>

<table>
<thead>
<tr>
<th>X=1</th>
<th>Y=0</th>
<th>Y=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X=Xmax</th>
<th>Y=Ymax</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 1</td>
<td></td>
</tr>
<tr>
<td>1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>0 1 0 1</td>
<td></td>
</tr>
<tr>
<td>1 0 1 0</td>
<td></td>
</tr>
</tbody>
</table>
### Memory core v.s. Multiple Table 1/2

<table>
<thead>
<tr>
<th>1x1 = 1</th>
<th>2x1 = 2</th>
<th>3x1 = 1</th>
<th>4x1 = 4</th>
<th>8x1 = 8</th>
<th>9x1 = 9</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x2 = 2</td>
<td>2x2 = 4</td>
<td>3x2 = 2</td>
<td>4x2 = 8</td>
<td>8x2 = 16</td>
<td>9x2 = 18</td>
</tr>
<tr>
<td>1x3 = 3</td>
<td>2x3 = 6</td>
<td>3x3 = 3</td>
<td>4x3 = 12</td>
<td>8x3 = 24</td>
<td>9x3 = 27</td>
</tr>
<tr>
<td>1x4 = 4</td>
<td>2x4 = 8</td>
<td>3x4 = 12</td>
<td>4x4 = 16</td>
<td>8x4 = 32</td>
<td>9x4 = 36</td>
</tr>
<tr>
<td>1x5 = 5</td>
<td>2x5 = 10</td>
<td>3x5 = 15</td>
<td>4x5 = 20</td>
<td>8x5 = 40</td>
<td>9x5 = 45</td>
</tr>
<tr>
<td>1x6 = 6</td>
<td>2x6 = 12</td>
<td>3x6 = 18</td>
<td>4x6 = 24</td>
<td>8x6 = 48</td>
<td>9x6 = 54</td>
</tr>
<tr>
<td>1x7 = 7</td>
<td>2x7 = 14</td>
<td>3x7 = 21</td>
<td>4x7 = 28</td>
<td>8x7 = 56</td>
<td>9x7 = 63</td>
</tr>
<tr>
<td>1x8 = 8</td>
<td>2x8 = 16</td>
<td>3x8 = 24</td>
<td>4x8 = 32</td>
<td>8x8 = 64</td>
<td>9x8 = 72</td>
</tr>
<tr>
<td>1x9 = 9</td>
<td>2x9 = 18</td>
<td>3x9 = 27</td>
<td>4x9 = 36</td>
<td>8x9 = 72</td>
<td>9x9 = 81</td>
</tr>
</tbody>
</table>
Memory core vs. Multiple Table 2/2

for (i=1 ; i<10; i++)
    for(j=1; j<10; j++)
        printf("%d x %d = %d\n", i, j, ixj);

We can use for loop and different variables and set boundary condition in C language, but how to implement similar function in memory tester pattern?

C language

Memory ATE
Memory ATE v.s. Logic ATE

1/2

cycle1, y= 0; x=0;
cycle2, ymax=0x3ff; xmax=0xffffffff;
cycle3, c=(ymax+1)*(xmax+1)-1

cycle4, d=expect_data, Data nc;

loop:

cycle5, y++,x++(ymax), Address nr, Data cn, jump( !c.tc) loop, c--;

cycle6, Data nc;

Less than 10 Vectors length
### Memory ATE v.s. Logic ATE

<table>
<thead>
<tr>
<th>cycle</th>
<th>address</th>
<th>data</th>
<th>control</th>
</tr>
</thead>
<tbody>
<tr>
<td>cycle1</td>
<td>0..000000000000000000hhlhlhlhxxxx;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cycle2</td>
<td>0..000000000000000001hhlhlhlhxxxx;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cycle3</td>
<td>0..0000000000000000010hhlhlhlhxxxx;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cycle4</td>
<td>0..0000000000000000011hhlhlhlhxxxx;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cycle0x3fffff</td>
<td>1..111111111111111110hhlhlhlhxxxx;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cycle0x4000000</td>
<td>1..111111111111111111hlhlhlhlxxxx;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

64M Vectors length
Memory ATE & Integration
Requirement for memory ATE

**RAM Tester**: DRAM, SRAM
- pattern generator capability: APG, BM, ECR,...
- data width: 32/64 or more, interleave, burst, refresh function,...
- high speed
- powerful redundancy analysis repair

**NVM Tester**: Flash, Mask ROM, EEPROM,...
- pattern generator capability: APG, BM, ECR,...
- high voltage – Vcc, Vpp
- high density buffer memory for mask ROM
- powerful redundancy analysis repair
- Tester-Per-Site™

**High Speed Tester**: XDR, GDDR, DDRIII
- High speed (>2G bps)
- EPA <100 ps
- Small jitter, Wide data Eye
Conventional Test Architectures

Tester-Per-Site™ Architecture

Shared-Resource Architecture
Throughput Comparison

Test Time, Shared-Resource Architecture

Test Time, Tester-Per-Site™ Architecture
ATE Main Frame Block Diagram

- Tester Processor
- Tester Control Bus Interface
- Timing Generator
- APG
- Data Selector
- Format Control
- Pin Electronics
- Manual
- DUT
- DC parametric measuring unit
- VI
- Device Power Supply
- VO

High-speed test vector transfer bus
High-speed tester control bus
Tester-Per-Site™ Parallel Test Architecture
Memory ATE (APG Resource)

D Register

BM

X/Y/Z Register

Scramble

ACAM

ECR0 - ECR15

DUT

PE0 - PE31

dl(0) - dl(15)

BM(0) - BM(15)

a(0) - a(31)
Engineering to High-Volume Manufacturing

Engineering tester
- Powerful / Flexible
- Good debugging tools
- Convenient
- Easy migrating to production

High-volume manufacturing tester
- Higher through-put
- Lower cost-of-test
- Easy maintain
Interface/Interconnect technology

Eng. Matrix – 768 pins
MCP, NOR, NAND development

300mm Wafer Probing
2 TD skip row, 1 TD full wafer

DSI
128 NOR, 320 NAND

Engineering
4 sites – 128 pins

Wafer Sort
144 sites – 4608 pins

Matrix – 24,576 pins
384 MCP, 384 NOR, >512 NAND

Final Test
128 sites – 4096 pins

VERIGY
Test Cell Environment

- Tester
- Test head
- Prober(CP) / Handler(FT)
- Load board
- Probe card
- Test program
- Server/CIM system

Test result (Wafer Map)

Server/Network

Engineer/Operator

Probe Card

Tester

Prober(CP)

Handler(FT)

Load Board
Economical Test Solution for Memory

Wafer Sort Configuration

Final Test Configuration
WS 1TD Probe Card solution

WS interface for full 300mm probing

144 Test Sites ensure the fastest test times @ up to 288 devices in parallel

WS 300mm probecard
1 Touchdown @ 100% efficiency
WS Interface

2304 I/O Channels
Vacuum Compression
(Pogos)

4608 I/O Channels
Mechanical Compression
(XZIF)
V5400 vs. V4400
V4400 probe card is 355mm
V5400 probe card is 440mm
24% more probe card area
Double the I/O density
75% more keep out area

V5400 vs. V4400
V4400 pad density is 70mm
V5400 pad density is 40mm
V5400 keep out area is 10” or 250mm
FT Interface: HiFix
HiFix Components

- DPS wiring board for 8 DPS channels
  - 8 boards in total
- Up to 16 HSM sites
- Cable assemblies (signal and DPS lines)
- Trigger and reference connectors for calibration robot
Memory Test Challenges

• High Speed

• Mix of parts is increasing
  - Flash, DRAM, SRAM

• Increase Parallelism

• Debug tools

• High throughput
• Flexible configuration
• Reduced system cost
High-Speed Memory Device Roadmap

Verigy’s Extrapolation

Source: SEC, Japan Rambus Symposium, June 04, Timing shows QS / MP

- DDR I/O speed is limited by “Physics”
- Expect New Memory Technology

Bandwidth demand drive speed of High-Speed DRAMs

nm Process technology is used to address speed & density (cost)
DDR III Memory
High Speed Solution: Per-Pin Processor

Memory ATE on a Single Chip (Test-Processor Per-Pin)

HSM3600 Sub-Module (4 Channels)

HSM3600 Card (32 Channels) Water Cooled

→ TRUE “Memory ATE Per-Pin” enabled by the Test-Processor Technology
High Speed Solution: HW Free APG

Front-end (Pin Electronics)

- **Pin 1**
  - DUAL LEVEL COMPARATOR
  - 50 Ω ACTIVE LOAD
  - PPMU P/F
  - To HPPMU 1 per cage
  - Value Measurement

- **Pin 3**
  - DUAL LEVEL COMPARATOR
  - 50 Ω ACTIVE LOAD
  - PPMU P/F
  - To HPPMU 1 per cage

- **Board ADC**
- **16 ch MUX**
- **1 per 16 ch (2 on 1 board)**

- **Memory**
  - Test Processor
  - **Drive**
  - **Receive**
  - **Control**

- **Test Processor**
  - **Drive**
  - **Receive**
  - **Control**

- **Memory**

**Pin 1**

- **Drive**
- **Receive**
- **Control**

**Pin 3**

- **Drive**
- **Receive**
- **Control**

**Board ADC**

**16 ch MUX**

**1 per 16 ch (2 on 1 board)**

**Third Level**

- **VIH DRIVER**
- **VIL IOL**
- **Vcom**
- **VOL**
- **DUAL LEVEL COMPARATOR**
- **DIFFERENTIAL RECEIVER**
- **PPMU P/F**
- **To HPPMU 1 per cage**
- **Value Measurement**
## High Speed Solution: Per-Pin Complier

<table>
<thead>
<tr>
<th>Address Word</th>
<th>a2</th>
<th>a1</th>
<th>a0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Repeating Patterns on a Pin

- **pin a2**: repeat 4 "0" repeat 4 "1"
- **pin a1**: repeat 2 "0011"
- **pin a0**: repeat 4 "01"
Memory Test Challenges

• High Speed

• Mix of parts is increasing
  - Flash, DRAM, SRAM

• Increase Parallelism

• Debug tools

- High throughput
- Flexible configuration
- Reduced system cost
Multi Chip Package (MCP)
100% of modern cell phones use MCPs

A streaming video phone with 0.3MP Camera

Source: iSuppli Corp.
Dynamic Interface: Matrix

1) Dynamic Interface design to access different Memory parts

2) Dynamic APG minimizes test time and allows for concurrent testing

Switch Pins to Test NOR/SRAM
Memory Test Challenges

- High Speed
- Mix of parts is increasing
  - Flash, DRAM, SRAM
- Increase Parallelism
- Debug tools

- High throughput
- Flexible configuration
- Reduced system cost
Increase Parallelism: PE Share

**Standard Pin Channel**
- Good Signal Quality (Yield)
- Low Parallelism (Throughput)
- High Cost

**Wire-OR Channel**
- High Parallelism (Throughput)
- Lowest Cost
- Degraded Signal Quality (Yield)
- Device Interaction (Yield)
- Serial Reads (Throughput)

**Active Fan-out Channel**
- Better Signal Quality (Yield)
- High Parallelism (Throughput)
- Better Cost
- Serial Reads (Throughput)

**Active Fan-out with Compare Channel**
- Better Signal Quality (Yield)
- High Parallelism (Throughput)
- Better Cost
- Parallel Reads (Throughput)
2. OpenShots()

In this exercise, we will work with a parametric test function. OpenShots has been pre-coded. Don't forget to uncomment this function in DoTestProgram(). To test open pins, we want to force 
-2 V and clamp the current at 100 μA (PMV) and fail all pins where the measured PMU current is 
greater (less negative) than -60 μA. The theory is, if the PMU attempts to drive a -2 V on a DUT 
pin, it forward-biases an internal protection diode, which turns on and conducts current at the 
negative PMU current limit of -100 μA. In this case, the PMU current clamp holds the PMU 
equilibrium output voltage at -600 mV, not -2 V. If the pin is open, PMU current is 0 μA, and 
voltage is -2 V.

To test short pins, we want to force -2 V and clamp the current at 100 μA (PMV) and fail all pins 
where the measured PMU voltage is greater (less negative) than -300 mV. The theory is, if the 
pin is shorted to another pin, we should measure 0 V on the pin because it is shorted to pins that 
are driven to 0 V (the device has been pre-conditioned to drive 0 V on all pins in the pre-coded 
part of the function OpenShots()).
For a driver sharing application (by-N sharing) the timing reference is the socket of site 1

- for the shared pins the fixture delay values compensate the delay to site 1 only
  - for site 1 there is no change compared to a non-shared application
Memory Test Challenges

• High Speed

• Mix of parts is increasing
  - Flash, DRAM, SRAM

• Increase Parallelism

• Debug tools

• High throughput
• Flexible configuration
• Reduced system cost
**Timing Diagram**

IO turn-around time
(Here: ~12ns @ 1Gbps data rate)
Scope view

'Oscilloscope' integrated into test system
BitMap Viewer

- True Topological View
- Overlay – Different layers represented by colors
- Zoom IN/OUT
- Detail View with Logical / Topological / Physical ADR

• State-of-the-art and easy to use!
PATTERN Tool

- Entry Point
- Vector Offset
- Navigates to Vector Address
- Step APG to break points given vector
- HW contents at current vector
- APG stop at current vector
- Register Values for current Pattern
- Failed Entry Point
- Failed Failing Pins
- Failed vector
- Failed pin

VERIGY
Q & A

• Thank you !!