VLSI Design

Chapter 4

Circuit Characterization and Performance Estimation

Jin-Fu Li
Chapter 4 Circuit Characterization and Performance Estimation

- Resistance & Capacitance Estimation
- Switching Characteristics
- Transistor Sizing
- Power Analysis
- Other Issues
Resistance Estimation

• Resistance
  – \( R = (\rho / t)(L/W) \), where \((\rho, t, L, W)\) is \((\text{resistivity, thickness, conductor length, conductor width})\)
  – Sheet resistance \( R_s = \Omega/ \square \)
  – \( R = R_s (L/W) \)

1 rectangular block
  \( R = R_s (L/W) \)

4 rectangular block
  \( R = R_s (2L/2W) = R_s (L/W) \)
Resistor – None rectangular

- Rectangle: $R = \frac{L}{W}$
- Parallelogram: $R = \frac{L}{W}$
- Trapezoid 1: $R = \frac{4L}{L + 4W_1}$
- Trapezoid 2: $R = \frac{2L}{L + 2W_1}$
Resistor – None rectangular (2)

Ratio = \frac{L}{W}

Ratio = \frac{W_1}{W_2}

Ratio = \frac{W_1}{W_2}

Ratio = \frac{W_2}{W_1}

Ratio = \frac{W_2}{W_1}
Capacitor

- Load capacitance on the output of a CMOS gate is the sum of
  - Gate capacitance
  - Diffusion capacitance
  - Routing capacitance

- Capacitance can be calculated by
  \[ C = \frac{\varepsilon_0 \varepsilon_x}{d} A \]
  - \( \varepsilon_x \): dielectric constant
  - \( \varepsilon_0 \): permitivity of free space
Gate Capacitor (1)

Accumulation

\[ V_g < 0 \]

Depletion

\[ V_g > 0 \]
Gate Capacitor (2)

**Inversion**

\[ V_g > 0 \]

**Capacitance variation**

\[ \frac{C}{C_0} \]

Accumulation  Depletion  Inversion

Low freq.  High freq.

\[ V_{gs} \]

\[ 0 \rightarrow V_t \]
Gate Capacitor (3)

\[
C_g = C_{gb} + C_{gs} + C_{gd}
\]
# Gate Capacitor (4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Off</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gb}$</td>
<td>$\frac{\varepsilon A}{t_{ox}}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>0</td>
<td>$\frac{\varepsilon A}{2t_{ox}}$</td>
<td>$\frac{2\varepsilon A}{3t_{ox}}$</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>0</td>
<td>$\frac{\varepsilon A}{2t_{ox}}$</td>
<td>0</td>
</tr>
</tbody>
</table>

$C_g = C_{gb} + C_{gs} + C_{gd}$

- $\frac{\varepsilon A}{t_{ox}}$
- $\frac{\varepsilon A}{t_{ox}}$
- $\frac{2\varepsilon A}{3t_{ox}}$
**Diffusion Capacitor**

\[ C_d = C_{ja} \times (ab) + C_{jp} \times (2a + 2b) \]

- \( C_{ja} \) = junction capacitance per micron square
- \( C_{jp} \) = periphery capacitance per micron
Wire Capacitor (1)

Fringing fields

Multi-layer conductor

C_{21} + C_{23} + C_{22} = C_2

Layer 1

Layer 2

Layer 3

substrate

Insulator (Oxide)

W

L

T

H
Wire Capacitor (2)
**Inductor**

- For bond wire inductance
  \[ L = \frac{\mu}{2\pi} \ln \left(\frac{4h}{d}\right) \]

- For on-chip metal wires
  \[ L = \frac{\mu}{2\pi} \ln \left(\frac{8h + w}{w} + \frac{w}{4h}\right) \]

- The inductance produces \( L\frac{di}{dt} \) noise especially for ground bouncing noise. Note that when CMOS circuit are clocked, the current flow changes greatly.

\[ V = L \frac{di}{dt} \]
Wire RC Effects (1)

\[ C \frac{dV_j}{dt} = (I_{j-1} - I_j) = \frac{(V_{j-1} - V_j)}{R} - \frac{(V_j - V_{j+1})}{R} \]

\[ r_c \frac{dV}{dt} = \frac{d^2V}{dx^2} \Rightarrow t_x = kx^2 \]

- \( r \) : resistance per unit length
- \( c \) : capacitance per unit length
Wire RC Effects (2)

Assume that \( t_x = 4 \times 10^{-15} x^2 \)

With buffer
\[
\begin{align*}
    t_p &= 4 \times 10^{-15} \times 1000^2 + t_{buf} + 4 \times 10^{-15} \times 1000^2 \\
    &= 4ns + t_{buf} + 4ns = 8ns + t_{buf}
\end{align*}
\]

Without buffer
\[
    t_p = 4 \times 10^{-15} \times 2000^2 = 16ns
\]
Delay Analysis (1)

\[ V_{\text{in}}(t) \rightarrow V_{\text{out}}(t) \]

\[ V_{\text{DD}} \]

\[ I_{\text{ds}} = V_{\text{gs}} - V_{t} \]

Time intervals:
- \( t_{pf} \)
- \( t_{dr} \)
- \( t_{f} \)
- \( t_{r} \)

Percentage points:
- 90%
- 50%
- 10%
Delay Analysis (2)

- **Saturated** $V_{out} \geq V_{DD} - V_{tn}$
- **Nonsaturated** $0 < V_{out} \leq V_{DD} - V_{tn}$

- **Saturated** $V_{out} \leq |V_{tp}|$
- **Nonsaturated** $|V_{tp}| < V_{out} < V_{DD}$

- $I_{dsn}$: N-device
- $I_{dsp}$: P-device
- $V_{out}(t)$
- $C_L$
- $R_{cn}$
- $R_{cp}$
Delay Analysis (3)

• The fall time consists of two intervals:
  - $t_{f1} =$ period during which the capacitor voltage, $V_{out}$, drops from $0.9V_{DD}$ to $(V_{DD}-V_{tn})$
  - $t_{f2} =$ period during which the capacitor voltage, $V_{out}$, drops from $(V_{DD}-V_{tn})$ to $0.1V_{DD}$

\[
C_L \frac{dV_{out}}{dt} + \frac{\beta_n}{2} (V_{DD} - V_{tn})^2 = 0 \quad \text{(In saturation)}
\]

\[
t_f \approx k \times \frac{C_L}{\beta_n V_{DD}} \quad t_r \approx k \times \frac{C_L}{\beta_p V_{DD}}
\]

\[
t_p \approx k \times \frac{C_L}{V_{DD}} \left( \frac{1}{\beta_n} + \frac{1}{\beta_p} \right)
\]
Design Challenges

- **Reduce $C_L$**
  - Careful layout can help to reduce the diffusion and interconnect capacitance

- **Increase $\beta_n$ and $\beta_p$**
  - Increase the transistor sizes also increases the diffusion capacitance as well as the gate capacitance. The latter will increase the fan-out factor of the driving gate and adversely affect its speed.

- **Increase $V_{DD}$**
  - The designer does not have too much control over this factor, as the supply voltage is determined by system and technology considerations.
Gate Delays

\[
\beta_{neff} = \frac{1}{(1/\beta_{n1}) + (1/\beta_{n2}) + (1/\beta_{n3})}
\]

\[
\beta_{n1} = \beta_{n2} = \beta_{n3} \implies \beta_{neff} = \frac{\beta_n}{3}
\]
Delay Analysis – Switch Level RC Model

![Diagram of a switch-level RC model with nodes and capacitors labeled.]
Switch Level RC Model

• Simple RC model

\[ t_{df} = \sum R_{\text{pulldown}} \times \sum C_{\text{pulldown-path}} \]

\[ = (R_{N1} + R_{N2} + R_{N3} + R_{N4}) \times (C_{\text{out}} + C_{ab} + C_{bc} + C_{cd}) \]

\[ t_{dr} = R_{p4} \times C_{\text{out}} \]

• Elmore delay model

\[ t_d = \sum R_i C_i \]

\[ t_{df} = (R_{N1} \times C_{cd}) + [(R_{N1} + R_{N2}) \times C_{bc}] + [(R_{N1} + R_{N2} + R_{N3}) \times C_{ab}] \]

\[ \quad + [(R_{N1} + R_{N2} + R_{N3} + R_{N4}) \times C_{\text{out}}] \]
Transistor Sizing

\[ t_{\text{inv-pair}} = t_{\text{fall}} + t_{\text{rise}} = R3C_{eq} + 2 \frac{R}{2} 3C_{eq} \]

\[ = 3RC_{eq} + 3RC_{eq} \]

\[ = 6RC_{eq} \]

\( C_{eq} \) is the capacitance of a unit (2/1) NMOS transistor

\( R \) is the equivalent channel resistance of a unit NMOS transistor
Transistor Sizing

\[ t_{\text{inv-pair}} = t_{\text{fall}} + t_{\text{rise}} = R2C_{\text{eq}} + 2R2C_{\text{eq}} = 6RC_{\text{eq}} \]
Transistor Sizing

\[ t_{\text{inv-pair}} = t_{\text{rise}} + t_{\text{fall}} = 6R(C_g + 2C_d) + R(C_g + C_d) \]

\[ = 7RC_{eq} \]

\[ C_{eq} = C_g + 2C_d \]
Transistor Sizing

minimum sized gate delay $t_d$

one stage delay $a t_d$

N stage delay $n a t_d = \ln(R) \frac{a}{\ln(a)} t_d$

Stage ratio -- $a$

Graph showing the relationship between stage ratio $a$ and $a/\ln(a)$. The equation for the curve is not provided in the text.
Power Dissipation

Instantaneous power:

\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:

\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:

\[
P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t)dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t)dt
\]
Power Analysis

• Power consumption of a CMOS circuit
  – *Static power* caused by the leakage current and other static current
  – *Dynamic power* caused by the total output capacitance
  – Dynamic power caused by the *short-circuit* current

• Total power consumption of a CMOS circuit is given by
  \[ P_t = P_s + P_d + P_{sc} \]
Power Analysis – Static Power

PN junction reverse bias leakage current

\[ i_0 = i_s (e^{qV_{in}/KT} - 1) \]

\[ P_s = \sum_{1}^{n} I_{leakage} \times V_{supply} \]
Power Analysis – *Dynamic Power*

- Let the inverter is operated at a switching frequency $f=1/T$

\[
P_d = \frac{1}{T} \int_0^T i_o(t)v_o(t)dt
\]

\[
i_p = i_o = C_L \frac{dv_o}{dt}
\]

\[
i_n = -i_o = -C_L \frac{dv_o}{dt}
\]

\[
P_d = \frac{1}{T} \left[ \int_0^{V_{DD}} C_Lv_o dv_o - \int_{V_{DD}}^0 C_Lv_o dv_o \right]
\]

\[
P_d = \frac{C_LV_{DD}^2}{T} = fC_LV_{DD}^2
\]
Energy vs. Power

• Energy consumption of an inverter (from $0 \rightarrow V_{DD}$)
  - The energy drawn from the power supply is
    * $E = QV = C_L V_{DD}^2$
  - The energy stored in the load capacitance is
    * $E_{cap} = \int_0^{V_{DD}} C_{V_o} dV_o = \frac{1}{2} C_L V_{DD}^2$
  - The output from $V_{DD} \rightarrow 0$
    * The $E_{cap}$ is consumed by the pull-down NMOS

• Low-energy design is more important than low-power design
Power Analysis – Short-Circuit Power

\[ P_{sc} = I_{mean} V_{DD} \]

\[ I_{mean} = 2 \times \frac{1}{T} \left[ \int_{t_1}^{t_2} i(t) dt + \int_{t_2}^{t_3} i(t) dt \right] \]

\[ I_{mean} = \frac{4}{T} \left[ \int_{t_1}^{t_2} i(t) dt \right] \]
Power Analysis – *Short-Circuit Power*

\[
I_{\text{mean}} = \frac{4}{T} \left[ \int_{t_1}^{t_2} \frac{\beta}{2} (V_{\text{in}}(t) - V_T)^2 \, dt \right]
\]

\[
V_{\text{in}}(t) = \frac{V_{DD}}{t_r} t
\]

\[
t_1 = \frac{V_T}{V_{DD}} t_r
\]

\[
t_2 = \frac{t_r}{2}
\]

\[
P_{sc} = \frac{\beta}{12} (V_{DD} - 2V_T)^3 \tau f, \text{ where } \tau = t_r = t_f
\]
Power Analysis – Switching Activity

- The dynamic power for a complex gate cannot be estimated by the simple expression $C_L V_{DD} f$

- Dynamic power dissipation in a complex gate
  - Internal cell power
  - Capacitive load power

- Capacitive load power
  - $P_L = \alpha C_L V_{DD}^2 f$

- Internal cell power
  - $P_{\text{int}} = \sum_{i=1}^{n} \alpha_i C_i V_i V_{DD} f$
Power Analysis – Glitching power

• In a static logic gate, the output or internal nodes can switch before the correct logic value is being stable. This phenomenon results in spurious transitions called glitches.
Rules for avoiding Glitching power

- Balance delay paths; particularly on highly loaded nodes
- Insert, if possible, buffers to equalize the fast path
- Avoid if possible the cascaded implementation
- Redesign the logic when the power due to the glitches is an important component
Principles for Power Reduction

• Prime choice: *reduce voltage*
  – Recent years have seen an acceleration in supply voltage reduction
  – Design at very low voltage still open question (0.6V…0.9V by 2010)

• *Reduce switching activity*

• *Reduce physical capacitance*
Low-Power Design – Layout Guidelines

• Identify, in your circuit, the high switching nodes
• Use for these high activity nodes low-capacitance layers such as metal2, metal3, etc.
• Keep the wires of high activity nodes short
• Use low-capacitance layers for high capacitive nodes and busses
Low-Power Design Guidelines

• Avoid, if possible, the use of dynamic logic design style

• For any logic design, reduce the switching activity, by logic reordering and balanced delays through gate tree to avoid glitching problem

• In non-critical paths, use minimum size devices whenever it is possible without degrading the overall performance requirements

• If pass-transistor logic style is used, careful design should be considered
Charge Sharing

- Charge $Q = CV$

- A bus can be modeled as a capacitor $C_b$
  - If the voltage on the bus is sampled to determine the state of a given signal

$$\begin{align*}
  Q_b &= C_b V_b \\
  Q_s &= C_s V_s \\
  Q_T &= C_b V_b + C_s V_s \\
  V_R &= \frac{Q_T}{C_T} = \frac{(C_b V_b + C_s V_s)}{(C_b + C_s)} \\
  C_T &= C_b + C_s
\end{align*}$$
Contact Replication

- Current tends to concentrate around the perimeter in a contact hole
  - This effect, called *current crowding*, puts a practical upper limit on the size of the contact
  - When a contact or a via between different layers is necessary, make sure to maximize the contact perimeter (not area)
Ground Bounce

Ground bounce

\[ V_{\text{in}} \]

\[ V_{\text{out}} \]

\[ L \frac{di}{dt} \]

\[ V_{\text{DD Pad}} \]

\[ V_{\text{SS Pad}} \]

\[ V_L = L \frac{di}{dt} \]
Approaches for Coping with $L(di/dt)$

- Multiple power and ground pins
  - Restrict the number of I/O drivers connected to a single supply pins (reduce the $di/dt$ per supply pin)

- Careful selection of the position of the power and ground pins on the package
  - Avoid locating the power and ground pins at the corners of the package (reduce the $L$)

- Increase the rise and fall times
  - Reduce the $di/dt$

- Adding decoupling capacitances on the board
  - Separate the bonding-wire inductance from the inductance of the board interconnect
Package Issues

• Packaging requirements
  – Electrical: low parasitics
  – Mechanical: reliable and robust
  – Thermal: efficient heat removal
  – Economical: cheap
Bounding Techniques

Wire Bonding

Substrate
Die
Pad
Lead Frame
Die Cost

Single die

Wafer

Going up to 12” (30cm)
Yield Estimation

\[ Y = \frac{{\text{No. of good chips per wafer}}}{{\text{Total number of chips per wafer}}} \times 100\% \]

\[ \text{Die cost} = \frac{{\text{Wafer cost}}}{{\text{Dies per wafer} \times \text{Die yield}}} \]

\[ \text{Dies per wafer} = \frac{{\pi \times \left( \frac{\text{wafer diameter}}{2} \right)^2}}{{\text{die area}}} - \frac{{\pi \times \text{wafer diameter}}}{{\sqrt{2 \times \text{die area}}}} \]