SiGe gate oxide prepared at low-temperatures in an electron cyclotron resonance plasma

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SiGe gate oxide prepared at low temperatures (25–400 °C) by electron cyclotron resonance (ECR) plasma is reported. 100–200 Å oxides were grown on Si$_{0.8}$Ge$_{0.2}$ substrates by ECR oxidation under different bias conditions. The electrical properties of the ECR grown oxides are strong functions of processing conditions and post-processing treatments. High frequency (1 MHz) and quasi-static capacitance-voltage ECR grown oxides' measurements indicate that device quality gate oxides can be produced by this process; specifically, the fixed charge and interface state densities are comparable to those of ECR grown metal-oxide-semiconductor capacitors on silicon with an aluminum gate.

The performance of complementary metal-oxide semiconductor (CMOS) circuits is largely limited by the low transconductance of pMOS transistors which could be improved by raising the hole mobility. Motivation to use a SiGe channel instead of the conventional Si channel is strong in light of the higher hole channel mobility in this system. Previous studies of thermal oxidation of SiGe alloys revealed that either a pure SiO$_2$ layer or a mixed oxide layer consisting of SiO$_2$ and GeO$_x$ ($x = 1 - 1.2$) was formed on top of the SiGe alloy, which was accompanied by the rejection of Ge from the oxide forming Ge-rich layers. These Ge-rich layers give rise to a poor oxide with large interface states. Alternative methods of SiGe oxidation were proposed such as rapid thermal oxidation, high pressure oxidation, and low energy ion beam oxidation. However, these techniques do not produce sufficiently high quality oxide and the best results have a fixed charge density $Q_f$ above $5 \times 10^{11}$ cm$^{-2}$ and interface state density $D_{it}$ above $10^{12}$ cm$^{-2}$ eV$^{-1}$. Recently, a plasma-enhanced chemical vapor deposition (PECVD) oxide on a thin Si buffer layer over Si$_{1-x}$Ge$_x$ with low interface state density (below $10^{11}$ cm$^{-2}$ eV$^{-1}$) was reported in which interface state density decreased monotonically as the Si buffer layer thickness was increased. In this approach, however, the transconductance decreases with Si buffer layer thickness and the conducting channel exists primarily at the Si/SiO$_2$ interface and not at the SiGe/Si interface. In the thin silicon-cap limit, the density of the interface states reaches $4 \times 10^{10}$ cm$^{-2}$ eV$^{-1}$.

Electron cyclotron resonance (ECR) microwave plasma oxidation is currently being investigated as a potential alternative for thermal oxidation. The major advantage of ECR plasma is that it provides an efficient method of energy transfer directly to the electrons from the electromagnetic field, thus allowing higher charged-particle densities at lower operating pressures. The use of ECR oxygen plasma to grow thin oxide on single-crystal silicon substrates has been reported. The physical characteristics of the ECR-grown oxides on Si are identical to thermal oxides and the electrical characteristics are acceptable for device fabrication. From our previous results, Si and Ge are fully oxidized using ECR oxidation as observed from in situ x-ray photoelectron spectroscopy (XPS) and ex situ auger electron spectroscopy (AES). In this letter, we report the oxidation of SiGe by ECR microwave plasma in which the fixed charge and interface state densities obtained are lowest among methods reported in the literature.

The experiments were carried out in an ultrahigh vacuum (UHV) system equipped with a monochromatic Al $K\alpha$ x-ray photoelectron spectrometer and an ECR microwave plasma source with a maximum power of 250 W at 2.45 GHz. Samples are positioned 13 cm away from the center of the plasma source. The typical ion energies in ECR plasma were around 20 eV which is too low to damage the semiconductor surface. The SiGe samples have a 200 Å of strained Si$_{0.8}$Ge$_{0.2}$ layer grown on n-type Si (100) substrates by molecular beam epitaxy at 400 °C. A dc bias voltage was applied to the sample during the ECR oxidation process. Before being loaded into the UHV chamber, samples were chemically cleaned by acetone, methanol, de-ionized water in ultrasonic bath, etched in HCl:H$_2$O$_2$:H$_2$O = 1:1:5 and NH$_4$OH:H$_2$O$_2$:H$_2$O = 1:1:6 at 80 °C for 10 min, respectively, to remove metallic impurities and organic contaminants, and then dipped in 10% hydrofluoric acid for 15 s. Metal-oxide-semiconductor (MOS) capacitor structures were fabricated by thermal evaporation of aluminum through a shadow mask forming 100 µm diameter dots on the oxide surface.

From in situ XPS studies, we found that there is still native oxide on SiGe surface after solvent cleaning. A low temperature (up to 250 °C) in situ hydrogen plasma cleaning process was used to remove the native oxide from the SiGe surface, and subsequently oxygen plasma is activated to grow a stoichiometric SiGe oxide. We observed that both Si and Ge are fully oxidized from in situ XPS studies and there is no Ge piling up along the interface from Auger depth profile studies. The electrical properties of the ECR oxides depend strongly on the processing conditions and post-processing treatment. The fixed oxide charge and interface state densities were extracted from the capacitance-voltage (C-V) measurements.

The ECR oxides grown without prior hydrogen plasma cleaning exhibit a hysteresis upon sweeping from accumulation back into depletion in the high frequency range.
C-V curves and the hysteresis loop is reduced as the substrate bias voltage is increased from +4 to +14 V as shown in Fig. 1. But the higher bias produces a small step in the C-V curve indicating the charge trapping states created, which might be due to the plasma radiation damage. Alternatively, the hysteresis is significantly reduced if hydrogen plasma is applied to clean the SiGe surface before ECR oxidation even for low substrate bias. The cause of nonideal behavior appears to be the effect of trapping of free carriers from the channel at the oxide-SiGe interface. The magnitudes of the fixed charge and interface state densities of ECR grown oxides without prior hydrogen plasma cleaning are one order higher than those of ECR grown oxide with prior hydrogen plasma cleaning.

Figure 2(a) shows the high frequency C-V characteristics of a 100 Å ECR oxide grown at 240 W, 400 °C, 5 × 10⁻⁴ Torr with a substrate bias voltage of +4 V. Post-metallization anneal was performed in vacuo (~1 × 10⁻⁷ Torr) at 450 °C for 30 min. A positive flatband voltage of 0.3 V is observed. The measured oxide fixed charge density Qf for this film was -1.5 × 10¹¹ cm⁻² and the interface state density Din was found to be 9.2 × 10¹¹ cm⁻² eV⁻¹ [dashed line shown in Fig. 2(a)]. The quality of the ECR oxide was further improved to Qf ~ 1 × 10¹¹ cm⁻² and Din ~ 7 × 10¹¹ cm⁻² eV⁻¹ after 30 min furnace annealing in forming gas at 450 °C [solid line shown in Fig. 2(a)]. It appears that hydrogen has diffused to the SiGe-oxide interface and chemically reacts with the interface traps, making them electrically inactive. The fixed charge has a sign opposite to that found in SiO₂ on Si. This is in agreement with results observed in rapid thermal oxidation of SiGe.

It is known for Si oxidation that nonbridging oxygen sites could act as negatively charged centers when the water-related traps with which they are likely to be associated are captured by an energetic electron. Figure 2(b) shows the interface states distribution obtained from the high-frequency and quasistatic measurements of a typical furnace annealed sample. For different bias films, the electrical properties calculated from the data are listed in Table I. The fixed charge and interface state densities of ECR grown SiGe oxide are 1.5 × 10¹⁰ cm⁻² and 7 × 10¹⁰ cm⁻² eV⁻¹. As a comparison, the MOS capacitor with an aluminum gate for ECR grown oxide on silicon has Qf > 1 × 10¹¹ cm⁻² and Din > 1 × 10¹² cm⁻² eV⁻¹. The C-V characteristics of ECR grown SiGe oxides are better than those of ECR grown MOS capacitors on silicon with an aluminum gate.

In conclusion, experimental data of SiGe oxidation by ECR microwave plasma have been presented. The electrical properties of ECR grown oxide are strong functions of processing conditions and post-processing treatments. The hysteresis of C-V curve can be reduced significantly by prior hydrogen plasma cleaning or bias control. Post-metallization anneal plays an important role to reduce fixed charge Qf and interface state density Din. As shown in our experimental data, the SiGe MOS capacitor has a threshold voltage less than 1 V and an interface state density five times that of a typical Si MOS capacitor. Further studies are required to find out if the interface state density can be reduced. It appears that a higher temperature anneal and/or the replacement of aluminum by polycrystalline silicon will allow one to produce a device-quality interface suitable for integrated circuits.

TABLE I. C-V electrical testing summary for ECR grown MOS capacitors.

<table>
<thead>
<tr>
<th>H plasma</th>
<th>Vₜₜₜ (V)</th>
<th>Anneal at 450°C</th>
<th>Fixed charge, Qf (10¹¹ cm⁻²)</th>
<th>Din (10¹⁰ cm⁻² eV⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>no</td>
<td>+18</td>
<td>in vacuo</td>
<td>-8.85</td>
<td>10.2</td>
</tr>
<tr>
<td>no</td>
<td>+14</td>
<td>in vacuo</td>
<td>-8.7</td>
<td>33.9</td>
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<tr>
<td>yes</td>
<td>+7</td>
<td>in vacuo</td>
<td>-3.49</td>
<td>15</td>
</tr>
<tr>
<td>yes</td>
<td>+7</td>
<td>in forming gas</td>
<td>-1.09</td>
<td>7</td>
</tr>
<tr>
<td>yes</td>
<td>+4</td>
<td>in vacuo</td>
<td>-1.54</td>
<td>9.2</td>
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<tr>
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<td>+4</td>
<td>in forming gas</td>
<td>-1.41</td>
<td>7.2</td>
</tr>
</tbody>
</table>

FIG. 1. High-frequency (1 MHz) C-V curves for various bias conditions ECR oxides.

FIG. 2. (a) High-frequency (1 MHz) C-V curve of ECR oxide grown at 240 W, 400 °C, with substrate bias voltage of +4 V. (b) Interface states distribution of ECR oxides grown at 240 W, 400 °C with substrate bias voltage of +4 V.
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