High performance Si/SiGe heterostructure MOSFETs for low power analog circuit applications

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Abstract

We have demonstrated a high performance Si1-xGe x pMOSFET technology for low power circuit applications. The incorporation of 30% Ge in the strained Si1-xGe x channel provides a drive current enhancement by a factor of 2.7 over its counterpart Si bulk pMOSFETs and manifests a marked advantage of two decade in exponential operating region allowing both lower power consumption and a wider dynamic range for low power circuit applications. The measured low frequency noise in Si1-xGe x pMOSFETs is found to be significantly lower than in Si devices. The experimental results promise the potential of SiGe/Si heterostructure MOSFETs in radio-frequency low power circuit applications.

1. Introduction

Signal swing, power, and device performance requirements for analog circuit applications result in tradeoffs for scaled MOSFET design. The power dissipation in the analog circuits is given by \( P = \frac{8kTf}{SNR} \frac{V_{dd}}{V_{pp}} \), where \( V_{dd} \) is the power supply voltage and \( V_{pp} \), the signal voltage swing, is restricted by approximately \( (0.9V_{dd} - V_{th} - 0.2) \) [1]. The lowering of the power supply has been proposed as an approach to realize low power CMOS integrated circuits. Nevertheless, this reduction can produce an increase in the gate delay. To avoid this undesirable delay increase, signal voltage swing has to be maximized which requires very low threshold voltages. Generally, threshold voltage scaling is achieved by device scaling as technological changes, but it usually results in a higher subthreshold static current and a degradation of the noise margin. Besides maximized signal range, high transconductance (\( g_m \)) and high \( g_m/I_d \) ratio are also required for good analog performance. They have been achieved through aggressively device scaling and strict control of short channel effects. For some high performance analog applications, low flicker noise is required since it is up-converted to phase noise and thus sets a fundamental limit on the spectral purity of high-speed communication systems. However, the noise is known to increase with downscaling, which is a consequence of a less efficient fluctuations averaging, when fewer low frequency noise (LFN) sources exist in the device. These issues result in conflicting design requirements for signal swing and device performance.

SiGe heterostructure MOSFETs have been experimentally demonstrated to have superior performance in carrier mobility, transconductance, and cut-off frequency for high speed digital [2] and high frequency analog applications [3]. SiGe MOSFETs have also been predicted to have great potential to offer a significant speed advantage at the low power limit of FET operation [4]. The aforementioned reasons have motivated our investigation of Si1-xGe x channel pMOSFETs' analog performance for low power and high frequency circuit applications.
2. Device fabrication

The fabrication of Si$_{1-x}$Ge$_x$ ($x = 0, 0.15, 0.3$) pMOSFETs started from growing an undoped tri-layer by UHV-CVD on 1–5 $\Omega$cm (100) n-type Si substrates: firstly a 50 nm Si buffer layer, secondly a 15 (8) nm strained Si$_{0.85}$Ge$_{0.15}$ epilayer, and finally a top-most 7 nm Si cap layer. The Si cap layer is used to protect the underlying Si$_{1-x}$Ge$_x$ layer from being directly oxidized during gate dielectric formation and serves to provide good Si/SiO$_2$ interface quality. Moreover, the Si cap also screen the channel carriers from Si/SiO$_2$ interface scattering since holes are well-confined within Si$_{1-x}$Ge$_x$ channel. A portion of this Si cap layer ($\approx 2.5$ nm) would be consumed during the subsequent RCA clean, HF dip, and the initial gate dielectric formation. A 10 nm LPCVD-TEOS oxide was deposited at 700 °C as gate dielectric, and subsequently followed by a 200 nm of undoped polysilicon layer deposition. Polysilicon gate was patterned by optical lithography and HBr-plasma etching. Gate and source/drain were doped by BF$_2$ implantation at 20 keV with a dosage of $5 \times 10^{15}$ cm$^{-2}$. A 900 °C, 20 s rapid thermal anneal (RTA) was used to activate the dopants. Finally passivation, contact-hole etch, metal deposition/patterning, and 400 °C forming gas sintering steps were performed to complete device fabrication.

3. Results and discussion

The drain currents of Si$_{1-x}$Ge$_x$ pMOS transistors are compared in Fig. 1. A 270% enhancement in drive current (defined at $|V_{gs} - V_{th}| = 3.5$ V, $|V_{ds}| = 4$ V) is achieved at 1 $\mu$m channel length with the use of Si$_{0.7}$Ge$_{0.3}$ channel as compared to their counterpart Si pMOSFET. This is due to the effective low-field hole mobility enhancement in strained Si$_{1-x}$Ge$_x$ channels (Fig. 2) and the reduced Si/SiO$_2$ interface scattering effect as well. Typical subthreshold characteristics of Si$_{1-x}$Ge$_x$ pMOS devices in linear and saturation regions are shown in Fig. 3. The threshold voltage shifts positively with higher Ge content in Si$_{1-x}$Ge$_x$ channel due to the enhanced Ge-induced band offset at Si$_{1-x}$Ge$_x$/Si interface, which results in better hole confinement in Si$_{1-x}$Ge$_x$ quantum well and hence, the onset of heavy inversion occurs at smaller gate voltage. The transistor parameters listed in channel as compared to their counterpart Si pMOSFET.

![Fig. 2. Low-field ($V_{ds} = -0.1$ V) effective channel hole mobility for the Si$_{1-x}$Ge$_x$ pMOSFETs.](image)

![Fig. 3. Subthreshold characteristics of $L_{g,mask} = 1 \mu$m Si$_{1-x}$Ge$_x$ pMOSFETs at $V_{ds} = -0.1$ V (dashed lines) and -4 V (solid lines).](image)
Table 1
Transistor parameters extracted at 300 K for 1 μm Si_{1-x}Ge \_x pMOSFETs

<table>
<thead>
<tr>
<th>Ge content</th>
<th>x = 0</th>
<th>x = 0.15</th>
<th>x = 0.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th}$ (V)</td>
<td>$-1$</td>
<td>$-0.28$</td>
<td>$-0.16$</td>
</tr>
<tr>
<td>Subthreshold slope (mV/dec)</td>
<td>122</td>
<td>82.3</td>
<td>83</td>
</tr>
<tr>
<td>Off-state current (nA/μm)</td>
<td>0.39</td>
<td>0.1</td>
<td>0.02</td>
</tr>
<tr>
<td>Subthreshold swing (mV)</td>
<td>380</td>
<td>475</td>
<td>500</td>
</tr>
<tr>
<td>$I_{dsat}$ (mA) at $</td>
<td>V_{gs} - V_{th}</td>
<td>= 3.5$ V</td>
<td>0.34</td>
</tr>
<tr>
<td>$g_{m,linear}$ (mS/mm)</td>
<td>9.5</td>
<td>14.1</td>
<td>17.6</td>
</tr>
<tr>
<td>$\mu_{eff}$ (cm²/Vs)</td>
<td>65</td>
<td>120</td>
<td>190</td>
</tr>
</tbody>
</table>

Assuming saturation ($V_{ds} > V_{ds, sat}$), in which case the $V_{ds}$ dependence can be neglected, this relation simplifies to an exponential law. The region of the exponential channel current on gate voltage dependence for SiGe pMOSFETs is determined by plotting the subthreshold slope with respective to gate bias as shown in Fig. 4. The extent of the plateau in the Si_{0.7}Ge_{0.3} pMOSFET’s curve, which defines the practical low-power design domain, manifests a marked advantage of 2 decades in subthreshold operating region allowing both low power operation and a wider dynamic range.

For high performance analog application, very LFN is essential since it will cause an unwanted phase modulation of the signal thus providing a limit on high-speed communications. At the same time LFN has been known to be a powerful tool to characterize the quality of the interfaces of the grown epilayers. Si_{1-x}Ge \_x pMOS devices with $W/L = 10 \mu$m/5 μm were chosen to avoid short-channel or periphery effects. Typical input referred noise ($S_{g}$) spectra versus frequency for Si_{1-x}Ge \_x pMOSFETs are presented in Fig. 5. All the spectra for Si_{1-x}Ge \_x pMOSFETs are dominated by a 1/f\(^n\)-like component ($n = 1$) in the range 1–1000 Hz. No characteristic bumps in the noise spectra, indicating the
contribution of the generation–recombination noise from local levels, were observed. It clearly shows that the input referred gate voltage noise \( S_{V_{g}} \) of Si\(_{0.7}\)Ge\(_{0.3}\) pMOSFETs are considerably lower than in Si bulk devices, which was considered owing to a physical separation of the current carriers and the scattering centers by the Si cap layer [6,7]. The gate bias dependence of normalized drain current noise for the Si\(_{0.7}\)Ge\(_{0.3}\) and the Si pMOSFETs at a drain bias of −0.1 V is shown in Fig. 6. Observe that the normalized drain current noise level for the Si\(_{0.7}\)Ge\(_{0.3}\) pMOSFET is significantly lower than that of the Si pMOSFET over the entire range of gate overdrive. To determine the physical mechanism of LFN in Si\(_{1-x}\)Ge\(_x\) pMOSFETs, the normalized drain current noise, \( S_{d}/I_d^2 \), was plotted as a function of drain current in Fig. 7. The good correlation of the normalized drain current noise with the corresponding transconductance to drain current ratio squared, \( (g_m/I_d)^2 \), over a wide drain current range (weak inversion regime) indicates

\[
\frac{S_{d}}{I_d^2} = \frac{1}{2C_0} \left( \frac{1}{x} \right)^2
\]

Fig. 6. Normalized drain current noise for the Si\(_{0.7}\)Ge\(_{0.3}\) and Si pMOSFETs as a function of gate overdrive.

Fig. 7. Variation of the normalized drain current noise \( S_{d}/I_d^2 \) (solid lines) for Si\(_{0.7}\)Ge\(_{0.3}\) and Si pMOSFETs and corresponding \( (g_m/I_d)^2 \) (dashed lines) with drain currents.

that the carrier number fluctuations dominate due to hole trapping in the oxide. It should be noted that there is slight departure of the noise level from the \( (g_m/I_d)^2 \) variation at strong inversion which can be attributed to extra correlated mobility fluctuation [8]. In addition, Fig. 7 also clearly shows that higher transconductance to drain current ratio \( (g_m/I_d) \) in Si\(_{0.7}\)Ge\(_{0.3}\) pMOSFETs than in Si pFETs due to higher carrier mobility in strained Si\(_{0.7}\)Ge\(_{0.3}\) channel, which are essential for good analog performance.

4. Conclusion

We report the demonstration of a high performance with low power consumption and low noise MOSFET technology with strained Si\(_{1-x}\)Ge\(_x\) channels. The incorporation of 30% Ge in the strained Si\(_{1-x}\)Ge\(_x\) channel provides a drive current enhancement by a factor of 2.7 over its counterpart Si bulk pMOSFETs and manifests a marked advantage of an extended subthreshold region allowing both lower power consumption and a wider dynamic range for low power applications. The relative spectral density of LFN in SiGe pMOSFETs is found to be significantly lower than in Si devices. The experimental results indicate that SiGe/Si heterostructure MOSFETs offer a promising extension to the prevailing CMOS technologies affording enhanced performance at relaxed geometries for low power analog circuit applications.

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References