Chapter 5
Elements of Physical Design

Jin-Fu Li
Advanced Reliable Systems (ARES) Lab.
Department of Electrical Engineering
National Central University
Jhongli, Taiwan
Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- MOS Sizing
- Physical Design of Logic Gates
- Design Hierarchies
Basic Concepts

- **Physical design**
  - The actual process of creating circuits on silicon
  - During this phase, schematic diagrams are carefully translated into sets of geometric patterns that are used to define the on-chip physical structures

- Every layer in the CMOS fabrication sequence is defined by a distinct pattern

- The process of physical design is performed using a computer tool called a *layout editor*
  - A graphics program that allows the designer to specify the shape, dimensions, and placement

- Complexity issues are attacked by first designing simple gates and storing their descriptive files in a library subdirectory or folder
Basic Concepts

- The gates constitute **cells** in the library
- Library cells are used as building blocks by creating copies of the basic cells to construct a larger more complex circuit
  - This process is called *instantiate* of the cell
  - A copy of a cell is called an *instance*
- Much of the designer’s work is directed toward the goal of obtaining a fast circuit in the minimum amount of area
  - Small changes in the shapes or area of a polygon will affect the resulting electrical characteristics of the circuit
CAD Toolsets

- Physical design is based on the use of CAD tools
  - Simplify the procedure and aid in the verification process
- Physical design toolsets
  - Layout editor
  - Extraction routine
  - Layout versus schematic (LVS)
  - Design rule checker (DRC)
  - Place and route routine
  - Electrical rule checker (ERC)
The masking sequence of the P-substrate technology was established as:
- Start with P-type substrate
- nWell
- Active
- Poly
- pSelect
- nSelect
- Active Contact
- Poly contact
- Metal1
- Via
- Metal2
- ...

Advanced Reliable Systems (ARES) Lab.  Jin-Fu Li, EE, NCU
Layout of Basic Structures

- It is worth remembering that the features on every level have design rule specifications for the minimum width $w$ of a line, and a minimum edge-to-edge spacing $s$ between adjacent polygons.

  - For example,
Layouts of PMOS & NMOS

- **NMOS**
  - Diagram showing NMOS layout with labels for different regions.

- **PMOS**
  - Diagram showing PMOS layout with labels for different regions.
The Layout of a CMOS Inverter

- A transistor-level CMOS inverter & the corresponding layout
Layouts of a 2-Input NAND Gate
Layouts of a 2-Input NOR Gate
Cell Concepts

- The basic building blocks in physical design are called **cells**
- Logic gates as basic cells

- Note that power supply ports for $V_{dd}$ and $V_{ss}$ are chosen to be at the same locations for every cell
- The width of each cell depends on the transistor sizes and wiring used at the physical level
Create a new cell providing the function

\[ f = a'b \]
Layout of Cells

- $V_{dd}$ & $V_{ss}$ power supply lines

- $D_{m1-m1}$: edge-to-edge distance between $V_{dd}$ and $V_{ss}$
- $P_{m1-m1}$: distance between the middle of the $V_{dd}$ and $V_{ss}$ lines
- $P_{m1-m1} = D_{m1-m1} + W_{dd}$, where $W_{dd}$ is the width of the power supply lines
Layout of Cells

Layout styles of transistors

\[ V_{dd} \]

\[ V_{ss} \]
Effect of Layout Shapes

- Larger spacing between $V_{dd}$ and $V_{ss}$

- Smaller spacing between $V_{dd}$ and $V_{ss}$
Routing Channels

- Interconnection routing considerations are very important considerations for the $V_{ss}$-$V_{dd}$ spacing
- In complex digital systems, the wiring is often more complicated than designing the transistor arrays
- The general idea for routing

![Routing Channel Diagram]
High-Density Techniques

- Alternate $V_{dd}$ and $V_{ss}$ power lines and share them with cells above and below
  - For example,

```
+---------+     +---------+
| V_{dd}  |     | V_{dd}  |
|         |     |         |
| Logic cells |  Inverted logic cells |
|         |     |         |
| V_{ss}  |     | V_{ss}  |
|         |     |         |
| Inverted logic cells | Logic cells |
|         |     |         |
| V_{dd}  |     | V_{dd}  |
```

- Since no space is automatically reserved for routing, this scheme allows for high-density of placement of cells.
- The main drawback is that the connection between rows must be accomplished by using Metal2 or higher.
High-Density Techniques

- MOS transistor placement

- PMOS transistors

- NMOS transistors

- V_{dd}

- V_{ss}

- nWell

- P-substrate

- Advanced Reliable Systems (ARES) Lab.

- Jin-Fu Li, EE, NCU
Port Placement

- An example of the port placement in a cell
MOS Sizing in Physical Design

- A minimum-size MOS transistor is the smallest transistor that can be created using the design rule set.
- Scaling of the unit transistor

![Diagram of transistor scaling](image_url)
Physical Designs of Complex Gates

Advanced Reliable Systems (ARES) Lab.

Jin-Fu Li, EE, NCU
Physical Design of XNOR Gate (1)
Physical Design of XNOR Gate (2)

Advanced Reliable Systems (ARES) Lab.  Jin-Fu Li, EE, NCU
Automation of Physical Design
Standard-Cell Physical Design

Advanced Reliable Systems (ARES) Lab.

Jin-Fu Li, EE, NCU
Standard-Cell Physical Design

Advanced Reliable Systems (ARES) Lab.

Jin-Fu Li, EE, NCU
Gate-Array Physical Design

V_{dd}

V_{ss}
Gate-Array Physical Design

Gate array cells

Routing channels

V\textsubscript{dd}

V\textsubscript{ss}
Sea-of-Gate Physical Design

![Diagram of Sea-of-Gate Physical Design]

- **V_{dd}** supply
- P-transistors
- **V_{ss}** supply
- N-transistors
- poly gates
- well contacts
- substrate contacts
Sea-of-Gate Physical Design
CMOS Layout Guidelines

- Run $V_{DD}$ and $V_{SS}$ in metal at the top and bottom of the cell
- Run a vertical poly line for each gate input
- Order the poly gate signals to allow the maximal connection between transistors via abutting source-drain connection
- Place n-gate segments close to $V_{SS}$ and p-gate segments close to $V_{DD}$
- Connection to complete the logic gate should be made in poly, metal, or, where appropriate, in diffusion
Guidelines for Improving Density

- Better use of routing layers - routes can occur over cells
- More “merged” source-drain connections
- More usage of “white” space in sparse gates
- Use of optimum device sizes - the use of smaller devices leads to smaller layouts
Layout Optimization

- Vary the size of the transistor according to the position in the structure.

- In submicron technologies, where the source/drain capacitances are less, such that this improvement is limited.
Layout Optimization

Advanced Reliable Systems (ARES) Lab.

Jin-Fu Li, EE, NCU
Layouts of Transmission Gates
Routing to Transmission Gates
2-Input Multiplexer
Design Hierarchies

Layout level

Cell library

Subsystems

Chips
Summary

- Basic physical design concepts have been introduced
- Cell concepts have also presented
- Layout optimization guidelines have been summarized
- Design hierarchy has been briefly introduced