Chapter 5
Elements of Physical Design

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Outline

- Basic Concepts
- Layout of Basic Structures
- Cell Concepts
- MOS Sizing
- Physical Design of Logic Gates
- Design Hierarchies
Basic Concepts

- **Physical design**
  - The actual process of creating circuits on silicon
  - During this phase, schematic diagrams are carefully translated into sets of geometric patterns that are used to define the on-chip physical structures

- Every layer in the CMOS fabrication sequence is defined by a distinct pattern

- The process of physical design is performed using a computer tool called a *layout editor*
  - A graphics program that allows the designer to specify the shape, dimensions, and placement

- Complexity issues are attacked by first designing simple gates and storing their descriptive files in a *library* subdirectory or folder
Basic Concepts

- The gates constitute **cells** in the library

- Library cells are used as building blocks by creating copies of the basic cells to construct a larger more complex circuit
  - This process is called **instantiate** of the cell
  - A copy of a cell is called an **instance**

- Much of the designer’s work is directed toward the goal of obtaining a fast circuit in the minimum amount of area
  - Small changes in the shapes or area of a polygon will affect the resulting electrical characteristics of the circuit
**CAD Toolsets**

- Physical design is based on the use of CAD tools
  - Simplify the procedure and aid in the verification process
- Physical design toolsets
  - Layout editor
  - Extraction routine
  - Layout versus schematic (LVS)
  - Design rule checker (DRC)
  - Place and route routine
  - Electrical rule checker (ERC)
Layout of Basic Structures

- The masking sequence of the P-substrate technology was established as
  - Start with P-type substrate
  - nWell
  - Active
  - Poly
  - pSelect
  - nSelect
  - Active Contact
  - Poly contact
  - Metal1
  - Via
  - Metal2
  - ...

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Layout of Basic Structures

It is worth remembering that the features on every level have design rule specifications for the minimum width $w$ of a line, and a minimum edge-to-edge spacing $s$ between adjacent polygons.

For example,
Design Rules

- Design rules (layout rules)
  - Provide a necessary communication link between circuit designers and process engineers during manufacturing phase
  - The goal of design rules is to achieve the optimum yield of a circuit with the smallest area cost

- Design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs
Design Rules

- The design rules primarily address two issues
  - The geometrical reproduction of features that can be reproduced by the mask-making and lithographical process
  - The interactions between different layers

- Lambda-based rules
  - Based on a single parameter, lambda, which characterizes the linear feature – the resolution of the complete wafer implementation process
Examples of Design Rules

- **Well**
  - Same Potential
  - Different Potential
  - 0 or 6
  - 10

- **Active**
  - 3

- **Contact or Via Hole**
  - 2

- **Polysilicon**
  - 2

- **Metal1**
  - 3
Transistor Layout
Design Rules for Vias & Contacts

1. Via
2. Metal to Poly Contact
3. Metal to Active Contact

Images showing the design rules with numbers indicating the rules.
Design Rule Checker
Layouts of PMOS & NMOS

- **NMOS**

- **PMOS**
The Layout of a CMOS Inverter

- A transistor-level CMOS inverter & the corresponding layout
Layouts of a 2-Input NAND Gate
Layouts of a 2-Input NOR Gate

![Diagram of 2-Input NOR Gate]
Cell Concepts

- The basic building blocks in physical design are called **cells**
- Logic gates as basic cells

- Note that power supply ports for $V_{dd}$ and $V_{ss}$ are chosen to be at the same locations for every cell.
- The width of each cell depends on the transistor sizes and wiring used at the physical level.
Cell Creation Using Primitive Cells

Create a new cell providing the function

\[ f = a'b \]
Layout of Cells

- **V\text{dd}** & **V\text{ss}** power supply lines

- \( D_{m1-m1} \): edge-to-edge distance between **V\text{dd}** and **V\text{ss}**
- \( P_{m1-m1} \): distance between the middle of the **V\text{dd}** and **V\text{ss}** lines
- \( P_{m1-m1} = D_{m1-m1} + W_{dd} \), where \( W_{dd} \) is the width of the power supply lines
Layout of Cells

- Layout styles of transistors

![Diagram showing layout styles of transistors with Vdd and Vss at the top and bottom, respectively, and WP and WN labels indicating different widths.]
Effect of Layout Shapes

- Larger spacing between $V_{dd}$ and $V_{ss}$

- Smaller spacing between $V_{dd}$ and $V_{ss}$
Routing Channels

- Interconnection routing considerations are very important considerations for the $V_{ss}$-$V_{dd}$ spacing
  - In complex digital systems, the wiring is often more complicated than designing the transistor arrays
- The general idea for routing
High-Density Techniques

- Alternate $V_{dd}$ and $V_{ss}$ power lines and share them with cells above and below
  - For example,

- Since no space is automatically reserved for routing, this scheme allows for high-density of placement of cells
  - The main drawback is that the connection between rows must be accomplished by using Metal2 or higher
High-Density Techniques

- MOS transistor placement

- PMOS transistors
  - $V_{dd}$
  - nWell
  - P-substrate
  - $V_{ss}$
  - P-substrate
  - nWell
  - $V_{dd}$

- NMOS transistors
  - P-substrate
  - nWell

- PMOS transistors
  - $V_{dd}$
Port Placement

- An example of the port placement in a cell
MOS Sizing in Physical Design

- A minimum-size MOS transistor is the smallest transistor that can be created using the design rule set.
- Scaling of the unit transistor

![Diagram showing MOS transistor scaling]

- Scaling by 2X
- Scaling by 4X

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Physical Designs of Complex Gates
Physical Design of XNOR Gate (1)
Physical Design of XNOR Gate (2)
Automation of Physical Design

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Standard-Cell Physical Design
Standard-Cell Physical Design
Gate-Array Physical Design
Gate-Array Physical Design

V_{dd}

Gate array cells

V_{ss}

Routing channels
Sea-of-Gate Physical Design

- Well contacts
- N-transistors
- P-transistors
- Poly gates
- V_{dd} supply
- V_{ss} supply
- Substrate contacts
- Supply well contacts
Sea-of-Gate Physical Design
CMOS Layout Guidelines

- Run $V_{DD}$ and $V_{SS}$ in metal at the top and bottom of the cell
- Run a vertical poly line for each gate input
- Order the poly gate signals to allow the maximal connection between transistors via abutting source-drain connection
- Place n-gate segments close to $V_{SS}$ and p-gate segments close to $V_{DD}$
- Connection to complete the logic gate should be made in poly, metal, or, where appropriate, in diffusion
Guidelines for Improving Density

- Better use of routing layers - routes can occur over cells
- More “merged” source-drain connections
- More usage of “white” space in sparse gates
- Use of optimum device sizes - the use of smaller devices leads to smaller layouts
Vary the size of the transistor according to the position in the structure

In submicron technologies, where the source/drain capacitances are less, such that this improvement is limited.
Layout Optimization

Right vs Wrong
Layouts of Transmission Gates
Routing to Transmission Gates
2-Input Multiplexer

\[ a \quad b \quad c \quad -c \quad a \quad b \quad z \]

\[ c \quad a \quad c \quad -c \quad a \quad b \quad z \]

\[ c \quad -c \quad c \quad a \quad b \quad \]

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Design Hierarchies

- Layout level
- Cell library
- Subsystems
- Chips
Summary

- Basic physical design concepts have been introduced
- Cell concepts have also presented
- Layout optimization guidelines have been summarized
- Design hierarchy has been briefly introduced