EE6083 VLSI Testing

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Syllabus

Contents

- Introduction
- Fault Modeling
- Testability Measures
- Fault Simulation
- Test Generation
- Design-for-Testability and Built-In Self-Test
- Test Standards: IEEE 1149.1 & IEEE 1500
- Memory Testing
- Basics of SOC and 3D IC Testing
**Syllabus**

- **Reference Books**

- **Grading**
  - Homework 30%
  - (Midterm + Final) 70%

- **Prerequisite**
  - Digital Logic Design

- **Key dates**
  - Midterm: 10:00-12:00, Thur., Nov. 8, E1-019
  - Final: 10:00-12:00, Thur., Jan. 17, E1-019
What Does an IC Do?

- Consumer Electronic Products
  - http://www.youtube.com/watch?v=B-RuuD2gR-c

- Cloud Computing
- Automotive
- Green Technology

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What Does an IC Look Like?

SPARC SOC Processor (IEEE JSSC, 2011)

1. TSMC 40nm high performance process (11 Cu metals and four transistor types)
2. 16 cores
3. Die area=377mm²
4. 1 billion transistors and 2.5 million flip-flops
5. 1.65-2.0 GHz consuming 120W
6. 833 signals and 1284 power pins
7. Scan test, MBIST, Loop-back tests (SerDes)
How is an IC Created?

1. **Design**
   - System → Behavior → Circuit → Layout

2. **Manufacturing**
   - Corrected Layout → Mask → Wafer → Package Die

3. **Test**
   - Wafer Sort → Burn-In → Final Test
Architecture of Current ICs

- Multi-core chip architecture
  - Use multiple identical cores to design a chip
- Network-on-chip communication infrastructure
  - Multiple point-to-point data links interconnected by switches (i.e., routers)


Importance of Testing Techniques

- Testing technique play an important role in current multicore chips
  - Quality insurance
  - Yield-improvement
  - Reliability-improvement
  - Monitoring
  - Diagnosis
  - …
**Example: Niagara2 & POWER6 (JSSC, 2008)**

Niagara2 (Sun)

POWER6 (IBM)

Design-for-Testability Features:

1. 32 Scans + ATPG
2. BIST for arrays
3. ...
Number of Txs per uP Chip

Transistor Cost

Semiconductor Learning Curve

Historical Cost/Transistor
-35% per Year
Inevitable future reduction in cost/transistor will slow when cumulative transistor unit volume growth slows

SOC Consumer Portable Processing Performance Trends

Source: ITRS 2011
SOC Consumer Portable Design Complexity Trends

Source: ITRS 2011
Downsizing Rates of Audio/Video Products

3D Integration Technology Using TSV

- 3D integration technology using through silicon via (TSV)
- Multiple dies are stacked and TSV is used for the inter-die interconnection

The fabrication flow of a 3D IC
- Die/wafer preparation
- Die/wafer assembly

Source: KAIST
Heterogeneous Integration

- Combine disparate technologies
  - DRAM, flash, RF, etc.
- Combine different technology nodes
  - For example: 65nm technology and 45nm technology
Low Power & Small Form Factor

Power

SOB

SIP

Technology

3D-IC

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Low Power & Small Form Factor

- 3D IC allows much more IO resources than 2D IC
- For example,
  - Stacking of processor and memory

Bandwidth is limited by IOs

Many TSVs are allowed for high bandwidth transportation
Challenges of 3D ICs

- Yield
- Design for resiliency
- Thermal
- Can we overcome it?
- Test
- Reliability
- ...

Source: IBM, 2008.
Test Knowledge is Important

- A profound understanding of the principles of manufacturing and test is essential for an engineer to design a quality product
- More and more design-for-testability (DFT) circuits should be added in current SOCs
- In the era of 3D integration technology
  - A 3D IC needs much more DFT circuits than a 2D one to cope with many issues induced by the 3D integration
- Knowledge of chip testing and system testing is needed
<table>
<thead>
<tr>
<th>Challenges ≥ 22nm</th>
<th>Summary of Issues</th>
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</thead>
<tbody>
<tr>
<td>Design productivity</td>
<td>System-level: high level of abstraction (HW/SW) functionalty spec, platform-based</td>
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<td>design, multi-processor programmability, system integration, AMS codesign and</td>
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<td>automation</td>
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<td>Verification: executable specification, ESL formal verification, intelligent test</td>
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<td>bench, coverage-based verification</td>
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<td>Logic/circuit/physical: analog circuit synthesis, multi-objective optimization</td>
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<td>Logic/circuit/physical: SIP and 3D (TSV-based) planning and implementation flows</td>
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<td>Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)</td>
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<td>Power consumption</td>
<td>Logic/circuit/physical: dynamic and static, system- and circuit-level power</td>
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<td>optimization</td>
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<td>Manufacturability</td>
<td>Performance/power variability, device parameter variability, lithography</td>
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<td>limitations</td>
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<td>impact on design, mask cost, quality of (process) models</td>
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<td>ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT</td>
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<td>Interference</td>
<td>Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis</td>
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<tr>
<td>Reliability and resilience</td>
<td>Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction</td>
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ATE—automatic test equipment  
EMI—electromagnetic interference  
silicon on insulator  
BISR—built-in self repair  
BIST—built-in self test  
ESL—Electronic System Level  
HW/SW—hardware/software  
MTTF—mean time to failure  
SOI—single oxide isolation  

Source: ITRS2011
## Overall Design Technology Challenges

<table>
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<tr>
<th>Challenges &lt; 22nm</th>
<th>Summary of Issues</th>
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| Design productivity | Verification: complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage  
Tools specific for SOI and non-static logic, and emerging devices  
Cost-driven design flow |
| Power consumption | Logic/circuit/physical: SOI power management  
Logic/circuit/physical: Reliability and resilience- and temperature-constrained 3D physical implementation flows |
| Manufacturability | Uncontrollable threshold voltage variability  
Advanced analog/mixed signal DFT (digital, structural, radio), “statistical” and yield-improvement DFT  
Thermal BIST, system-level BIST |
| Interference | Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.) |
| Reliability and resilience | Autonomic computing, robust design, SW reliability and resilience |

Source: ITRS2011