Chapter 1 Introduction

Jin-Fu Li
Advanced Reliable Systems (ARES) Laboratory
Department of Electrical Engineering
National Central University
Jungli, Taiwan
Outline

- VLSI Realization
- Role of Testing
- Verification & Testing
- Defects, Faults, and Errors
- VLSI Testing Concepts
- Testing Economics
- Test Quality Measure
VLSI Realization Process

Customer’s need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer
Definitions

☐ Design synthesis
  ■ Given an I/O function, develop a procedure to manufacture a device using known materials and processes

☐ Verification
  ■ Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function

☐ Test
  ■ A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect
VLSI Design Cycle

- Concept
  - Designer
    - Behavior Specification
      - Behavior Synthesis
        - RTL Design
          - Logic Synthesis
            - Netlist (Logic Gates)
              - Layout Synthesis
                - Layout (Masks)
                  - Manufacturing
                    - Final Product
                      - Product Verification
            - Logic Verification
                - RTL Verification
                  - Design Validation
            - Logic Verification
                - RTL Verification
                  - Design Validation
                      - Concept

Verification

- The four representations of the design
  - Behavioral, RTL, gate level, and layout
- In mapping the design from one phase to another, it is likely that some errors are produced
  - Caused by the CAD tools or human mishandling of the tools
- Usually, simulation is used for verification, although more recently, formal verification has been gaining in importance
- Two types of simulations are used to verify the design
  - Functional simulation & timing simulation
Functional & Timing Simulations

☐ Functional simulation
  ▪ No delays (or, at most, constant delay) of the functional units are included
  ▪ The primary concerns
    □ To check if each block performs intended function
    □ To modify the design to evaluate alternatives before finalizing the design

☐ Timing simulation
  ▪ The delays associated with the various gates are assigned
  ▪ Usually, nominal delays are assigned to the gates
  ▪ Actual verification of the prototype gives more assurance, since it embodies the process-dependent parameters
Role of Testing

- If you design a product, fabricate, and test it, and it fails the test, then there must be a cause for the failure
  - Test was wrong
  - The fabrication process was faulty
  - The design was incorrect
  - The specification problem

- The role of *testing* is to detect whether something went wrong and the role of *diagnosis* is to determine exactly what went wrong

- Correctness and effectiveness of testing is most important for quality products
Benefits of Testing

- *Quality* and *economy* are two major benefits of testing.
- The two attributes are greatly dependent and can not be defined without the other.
- Quality means satisfying the user’s needs at a minimum cost.
- The purpose of testing is to weed out all bad products before they reach the user.
  - The number of bad products heavily affect the price of good products.
- A profound understanding of the principles of manufacturing and test is essential for an engineer to design a quality product.
Feature Size and Transistors

- Semiconductor Industry Association’s (SIA’s)
Transistors Per I/O

- Semiconductor Industry Association’s (SIA’s)
Trends of Testing

- Two key factors are changing the way of VLSI ICs testing
  - The manufacturing test cost has been not scaling
  - The effort to generate tests has been growing geometrically along with product complexity

![Graph showing trends in Si capital and test capital](graph.png)
Test Knowledge is Important

- Testing is becoming a factor in design optimization
- Designers customarily strive for an optimal design
  - A high-speed, low-power design occupying the smallest possible area
- Conventionally, the designer often optimize one of the tree attributes: speed (or delay), area, and power
- At present, a fourth attribute is considered
  - Testability
- Nowadays, the testability cycle should parallel the design cycle
DFT Cycle

Behavioral Description
→ Behavioral DFT Synthesis
→ RTL Description
→ Logic DFT Synthesis
→ Gate Description
→ Test Pattern Generation
→ Fault Coverage?

Gate
→ Technology Mapping
→ Layout
→ Parameter Extraction
→ Manufacturing
→ Product
→ Test Application
→ Good Product

Low

High
**Verification & Test**

**Verification**
- Verifies correctness of design
- Performed by simulation, hardware emulation, or formal methods
- Perform once before manufacturing
- Responsible for quality of design

**Test**
- Verifies correctness of manufactured hardware
- Two-part process
  - Test generation: software process executed once during design
  - Test application: electrical tests applied to hardware
- Test application performed on every manufactured device
- Responsible for quality of device
Reconvergent path model
System to Silicon

System Requirements

Algorithm

Hardware Architecture

System Integration

Fabricate and Test

Physical

Design For Test

[Source: MITRE]
Defect, Fault, and Error

- **Defect**
  - A defect is the unintended difference between the implemented hardware and its intended design.
  - Defects occur either during manufacture or during the use of devices.

- **Fault**
  - A representation of a *defect* at the abstracted function level.

- **Error**
  - A wrong output signal produced by a defective system.
  - An error is caused by a *Fault* or a design error.
Typical Types of Defects

- Extra and missing material
  - Primarily caused by dust particles on the mask or wafer surface, or in the processing chemicals

- Oxide breakdown
  - Primarily caused by insufficient oxygen at the interface of silicon (Si) and silicon dioxide (SiO₂), chemical contamination, and crystal defects

- Electromigration
  - Primarily caused by the transport of metal atoms when a current flows through the wire
  - Because of a low melting point, aluminum has large self-diffusion properties, which increase its electromigration liability
Example

- Consider one two-input AND gate

- Defect: a short to ground

- Fault: signal b stuck at logic 0
- Error: a=1, b=1, c=0 (correct output c=1)
- Note that the error is not permanent. As long as at least one input is 0, there is no error in the output
Defect, Fault, and Error

- Different types of defects may cause the same fault

- Different types of faults may cause the same error
  - E.g., A stuck-at-0, Y=1; C stuck-at-1, Y=1
The Test Problem

Defect → Fault → Test pattern → Fault coverage

Fault modeling → Test pattern generation → Fault simulation

<table>
<thead>
<tr>
<th></th>
<th>C</th>
<th>D</th>
<th>Y</th>
<th>Y(C is S/1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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Ideal Tests & Real Tests

□ The problems of ideal tests
- Ideal tests detect all defects produced in the manufacturing process
- Ideal tests pass all functionally good devices
- Very large numbers and varieties of possible defects need to be tested
- Difficult to generate tests for some real defects

□ Real tests
- Based on analyzable fault models, which may not map on real defects
- Incomplete coverage of modeled faults due to high complexity
- Some good chips are rejected. The fraction (or percentage) of such chips is called the yield loss
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the defect level
How to Test Chips?

Test patterns

---11
---01
......
---00
---10

Circuit under test

Test responses

10---
00---
......
01---
10---

Stored Correct Responses

Comparator

Test result
Cost of Test

- Design for testability (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead

- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging

- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost
ADVENTEST Model T6682 ATE

- Consists of
  - Powerful computer
  - Powerful 32-bit digital signal processor (DSP) for analog testing
  - Probe head: actually touches the bare dies or packaged chips to perform fault detection experiments
  - Probe card: contains electronics to measure chip pin or pad
Internal Structure of the ATE

Chip Under Test (CUT)

Pin Electronics

Clocking

Generators

Analyzers

Internal Bus

Pattern Memory

System Controller

Disk

Workstation

Test Program

Source: H.-J. Huang, CIC
ATE Test Operation

Source: H.-J. Huang, CIC

STIL 1.0;

Input Stimulus

Input Drivers

CUT

Expected Response

Actual Response

Pattern Memory

Compare Output

Test Program

Pass/Fail

Local Per-Pin Memory

Advanced Reliable Systems (ARES) Lab.
Jin-Fu Li, EE, NCU
Types of Test

- **Characterization testing**
  - A.k.s. *design debug* or *verification testing*
  - Performed on a new design before it is sent to production
  - Verify whether the design is correct and the device will meet all specifications
  - Functional tests and comprehensive AC and DC measurements are made
  - A characterization test determines the exact limits of device operation values

- **DC Parameter tests**
  - Measure steady-state electrical characteristics
  - For example, threshold test
    - $0 < V_{OL} < V_{IL}$
    - $V_{IH} < V_{OH} < V_{CC}$
Types of Test

- **AC parametric tests**
  - Measure transient electronic characteristics
  - For example:
    - Rise time & fall time tests
Types of Test

- **Production testing**
  - Every fabricated chip is subjected to production tests
  - The test patterns may not cover all possible functions and data patterns but must have a high fault coverage of modeled faults
  - The main driver is cost, since every device must be tested. Test time must be absolutely minimized
  - Only a go/no-go decision is made
  - Test whether some device-under-test parameters are met to the device specifications under normal operating conditions

- **Burn-In testing**
  - Ensure reliability of tested devices by testing
  - Detect the devices with potential failures
**Types of Test**

- The potential failures can be accelerated at elevated temperatures.
- The devices with *infant mortality failures* may be screened out by a short-term burn-in test in an accelerate.

- Failure rate versus product lifetime (*bathtub curve*)

![Bathtub Curve Diagram](image-url)
Testing Economics

- Chips must be tested before they are assembled onto PCBs, which, in turn, must be tested before they are assembled into systems.

- The rule of ten
  - If a chip fault is not detected by chip testing, then finding the fault costs 10 times as much at the PCB level as at the chip level.
  - Similarly, if a board fault is not found by PCB testing, then finding the fault costs 10 times as much at the system level as at the board level.

- Some claim that the rule of ten should be renamed the rule of twenty
  - Chips, boards, and systems are more complex.
VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol $Y$.
- Cost of a chip

\[
\text{Cost of fabricating and testing a wafer} = \frac{\text{Yield} \times \text{Number of chip sites on the wafer}}{\text{Cost of fabricating and testing a wafer}}
\]
VLSI Chip Yield

Wafer yield = $\frac{12}{22} = 0.55$

Wafer yield = $\frac{17}{22} = 0.77$
Fault Coverage & Defect Level

- **Fault coverage (FC)**
  - The measure of the ability of a test (a collection of test patterns) to detect a given faults that may occur on the device under test
  - FC = #(detected faults) / #(possible faults)

- **Defect level (DL)**
  - The ratio of faulty chips among the chips that pass tests
  - DL is measured as defects per million (DPM)
  - DL is a measure of the effectiveness of tests
  - DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 DPM is considered unacceptable

- \[ DL = 1 - Y^{(1-FC)} \text{ and } 0 < DL \leq 1 - Y \]
Defect Level & Quality Level

- For example, required FC for DL=200 DPM

<table>
<thead>
<tr>
<th>Y(%)</th>
<th>10</th>
<th>50</th>
<th>90</th>
<th>95</th>
<th>99</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC(%)</td>
<td>99.991</td>
<td>99.97</td>
<td>99.8</td>
<td>99.6</td>
<td>98</td>
</tr>
</tbody>
</table>

- Quality level (QL)
  - The fraction of good parts among the parts that pass all the tests and are shipped
  - \( QL = 1 - DL = Y^{(1-FC)} \) and \( 0 \leq QL \leq 1 \)

- Consequently, fault coverage affects the quality level