Chapter 1
Introduction to CMOS Circuit Design

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Outline

- Introduction
- MOS Transistor Switches
- CMOS Logic
- Circuit and System Representation
**Binary Counter**

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ A = a'b' + ab' \]
\[ B = a'b + ab' \]

Source: Prof. V. D. Agrawal
1-bit Multiplier

\[ C = A \times B \]
Switch: MOSFET

- MOSFETs are basic electronic devices used to direct and control logic signals in IC design
  - MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
  - N-type MOS (NMOS) and P-type MOS (PMOS)
  - Voltage-controlled switches
- A MOSFET has four terminals: gate, source, drain, and substrate (body)
- Complementary MOS (CMOS)
  - Using two types of MOSFETs to create logic networks
  - NMOS & PMOS
P-N Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

\[\text{p-type} \quad \text{n-type}\]

anode       cathode
NMOS Transistor

- Four terminals: gate, source, drain, body
- Gate-oxide-body stack looks like a capacitor
  - Gate and body are conductors
  - SiO₂ (oxide) is a very good insulator
  - Called metal-oxide-semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal
NMOS Operations

- Body is commonly tied to ground (0 V)

- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF
**NMOS Operations (Cont.)**

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON
PMOS Operations

- Similar, but doping and voltages reversed
  - Body tied to high voltage ($V_{DD}$)
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

![PMOS Diagram]

- Polysilicon
- SiO₂
- Source
- Gate
- Drain
- p⁺
- n
- bulk Si
Threshold Voltage

- Every MOS transistor has a characterizing parameter called the threshold voltage $V_T$
- The specific value of $V_T$ is established during the manufacturing process
- Threshold voltage of an NMOS and a PMOS

**NMOS**
- Gate-source voltage
  - $V_A = 1$: Mn On
  - $V_A = 0$: Mn Off
- Logic translation

**PMOS**
- Gate-source voltage
  - $V_A = 1$: Mp Off
  - $V_A = 0$: Mp On
- Logic translation
MOS Transistor is Like a Tap...

Source: Prof. Banerjee, ECE, UCSB
MOSFET & FinFET

MOSFET

Bulk FinFET

SOI FinFET
IG & SG FinFETs

According to the gate structure, FinFET can be classified as
- Independent-Gate (IG) FinFET
- Short-Gate (SG) FinFET
MOS Switches

☐ NMOS symbol and characteristics

☐ PMOS symbol and characteristics
CMOS Switch

A complementary CMOS switch

- Transmission gate

Symbols

Characteristics
**CMOS Logic - Inverter**

- The NOT or INVERT function is often considered the simplest Boolean operation
  - \[ F(x) = \text{NOT}(x) = x' \]

![Logic Level Diagram]

- **Logic Level Diagram**
  - 0: Vdd, 1: 0, Vdd/2: Indeterminate logic level

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Advanced Reliable Systems (ARES) Lab.  Jin-Fu Li, EE, NCU
Combinational Logic

- Serial structure

Diagram showing the truth table and logic symbols for serial structure with inputs a and b and outputs S1 and S2.
Combinational Logic

Parallel structure

\[ a \neq b \quad a = b \]

\[ a = b \quad a \neq b \]
NAND Gate

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
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<tr>
<td>1</td>
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<td>0</td>
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</table>

Output

A B

NAND gate circuit diagram
NOR Gate

A
B

<table>
<thead>
<tr>
<th></th>
<th>0</th>
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</table>

A
B

Output
Compound Gate

\[ F = ((AB) + (CD)) \]
Structured Logic Design

- CMOS logic gates are intrinsically inverting
  - The output always produces a NOT operation acting on the input variables
- For example, the inverter shown below illustrates this property

```
<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
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</table>
```

![Inverter Diagram](attachment:inverter_diagram.png)
Structured Logic Design

- The inverting nature of CMOS logic circuits allows us to construct logic circuits for AOI and OAI expressions using a structured approach.

- **AOI logic function**
  - Implements the operations in the order **AND then OR then NOT**
  - E.g., \( g(a, b, c, d) = a.b + c.d \)

- **OAI logic function**
  - Implements the operations in the order **OR then AND then NOT**
  - E.g., \( g(a, b, c, d) = (a + b) \cdot (c + d) \)
Structured Logic Design

- Behaviors of nMOS and pMOS groups
  - Parallel-connected nMOS
    - OR-NOT operations
  - Parallel-connected pMOS
    - AND-NOT operations
  - Series-connected nMOS
    - AND-NOT operations
  - Series-connected pMOS
    - OR-NOT operations

- Consequently, wired groups of nMOS and pMOS are logical duals of another
Dual Property

- If an NMOS group yields a function of the form
  \[ g = a \cdot (b + c) \]

  then an identically wired PMOS array gives the dual function
  \[ G = a + (b \cdot c) \]

  where the AND and OR operations have been interchanged

- This is an interesting property of NMOS-PMOS logic that can be exploited in some CMOS designs
An Example of Structured Design

\[ X = a + b \cdot (c + d) \]
An Example of XOR Gate

- Boolean equation of the two input XOR gate
  - \( a \oplus b = \overline{a} \cdot b + a \cdot \overline{b} \), this is not in AOI form
  - But, \( a \oplus b = a \cdot b + \overline{a} \cdot \overline{b} \), this is in AOI form
  - Therefore, \( a \oplus b = (a \oplus b) = a \cdot b + \overline{a} \cdot \overline{b} \)

- XOR Gate

- XNOR Gate
Multiplexer
Static CMOS Summary

- In static circuits at every point in time (except when switching), the output is connected to either Vdd or Gnd through a low resistance path.
  - Fan-in of \( n \) (or \( n \) inputs) requires \( 2n \) (\( n \) N-type and \( n \) P-type) devices.

- Non-ratioed logic: gates operate independent of PMOS or NMOS sizes.

- No path ever exists between Vdd and Gnd: low static power.

- Fully-restored logic (NMOS passes “0” only and PMOS passes “1” only).

- Gates must be inverting.
Design Flow for a VLSI Chip

Specification

Behavioral Design

- Function
- Function

- Function

Structural Design

Physical Design

- Timing
- Power
Circuit and System Representations

- **Behavioral representation**
  - Functional, high level
  - For documentation, simulation, verification

- **Structural representation**
  - System level – CPU, RAM, I/O
  - Functional level – ALU, Multiplier, Adder
  - Gate level – AND, OR, XOR
  - Circuit level – Transistors, R, L, C
  - For design & simulation

- **Physical representation**
  - For fabrication
Behavior Representation

- A one-bit full adder (Verilog)

```
module fadder(sum, cout, a, b, ci);
output sum, cout;
input a, b, ci;
reg sum, cout;

always @(a or b or ci) begin
    sum = a^b^ci;
    cout = (a&b)|(b&ci)|(ci&a);
end
endmodule
```

![Fadder Diagram]

ci → fadder → cout
a  b
   ↓  ↓
   sum
A four-bit full adder (Verilog)

```verilog
module adder4(s4, s3, s2, s1, s0, ci);
    output[3:0] sum;
    output c4;
    input[3:0] a, b;
    input ci;
    reg[3:0] s;
    reg c4;
    wire[2:0] co;
    fadder a0(s[0], co[0], a[0], b[0], ci);
    fadder a1(s[1], co[1], a[1], b[1], co[0]);
    fadder a2(s[2], co[2], a[2], b[2], co[1]);
    fadder a3(s[3], c4, a[3], b[3], co[2]);
endmodule
```
Physical Representation

- Layout of a 4-bit NAND gate