Chapter 3
Fabrication of CMOS Integrated Circuits

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Outline

- Background
- The CMOS Process Flow
- Latchup
- Antenna Rules & Layer Density Rules
- CMOS Process Enhancements
- Summary
Introduction

☐ An integrated circuit is created by stacking layers of various materials in a pre-specified sequence.

☐ Both the electrical properties of the material and the geometrical patterns of the layer are important in establishing the characteristics of devices and networks.

☐ Most layers are created first, and then patterned using lithographic sequence.

☐ Doped silicon layers are the exception to this rule.
Material Growth and Deposition

- **Silicon Dioxide (SiO$_2$)**
  - An excellent electrical insulator
  - It can be *grown* on a silicon wafer or *deposited* on top of the wafer
  - Thermal oxidation
  - Chemical vapor deposition (CVD) oxidation

- **Silicon Nitride (Si$_3$N$_4$)**
  - A.k.a. nitride
  - Nitrides act as strong barriers to most atoms, this makes them ideal for use as an overglass layer

- **Polycrystal Silicon**
  - Called *polysilicon* or just *poly* for short
  - It is used as the gate material in MOSFETs
  - It adheres well to silicon dioxide
Material Growth and Deposition

- **Metals**

  - **Aluminum (Al)** is the most common metal used for interconnect wiring in ICs
    - It is prone to *electromigration*
    - \( J = \frac{I}{A}; A = wt \) is the cross-section area
    - Layout engineers cannot alter the thickness \( t \) of the layer
    - Electromigration is thus controlled by specifying the minimum width \( w \) to keep \( J \) below a max. value

  - **Copper (Cu)** has recently been introduced as a replacement to aluminum
    - Its resistivity is about one-half the value of Al
    - Standard patterning techniques cannot be used on copper layers; specialized techniques had to be developed
Material Growth and Deposition

- **Doped Silicon Layers**
  - Silicon wafer is the starting point of the CMOS fabrication process
  - A doped silicon layer is a patterned n- or p-type section of the wafer surface
  - This is accomplished by a technique called ion implantation

- **Basic section of an ion implanter**
Material Growth and Deposition

- The process of deposition causes that the top surface has hillocks
  - If we continue to add layers (e.g., metal layers), the surface will get increasing rough and may lead to breaks in fine line features and other problems
  - Surface planarization is required
- Chemical-Mechanical Polishing (CMP)
  - It uses a combination of chemical etching and mechanical sanding to produce planar surfaces on silicon wafers
- Surface planarization

![Diagram of material growth and deposition](image)
Lithography

- One of the most critical problems in CMOS fabrication is the technique used to create a pattern.
  - Photolithography
- The photolithographic process starts with the desired pattern definition for the layer.
- A mask is a piece of glass that has the pattern defined using a metal such as chromium.
Transfer a Mask to Silicon Surface

- The process for transferring the mask pattern to the surface of a silicon region
  - Coat photoresist
  - Exposure step
  - Etching
- Coat photoresist
  - Liquid photoresist is sprayed onto a spinning wafer
- Exposure
  - Photoresist is sensitive to light, such as ultraviolet (UV)
Transfer a Mask to Silicon Surface

- The figure shown below depicts the main idea.

- The hardened resist layer is used to protect underlying regions from the etching process.

- Etching
  - The chemicals are chosen to attack and remove the material layer not shielded by the hardened photoresist.
Doping

- The figure shows the etching process

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Oxide layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardened resist layer</td>
<td>Patterned oxide layer</td>
</tr>
</tbody>
</table>

- Creation of doped silicon

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Arsenic ions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral doping</td>
<td>N+ N+</td>
</tr>
</tbody>
</table>

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Doping

- The conductive characteristics of intrinsic silicon can be changed by introducing impurity atoms into the silicon crystal lattice.
- Impurity elements that use (provide) electrons are called as acceptor (donor).
- Silicon that contains a majority of donors (acceptor) is known as n-type (p-type).
- When n-type and p-type materials are merged together, the region where the silicon changes from n-type to p-type is called junction.
MOS Transistor

- Basic structure of a NMOS transistor
Fabrication Steps for an NMOS

1. Patterning SiO₂ Layer
2. Implant or Diffusion
3. Gate Oxidation
4. Contact Cuts
5. Patterning Polysilicon
6. Polysilicon
7. Al contacts
8. SiO₂ by deposition

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Basic CMOS Technology

- Four dominant CMOS technologies
  - N-well process
  - P-well process
  - Twin-tub process
  - Silicon on insulator (SOI)

- N-well (P-well) process
  - Starts with a lightly doped p-type (n-type) substrate (wafer), create the n-type (p-type) well for the p-channel (n-channel) devices, and build the n-channel (p-channel) transistor in the native p-substrate (n-substrate)
N-Well CMOS Process

Cross Section of Physical Structure

Mask (top view)

p-substrate
n-well

n-well mask

nitride
oxide

active mask

Active

n-well
N-Well CMOS Process

Trench Etch

Liner Oxidation

Fill Trench

CMP for Planarization
N-Well CMOS Process

---

p-substrate

---

n-well

---

polysilicon mask

---

n+ mask

---

p-substrate

---

n-well

---

polysilicon

---

n+ mask
N-Well CMOS Process

Light implant

Heavier implant

Shadow drain implant

LDD (lightly doped drain) structure

p+ mask

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N-Well CMOS Process

p-substrate

n-well

contact mask

metal mask
CMOS Inverter in N-Well Process

![CMOS Inverter Circuit Diagram]

- **Vdd**
- **Vss**
- **in**
- **out**
CMOS Inverter in N-Well Process
A Sample of Multi-Layer Metal
Latchup

- Latchup is defined as the generation of a low-impedance path in CMOS chips between power supply rail and the ground rail due to interaction of parasitic $pnp$ and $nnp$ bipolar transistors.

- These BJTs form a silicon-controlled rectifier (SCR) with positive feedback and virtually short circuit the power rail to ground, thus causing excessive current flows and even permanent device damage.
Latchup of a CMOS Inverter

![CMOS Inverter Diagram]

- **Rsubstrate**: Resistor in the substrate
- **NPN**: NPN transistor
- **PNP**: PNP transistor
- **Vdd**: Power supply
- **N-well**: N-well region
- **P-substrate**: P-substrate region
- **Vne**: Voltage across the N-well
- **Iramp**: Current ramp
- **Trigger point**: Point where latchup occurs
- **Holding Voltage**: Voltage required to maintain latchup

Graph:
- **2.0mA**: Current level
- **Vne**: Voltage curve showing latchup behavior
- **Holding Voltage**: Voltage range where latchup is sustained
Latchup Triggering

- Latchup can be triggered by transient current or voltages that may occur internally to a chip during power-up or externally due to voltages or currents beyond normal operating ranges.
- Two possible triggering mechanisms:
  - Lateral triggering & vertical triggering
- Ex: the static trigger point of lateral triggering is

\[
I_{\text{trigger}} \approx \frac{V_{\text{pnp-on}}}{\alpha_{\text{nnp}} R_{\text{well}}}
\]
Latchup Prevention

- Reducing the value of resistors and reducing the gain of the parasitic transistors are the basis for eliminating latchup.

- Latchup can be prevented in two basic methods:
  - Latchup resistant CMOS process
  - Layout techniques

- I/O latchup prevention
  - Reducing the gain of parasitic transistors is achieved through the use of guard rings.
Guard Rings

- Guard rings are that p+ diffusions in the p-substrate and n+ diffusions in the n-well to collect injected minority carriers.
I/O Latchup Prevention

- A p+ guard ring is shown below for an n+ source/drain

- A n+ guard ring is shown below for a p+ source/drain
Antenna Rules

- When a metal wire contacted to a transistor gate is plasma-etched, it can charge up to a voltage sufficient to break down thin gate oxide
- The metal can be contacted to diffusion to provide a path for the charge to bleed away
- Antenna rules specify the maximum area of metal that can be connected to a gate without a source or drain to act as a discharge element
- The design rule normally defines the maximum ratio of metal area to gate area such that charge on the metal will not damage the gate
  - The ratios can vary from 100:1 to 5000:1 depending on the thickness of the gate oxide (and hence breakdown voltage) of the transistor in question
Antenna Rule Violation and Fix

Wire attracts charge during plasma processing and builds up voltage $V=Q/C$

Length $L_2$ exceeds allowed limit

Any source/drain can act as a discharge element

Gate may be connected to source/drain at any metal layer in an auto routing situation

Added link solves problem-$L_1$ satisfies design rule
Antenna Diode Addition

- An alternative method is to attach source/drain diodes to problem nets as shown below.
  - These diodes can be simple junctions of n-diffusion to p-substrate rather than transistor source/drain regions.

![Diagram showing antenna diode addition with label L2 and an annotation indicating where the diode may be added.](image)
Layer Density Rules

- For advanced processes, a minimum and maximum density of a particular layer within a specific area should be specified
  - Layer density rules

- Layer density rules are required as a result of the CMP process and the desire to achieve uniform etch rates

- For example, a metal layer might have to have 30% minimum and 70% maximum fill within a 1mm by 1mm area

- For digital circuits, layer density levels are normally reached with normal routing

- Analog & RF circuits are almost sparse
  - Gate and metal layers may have to be added manually or by a fill program after design has been completed
CMOS Process Enhancements

- **Multiple threshold voltages**
  - Low-\(V_t\) → more on current, but greater subthreshold leakage
  - High-\(V_t\) → less current, but smaller subthreshold leakage
  - User low-\(V_t\) devices on critical paths and higher-\(V_t\) devices elsewhere to limit leakage power
  - Multiple masks and implantation steps are used to set the various thresholds

- **Silicon on insulator (SOI) process**
  - The transistors are fabricated on an insulator
  - Two major insulators are used, SiOs and sapphire
  - Two major advantages: elimination of the capacitance between the source/drain regions and body, leading to higher-speed devices; lower subthreshold leakage
CMOS Process Enhancements

- High-k gate dielectrics
  - MOS needs high gate capacitance to attract charge to channel → very thin SiO₂ gate dielectrics
  - Scaling trends indicate the gate leakage will be unacceptably large in such thin gates
  - Gates could use thicker dielectrics and hence leak less if a material with a higher dielectric constant were available
High-K and Metal Gate MOSFET

>45nm

Poly-Si/SiO₂

1. \( t_{ox} \) is downscaling with the technology downscaling
2. \( t_{ox} \) → gate leakage ↑

\( t_{ox} \) is downscaling with the technology downscaling

gate leakage ↑

\( t_{ox} \) → gate leakage ↑

<=45nm

Metal/High-k

1. Additional poly-depletion capacitor
2. Reaction with high-k dielectric
3. High gate resistance

Poly-depletion capacitor → Poly-Si

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Summary

☐ Some of more common CMOS technologies have been covered

☐ A representative set of n-well process has been introduced

☐ The important condition known as latchup has been introduced with necessary design rules to avoid this condition in CMOS chips

☐ Antenna rules & layer density rules should be considered in modern manufacturing process