1. **Shannon’s Expansion Theorem** (4 points)

Consider a Boolean function \( f(x_1, x_2, \ldots, x_i, \ldots, x_n) \) with \( n \) variables. According to Shannon’s Expansion Theorem, we can expand the Boolean function in terms of any one of its variables \( x_i \). That is,

\[
f(x_1, x_2, \ldots, x_i, \ldots, x_n) = x_i f(x_1, x_2, \ldots, 1, \ldots, x_n) + \overline{x_i} f(x_1, x_2, \ldots, 0, \ldots, x_n).
\]

On the other hand, consider a two-input multiplexer with with the output \( f \) and the inputs \( g_1 \) and \( g_2 \) and the control signal \( x_i \). Assume that \( f = g_1 \) when \( x_i = 1 \) and \( f = g_2 \) when \( x_i = 0 \). Then, the Boolean function of the multiplexer can be expressed as \( f = x_i g_1 + \overline{x_i} g_2 \).

Complete the following questions:

(a) Realize the Boolean function \( f(x_1, x_2, x_3, x_4) = x_1 x_2 + x_3 x_4 \) using two-input multiplexers. (2 points)

(b) Can any Boolean functions be realized by two-input multiplexers? Please explain your answer. (2 points)

2. **CMOS Logic Design** (4 points)

Consider the logic diagram given in Figure 1.

![Figure 1: A combinational circuit](image)

(a) Design a CMOS circuit for implementing \( F \). (2 points)

(b) Assume that all the NMOS and PMOS transistors for realizing the \( F \) have the same size \( W/L \) and the gate capacitance of an NMOS or a PMOS transistor is 2pf. Also, the drain capacitance of the transistor and the parasitic capacitance of the wire can be ignored. Calculate the value of capacitance of the nodes \( x \) and \( y \). (2 points)

3. **MOS Theory** (2 points)

Fig. 2 shows a CMOS inverter. Assume that the body effect can be neglected. Identify the transistor(s) which cannot operate in the saturation region. Explain your answer.

![Figure 2: A CMOS inverter](image)