EE6013 VLSI Design

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Syllabus

- Contents
  - Introduction to CMOS Circuits
  - MOS Transistor Theory
  - Fabrication of CMOS Integrated Circuits
  - Electrical Characteristics of CMOS Circuits
  - Elements of Physical Design
  - Combinational Circuit Design
  - Sequential Circuit Design
  - Datapath Design
  - Low-Power Design in VLSI Chips
  - Memory Design

Syllabus

- Text Book
  - N. H. E. Weste and D. Harris, "*CMOS VLSI Design, a Circuits and Systems Perspective*", Third Edition. Addison Wesley, 2005.
- Reference Book
  - S.-M. Kang and Y. Leblebici,"CMOS Digital Integrated Circuits", McGRAW-HILL, 2003.
- Grading
  - Homework 30%
  - Midterm 25%
  - Final 25%
  - Project 20%
  - Overdue homework is not accepted!
- Prerequisite
  - Digital logic design, Microelectronics
- Key dates
  - Midterm 1: 13:00-15:00, Tuesday, Nov. 13, E1-118
  - Midterm 2: 13:00-15:00, Tuesday, Dec. 25, E1-118
  - Final project presentation: Jan. 8 (E1-118) and 9 (E1-110)
  - Final project report: before 17:00, Jan. 11, E1-402

Syllabus

- Teaching assistants
- Course Website: http://www.ee.ncu.edu.tw/~jfli/

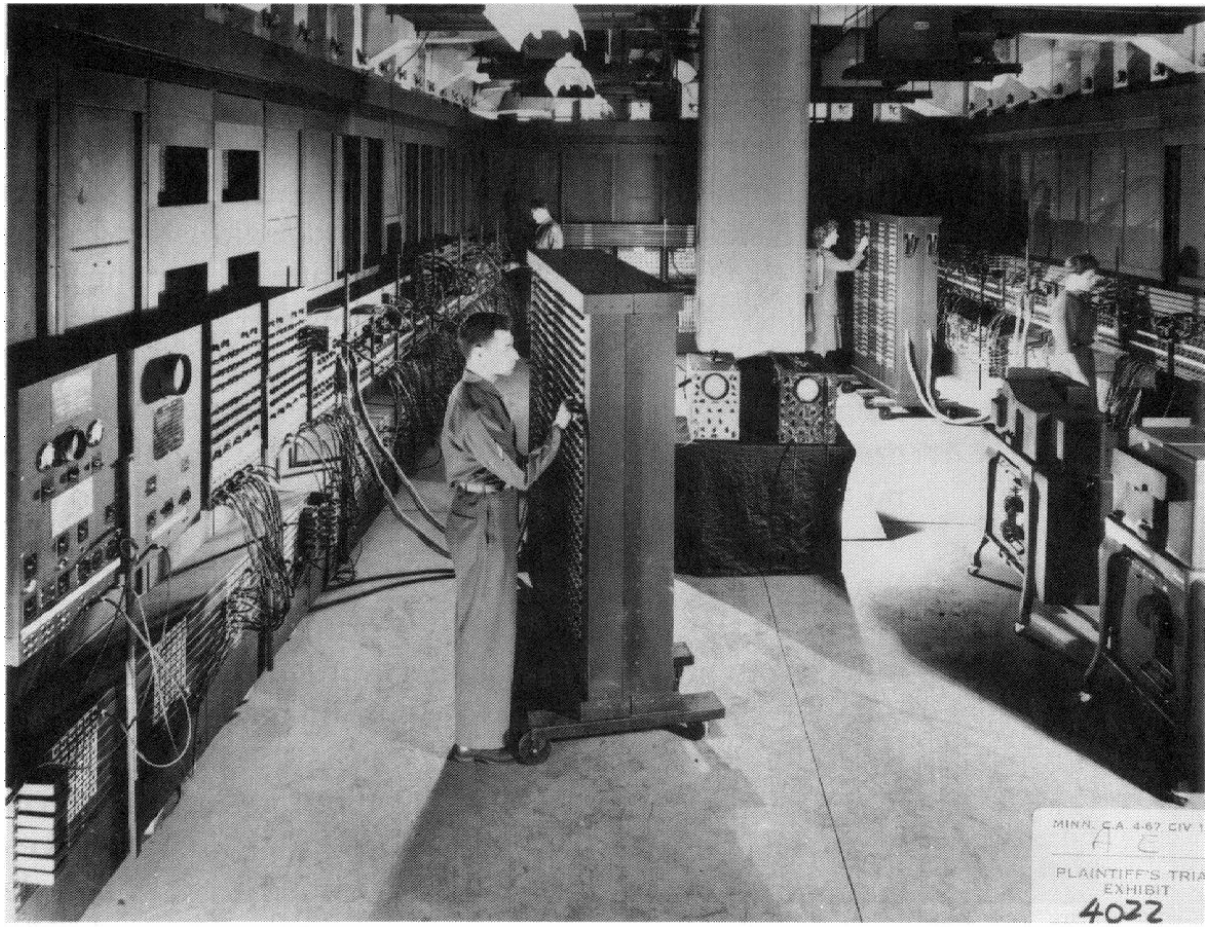
Lecture Schedule

Date	Note
Week 1 (9/11, 9/12)	
Week 2 (9/18, 9/19)	
Week 3 (9/26)	No class on 9/24
Week 4 (10/2, 10/3)	
Week 5 (10/9)	Hspice Tutorial (Assistants); ATS 2007, Beijin, China
Week 6 (10/16, 10/17)	
Week 7 (10/23, 10/24)	
Week 8 (10/30, 10/31)	
Week 9 (11/6, 11/7)	
Week 10 (11/13, 11/14)	11/13: Midterm1
Week 11 (11/20)	No class on 11/21 (運動會)
Week 12 (11/27, 11/28)	
Week 13 (12/4, 12/5)	
Week 14 (12/11, 12/12)	
Week 15 (12/18, 12/19)	
Week 16 (12/25, 12/26)	12/25: Midterm 2
Week 17 (1/2)	
Week 18 (1/8, 1/9)	Project Presentation

What is This Course all About?

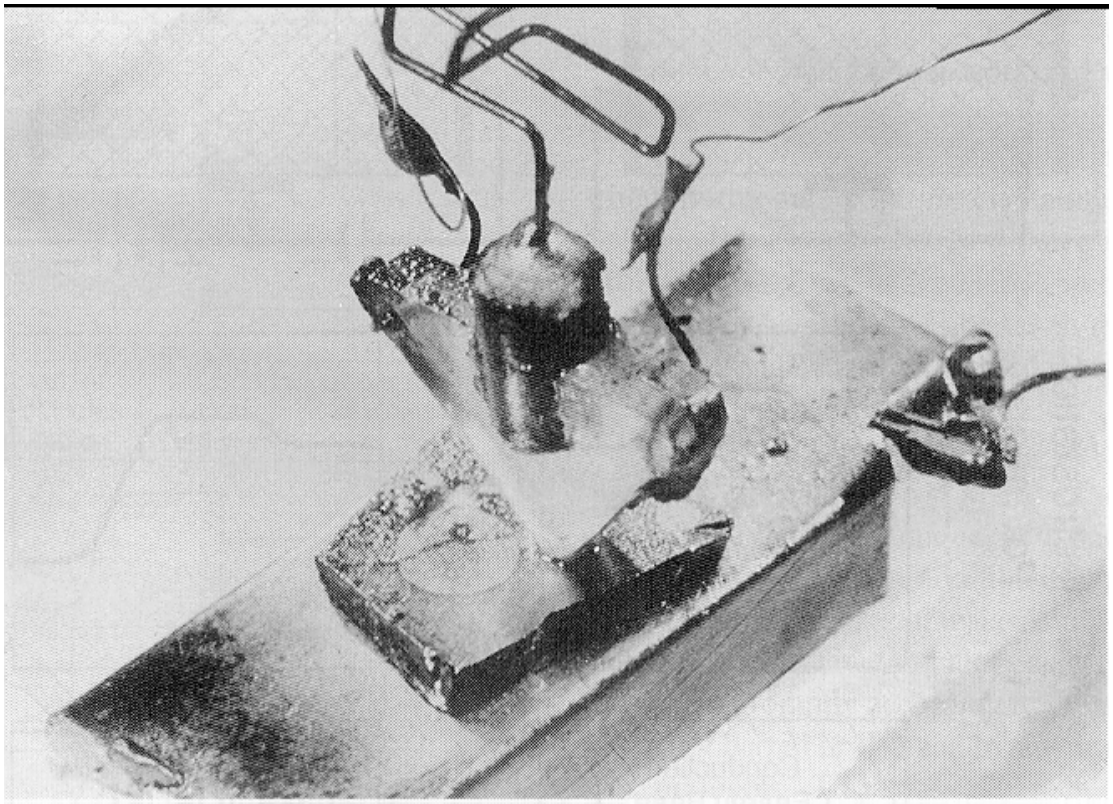
- **Scopes of VLSI design**
  - Digital circuits
  - Analog circuits
  - Mixed-signal circuits
  - Memory circuits
- **This course will cover the following contents**
  - CMOS devices and manufacturing technology; CMOS inverters and gates; propagation delay; noise margins; CMOS power dissipation; sequential circuits; arithmetic circuits; interconnect; memories; and low-power design techniques.
- **What will you learn?**
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: area, speed, and power dissipation

ENIAC - The first electronic computer (1946)



Source: J. Rabaey, 2004

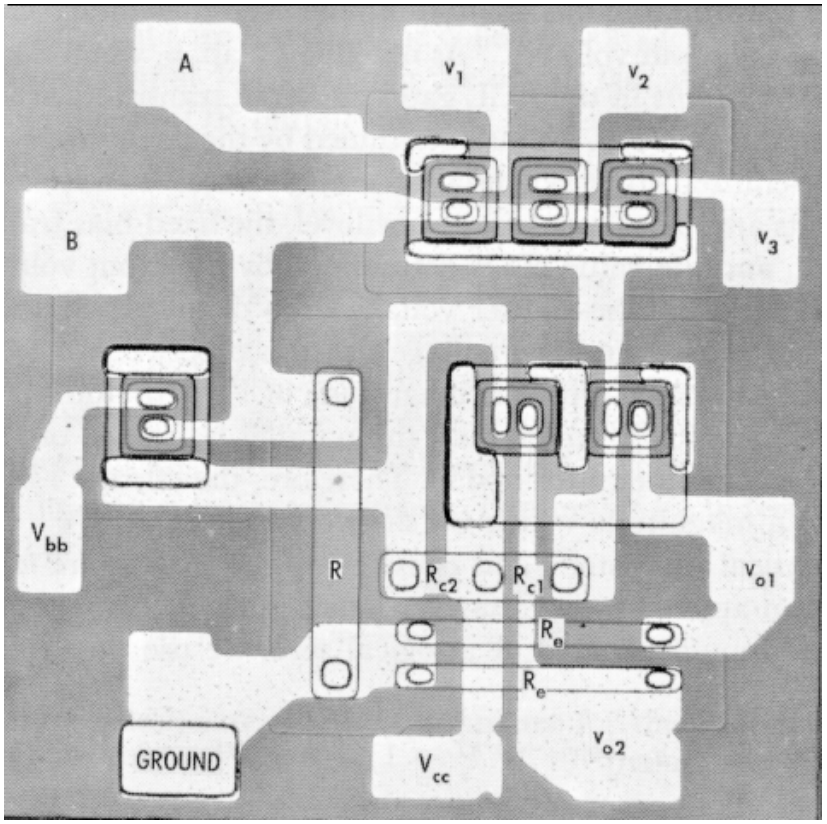
The Transistor Revolution



First transistor (Bell Labs, 1948)

Source: J. Rabaey, 2004

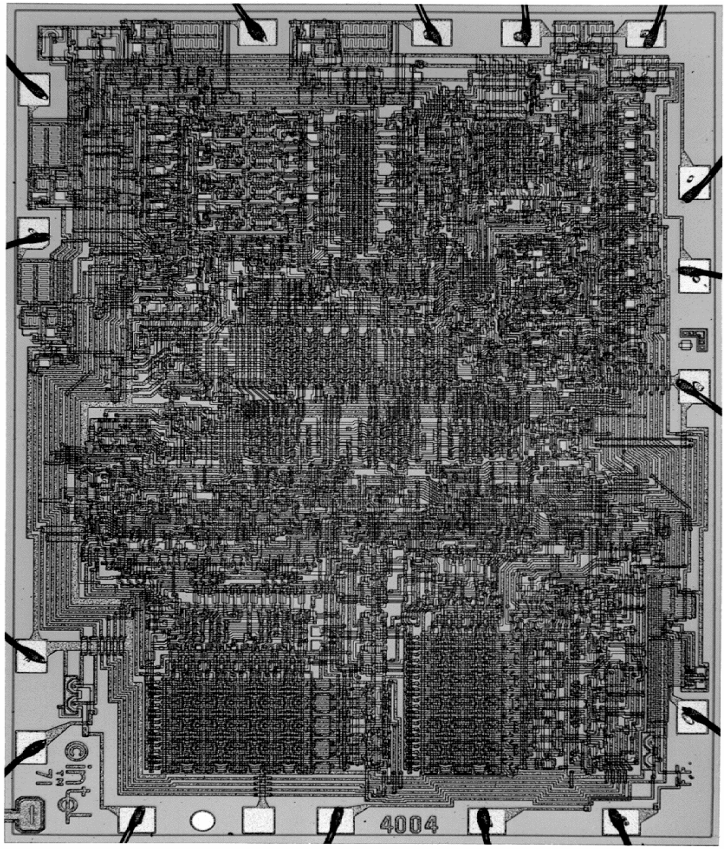
The First Integrated Circuits



ECL 3-input Gate (bipolar logic), Motorola 1966

Source: J. Rabaey, 2004

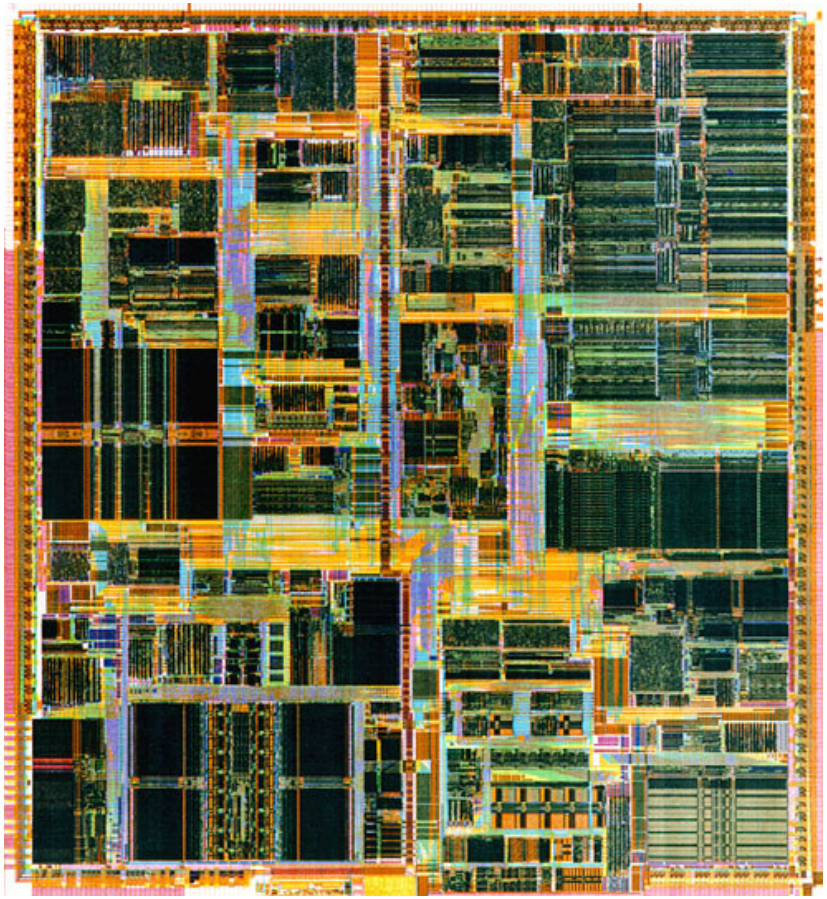
Intel 4004 Microprocessor



1000 transistors,1 MHz operation, 1971

Source: J. Rabaey, 2004

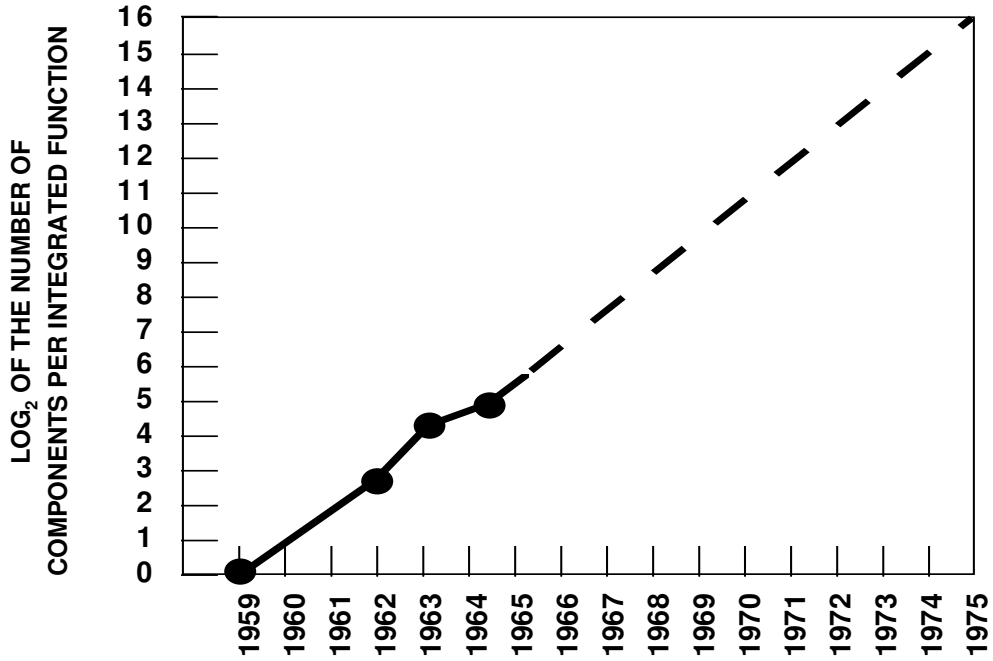
Intel Pentium (IV) microprocessor



Source: J. Rabaey, 2004

Moore's Law

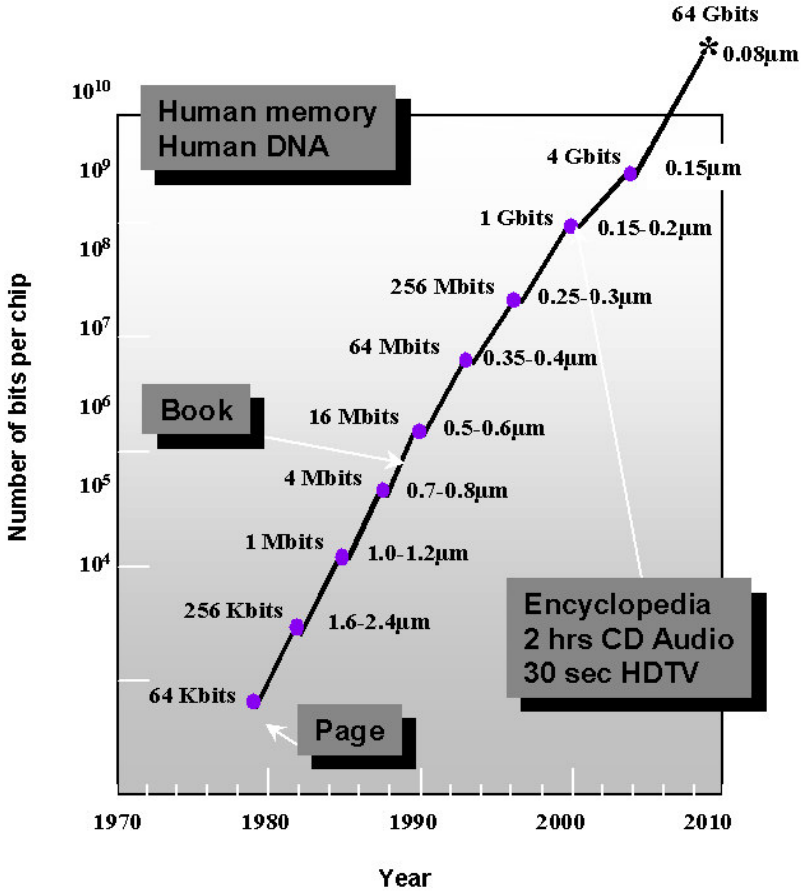
In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months. He made a prediction that semiconductor technology will double its effectiveness every 18 months



Source: J. Rabaey, 2004

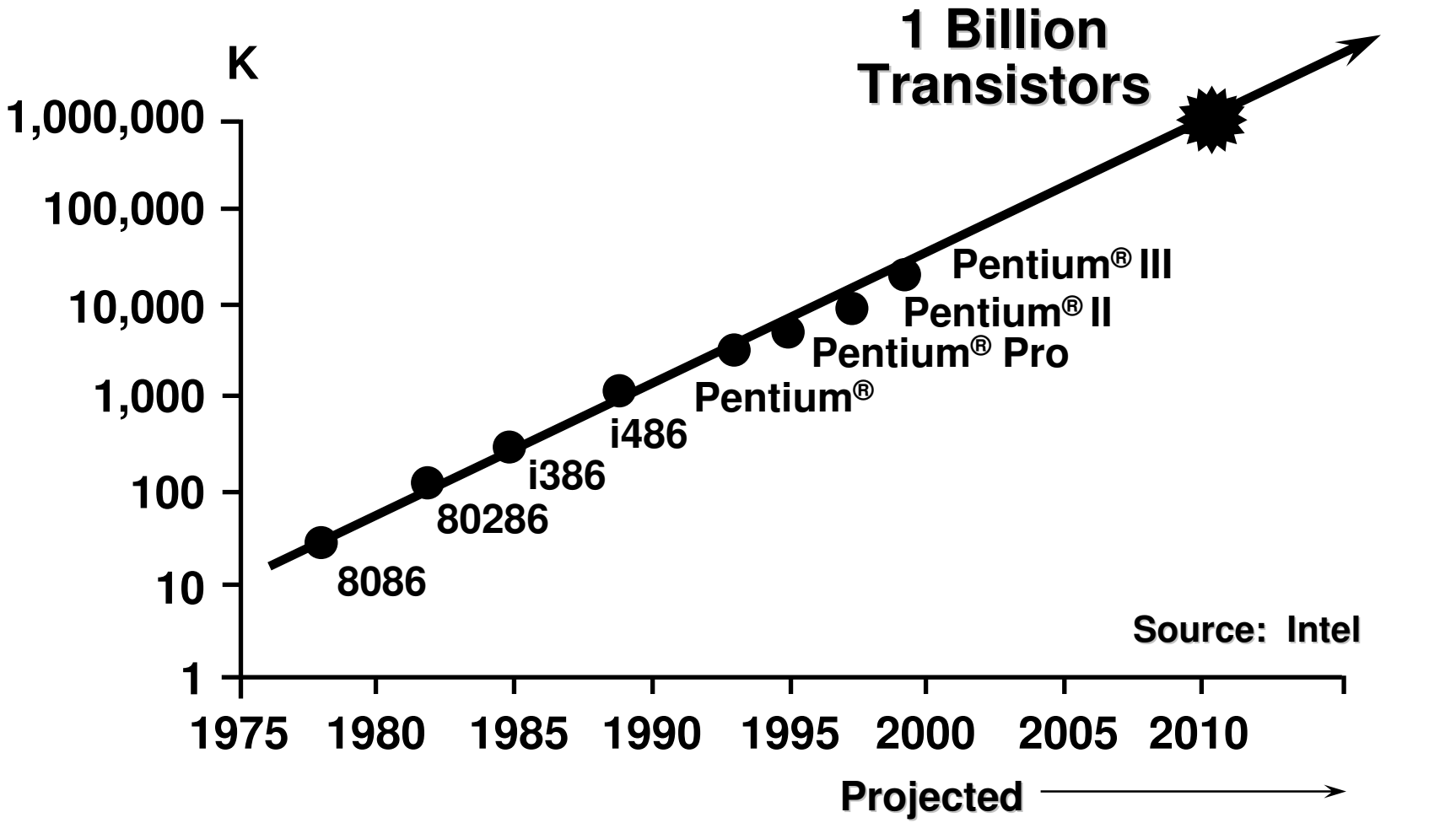
Electronics, April 19, 1965.

Evolution in Complexity



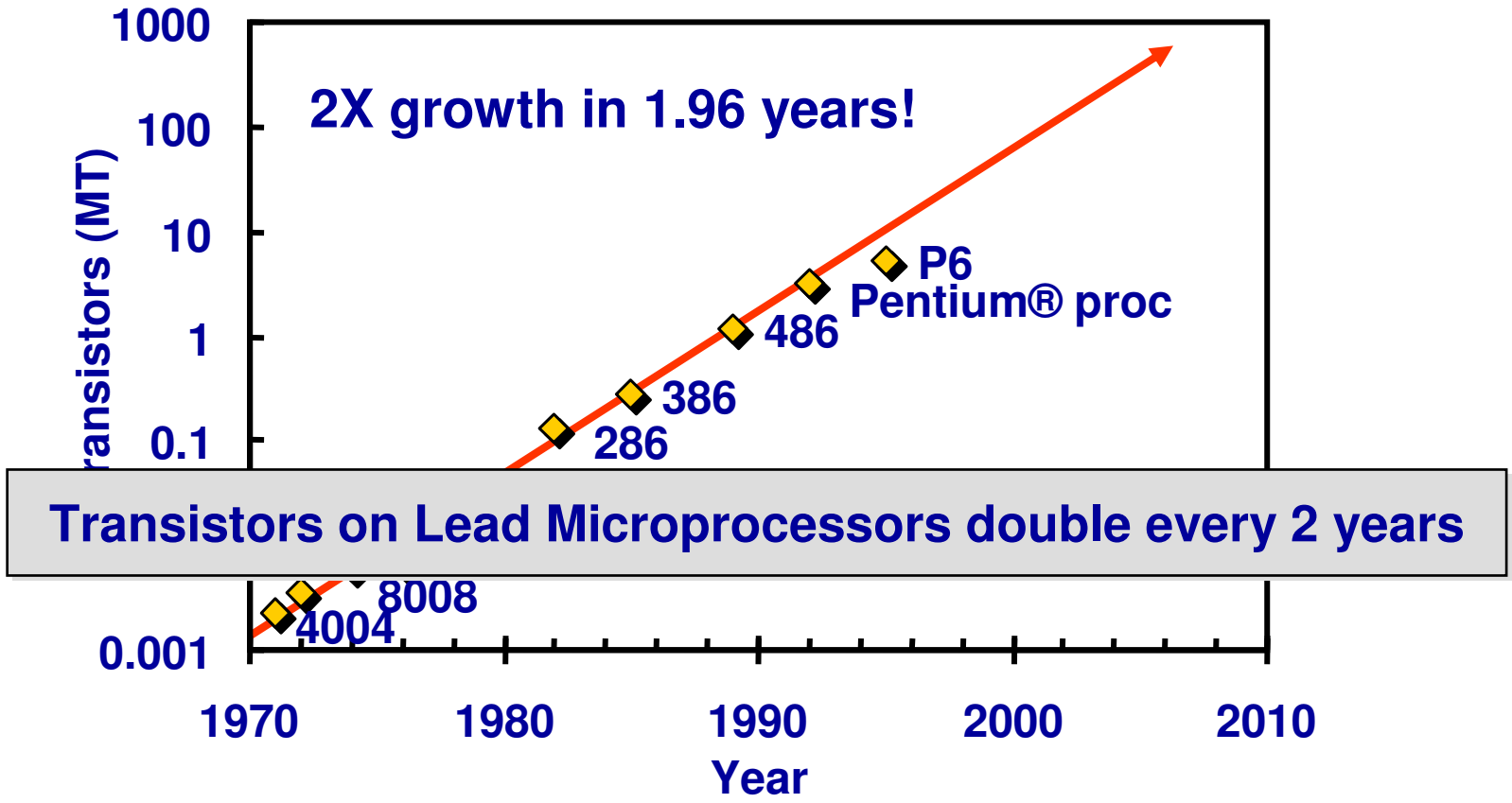
Source: J. Rabaey, 2004

Transistor Counts



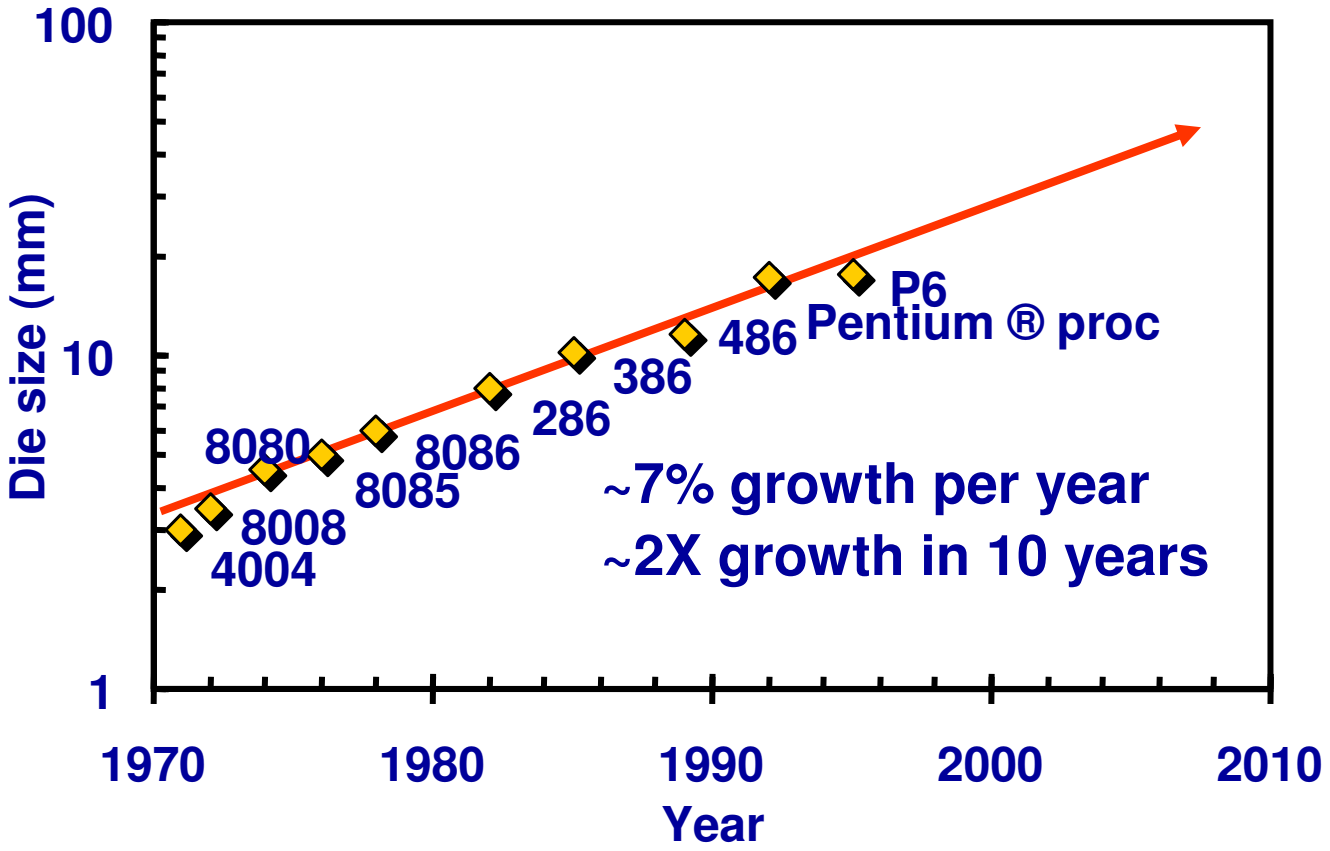
Source: J. Rabaey, 2004

Moore's law in Microprocessors



Source: J. Rabaey, 2004

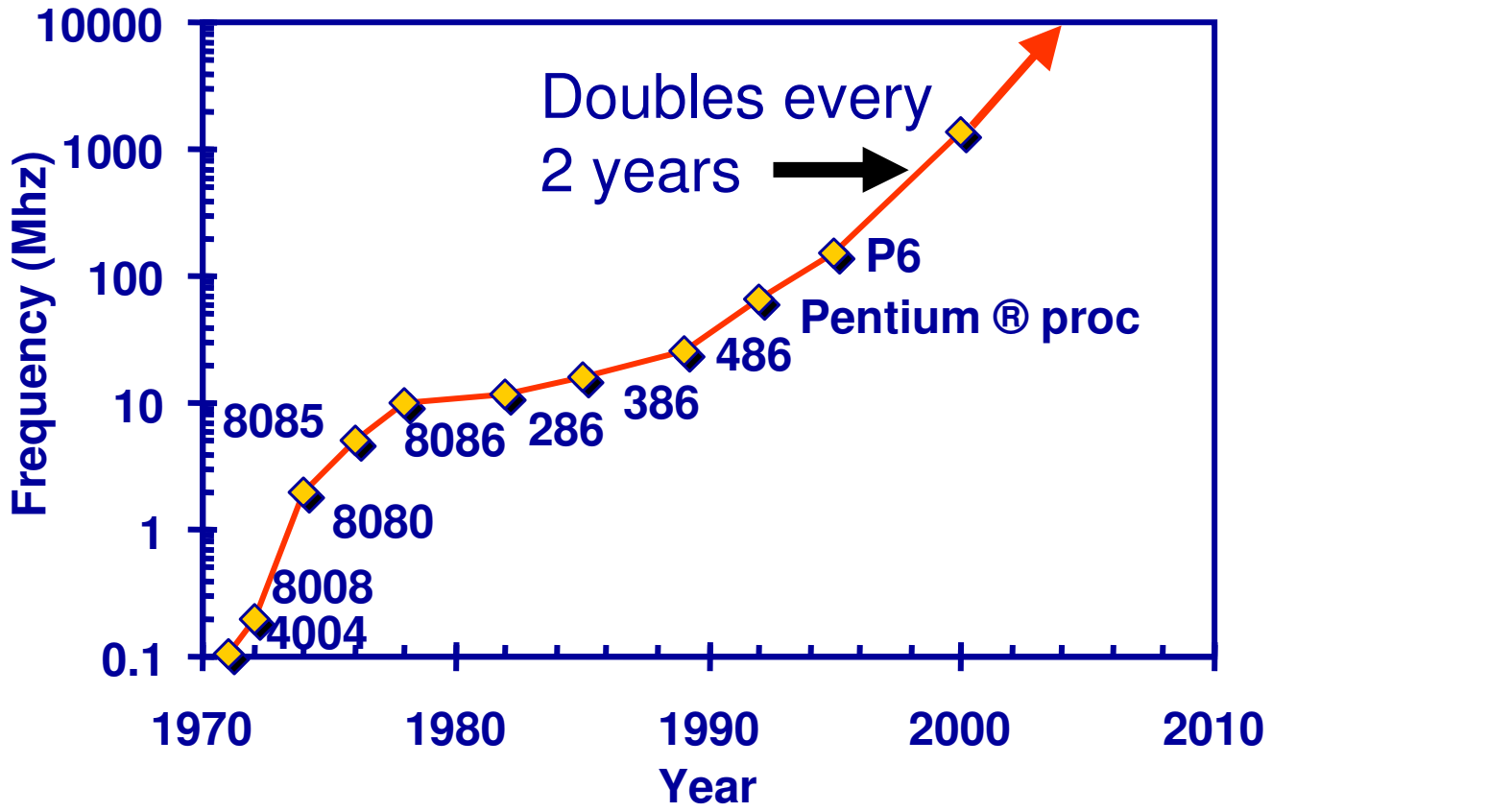
Die Size Growth



Die size grows by 14% to satisfy Moore's Law

Source: J. Rabaey, 2004

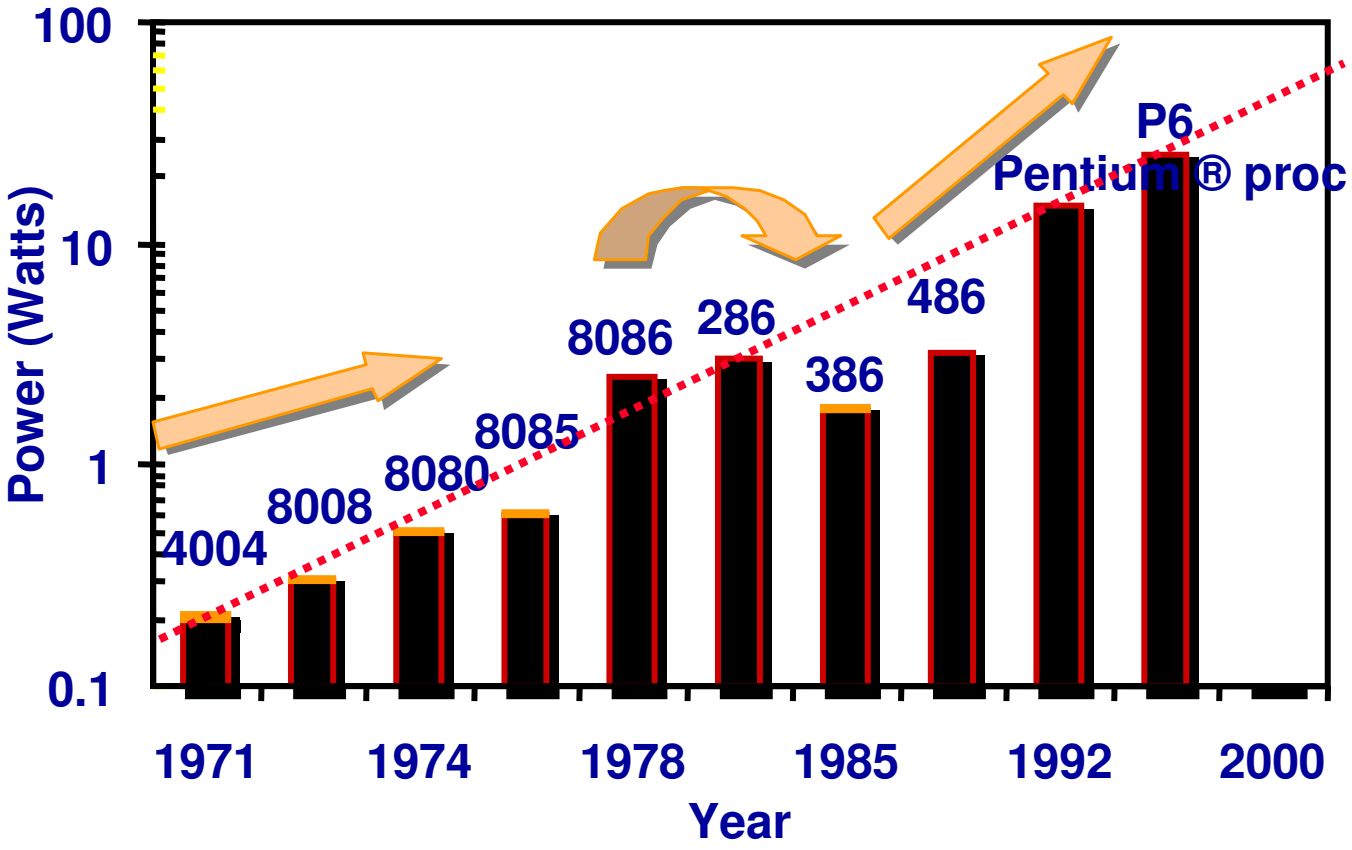
Frequency



Lead Microprocessors frequency doubles every 2 years

Source: J. Rabaey, 2004

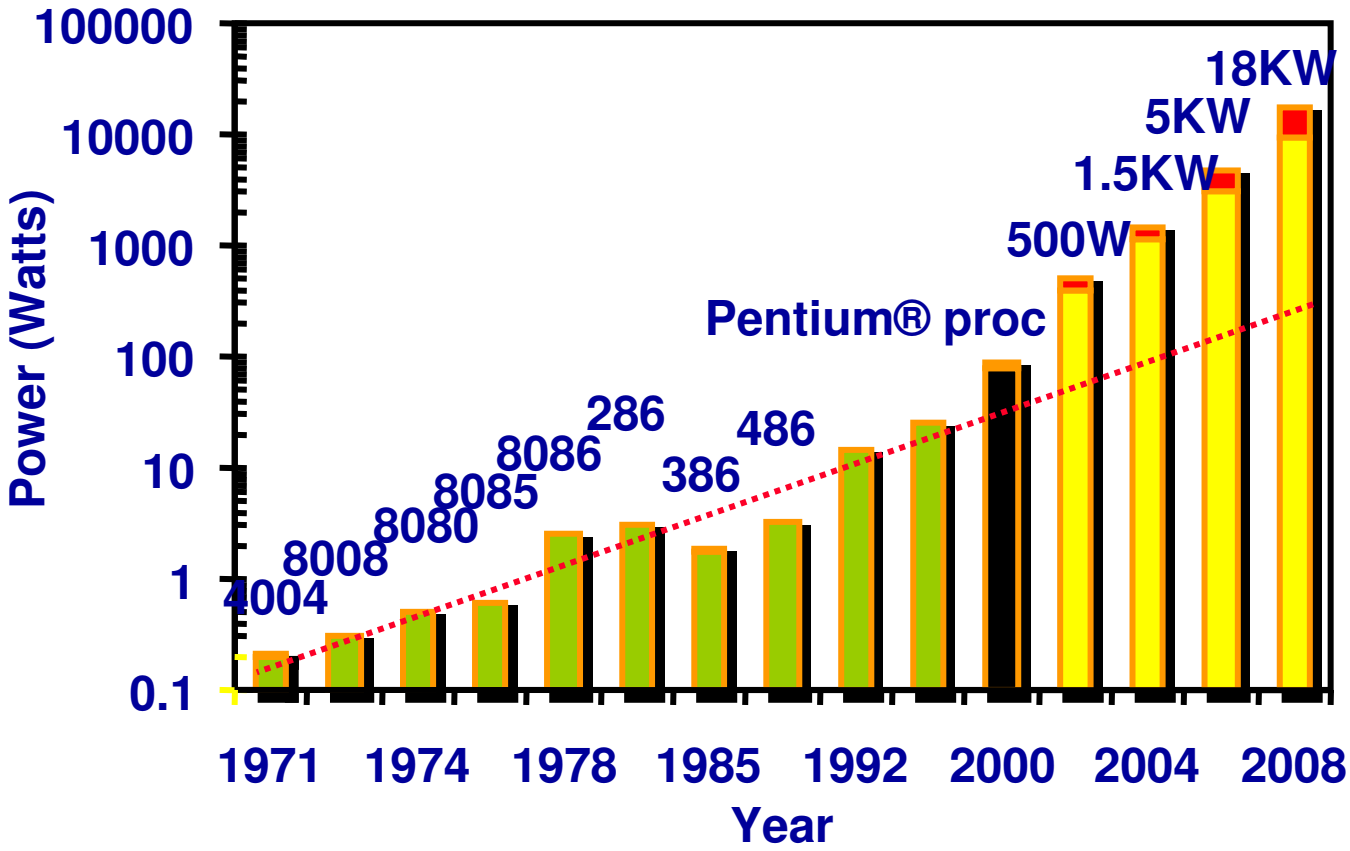
Power Dissipation



Lead Microprocessors power continues to increase

Source: J. Rabaey, 2004

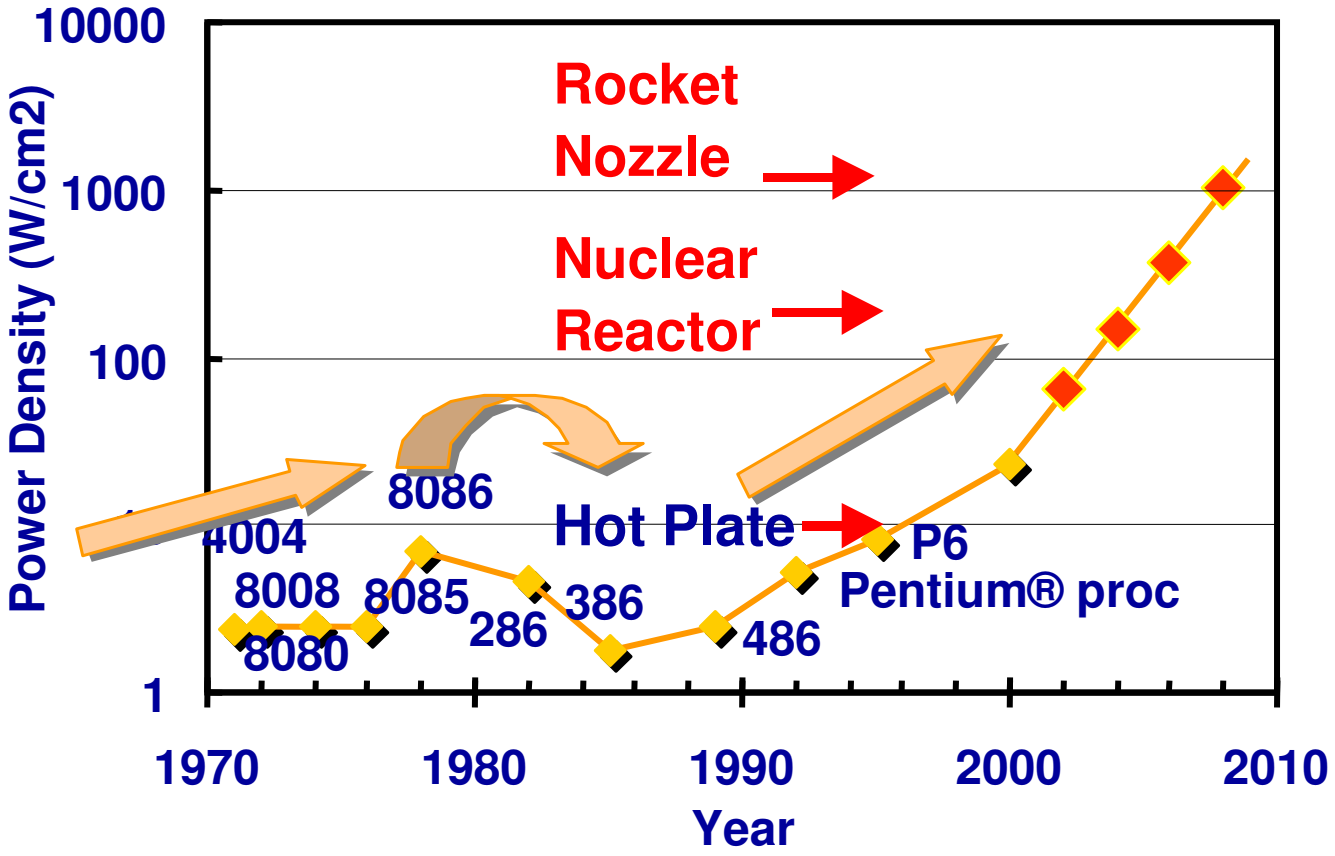
Power Will Be a Major Problem



Power delivery and dissipation will be prohibitive

Source: J. Rabaey, 2004

Power Density

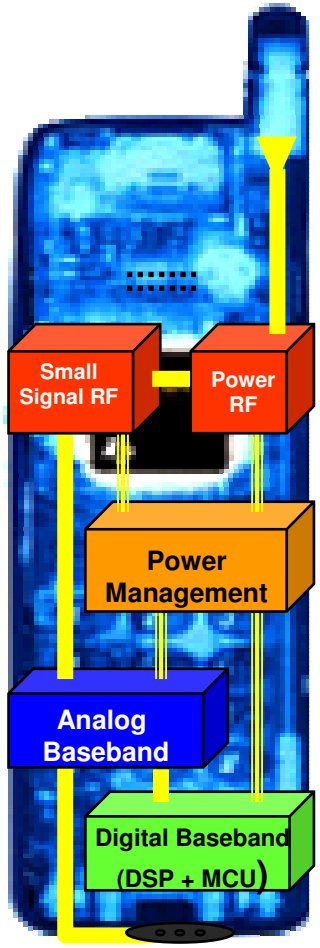


Power density too high to keep junctions at low temp

Source: J. Rabaey, 2004

Not Only Microprocessors

Cell Phone



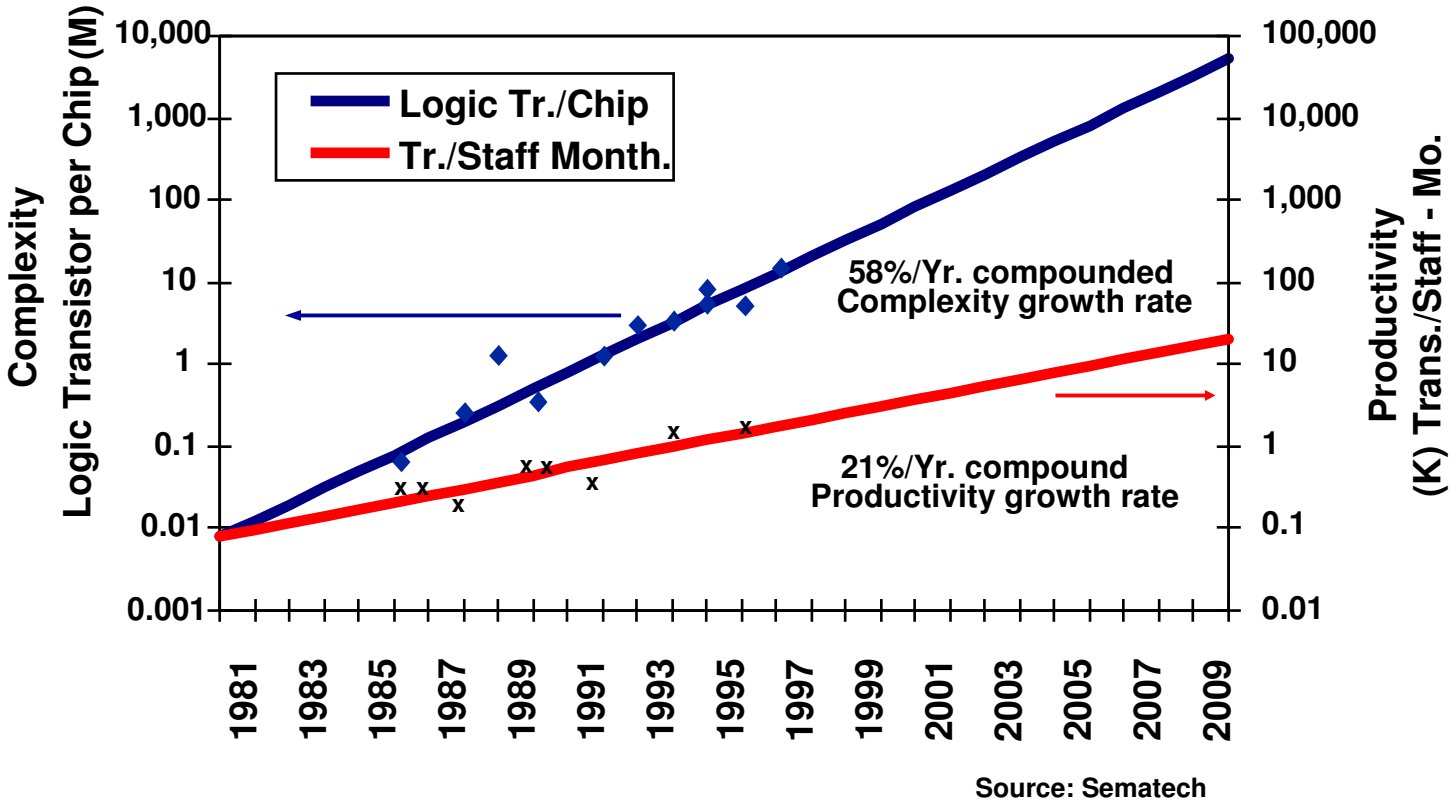
Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)

Source: J. Rabaey, 2004

Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

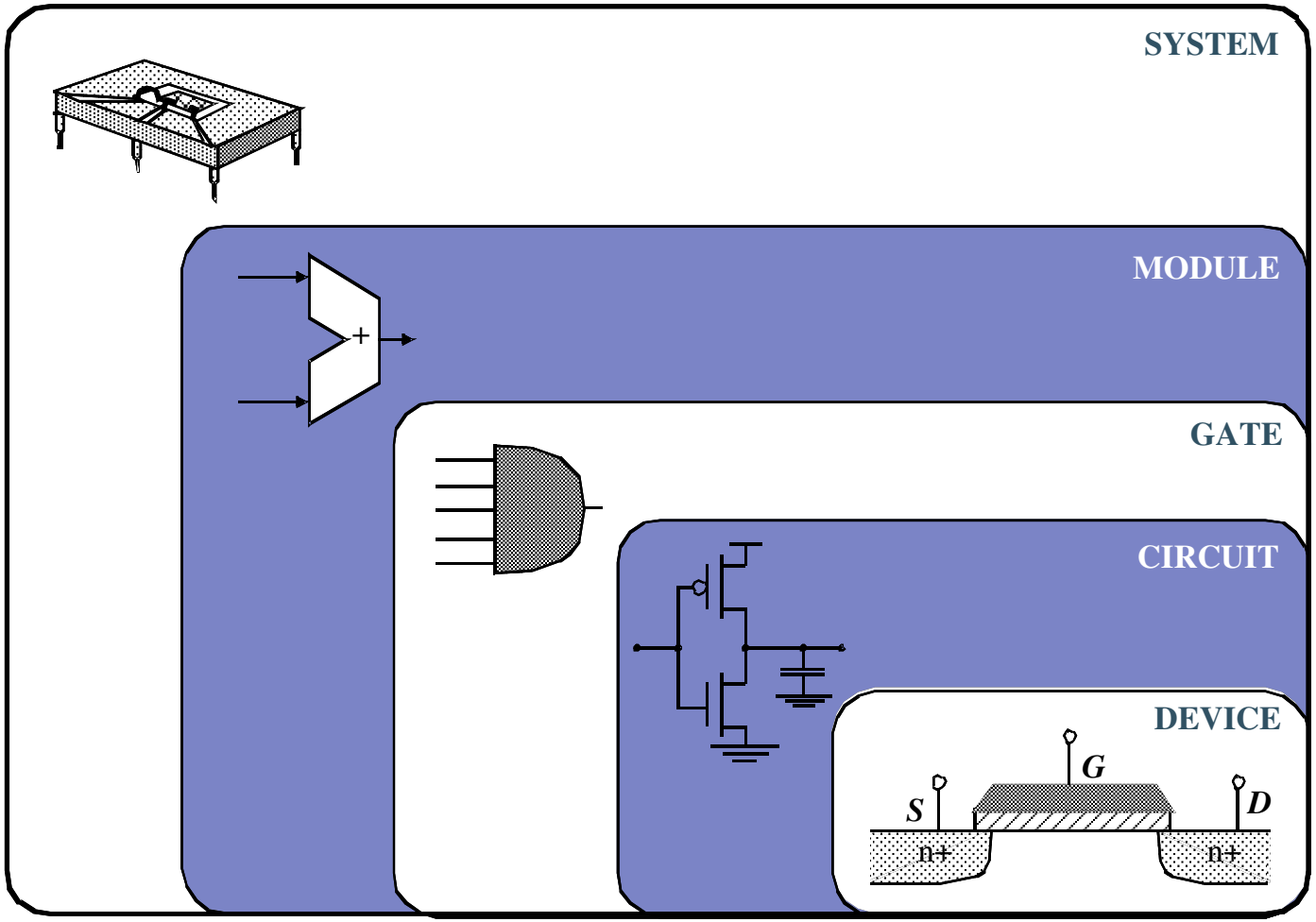
Source: J. Rabaey, 2004

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Source: J. Rabaey, 2004

Design Abstraction Levels



Source: J. Rabaey, 2004

Design Metrics

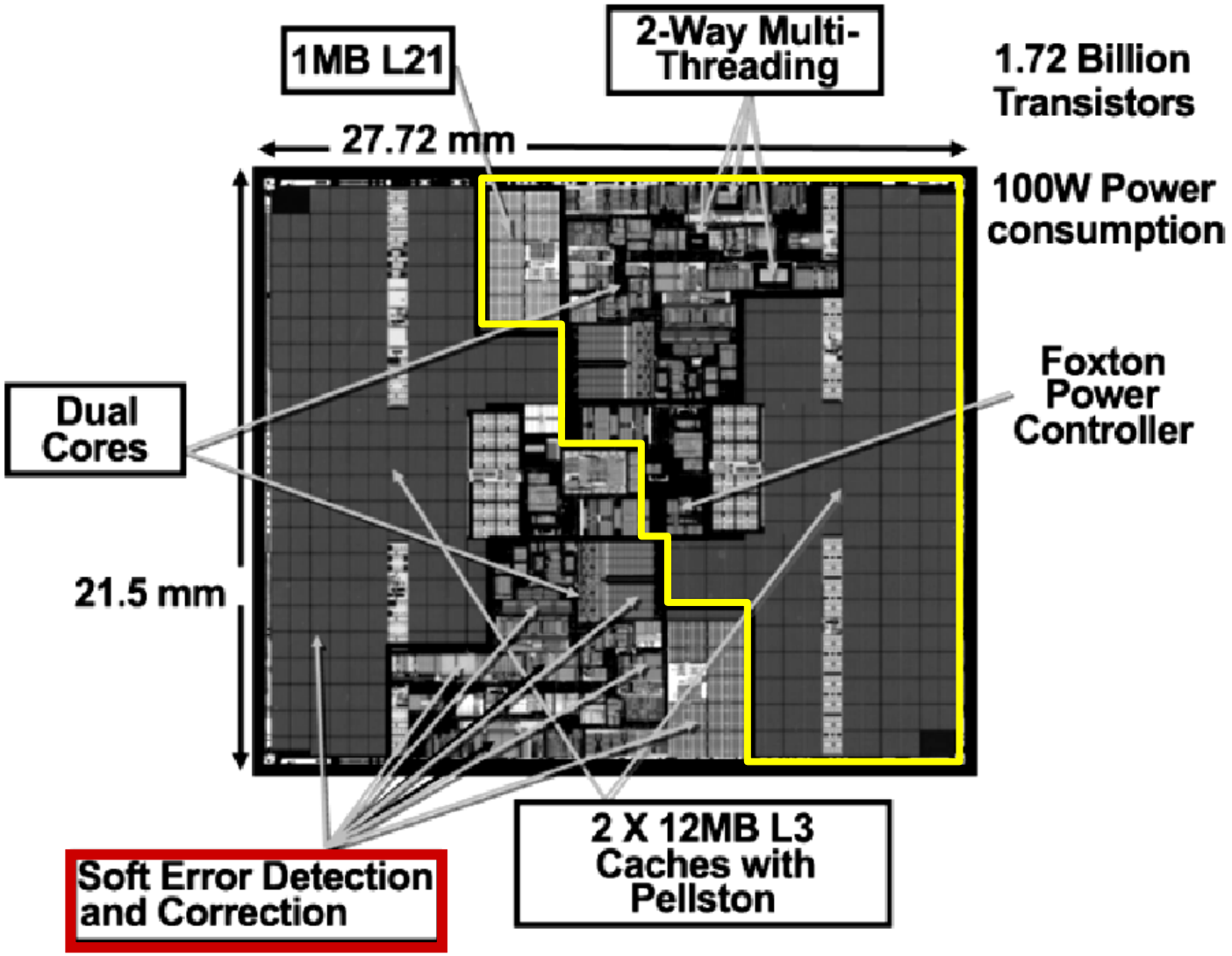
- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

Source: J. Rabaey, 2004

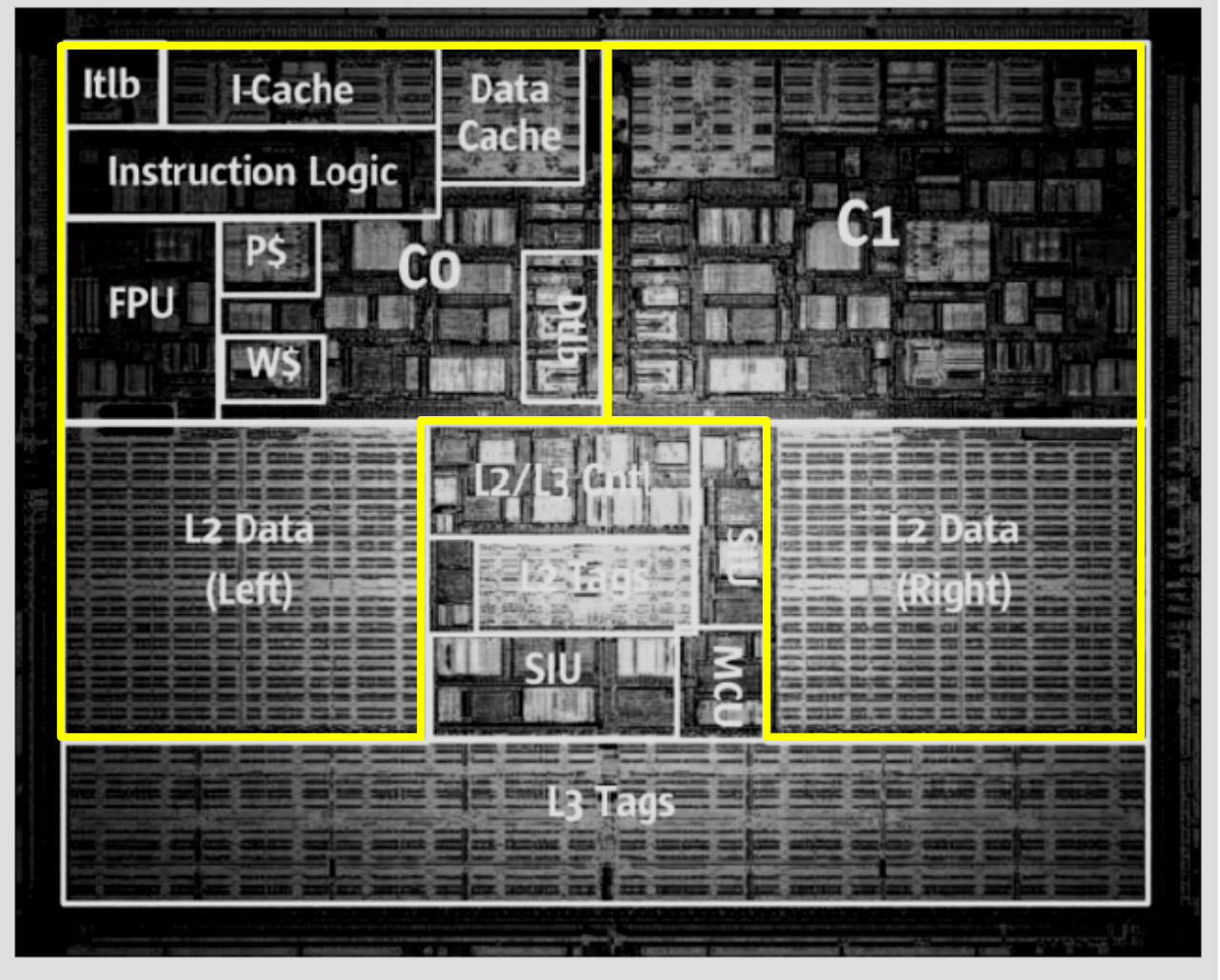
One New Trend on Complex VLSI Designs

- Regular structures with network-connected communication mechanism
  - Multicore processor chips
  - Network-on-chips
- Multicore processor chips can cope with the following challenges in nano-scale technology
  - High power
  - Low reliability
  - Low yield
- Network-on-chips can cope with the following challenge in nano-scale technology
  - Long interconnection delay

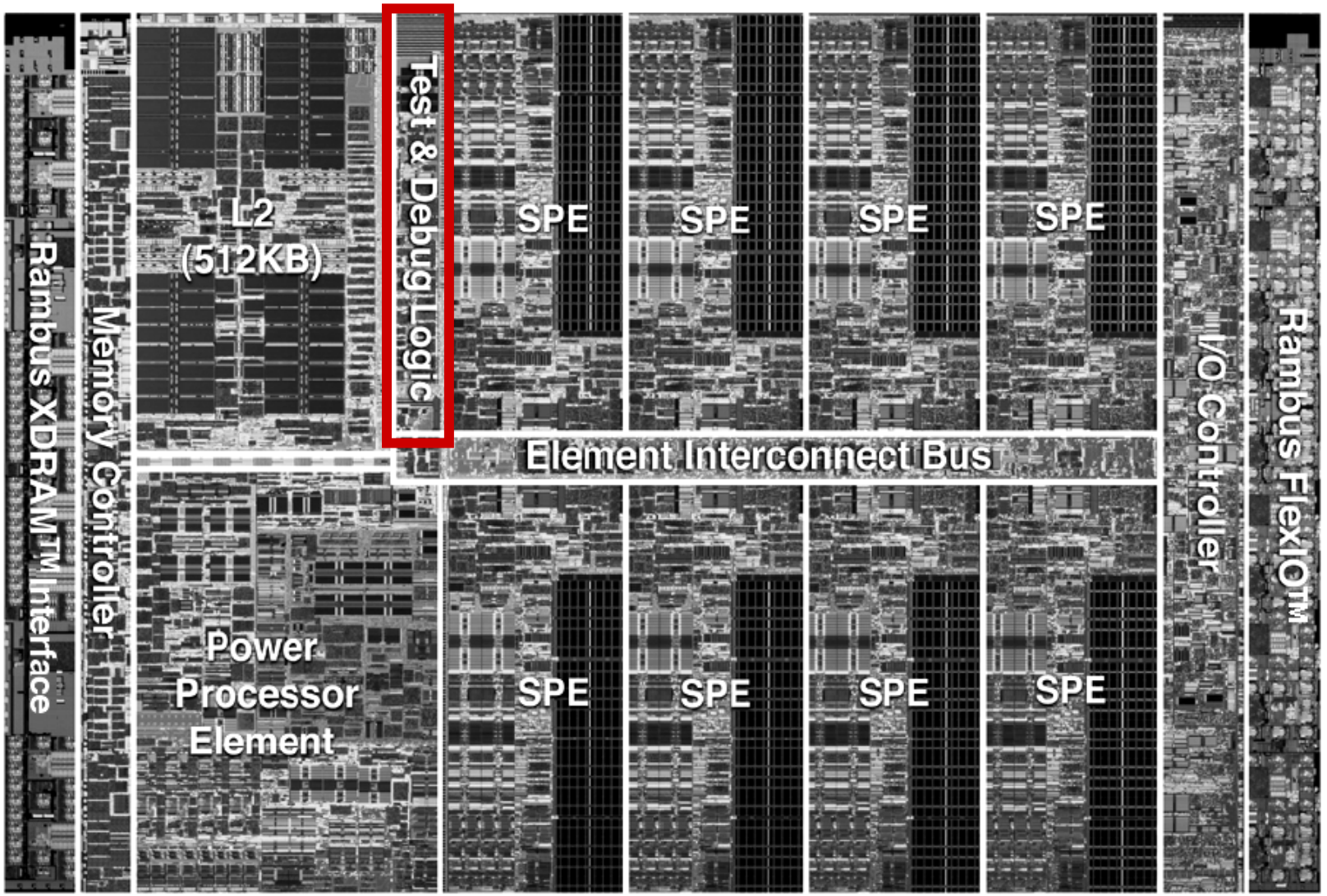
Itanium (JSSC, Jan. 2006)



SPARC V9 (JSSC, Jan. 2006)



Cell Processor (JSSC, Jan. 2006)



Example of an Network-on-Chip