Chapter 3
Fabrication of CMOS Integrated Circuits

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Outline

- Background
- The CMOS Process Flow
- Design Rules
- Latchup
- Antenna Rules & Layer Density Rules
- CMOS Process Enhancements
- Summary

Introduction

- An integrated circuit is created by stacking layers of various materials in a pre-specified sequence
- Both the electrical properties of the material and the geometrical patterns of the layer are important in establishing the characteristics of devices and networks
- Most layers are created first, and then patterned using lithographic sequence
- Doped silicon layers are the exception to this rule

Material Growth and Deposition

- Silicon Dioxide (SiO_2)
  - It is an excellent electrical insulator
  - It can be grown on a silicon wafer or deposited on top of the wafer
  - Thermal oxide
    - $Si+O_2 \rightarrow SiO_2$ (dry oxidation), using heat as a catalyst
      - Growth rate is lower
    - $Si+2H_2O \rightarrow SiO_2+2H_2$ (wet oxidation)
      - Growth rate is faster
    - The surface of the silicon is recessed from its original location
  - CVD oxide
    - $SiH_4(gas)+2O_2(gas) \rightarrow SiO_2(solid)+2H_2O(gas)$
    - Chemical vapor deposition (CVD)

Material Growth and Deposition

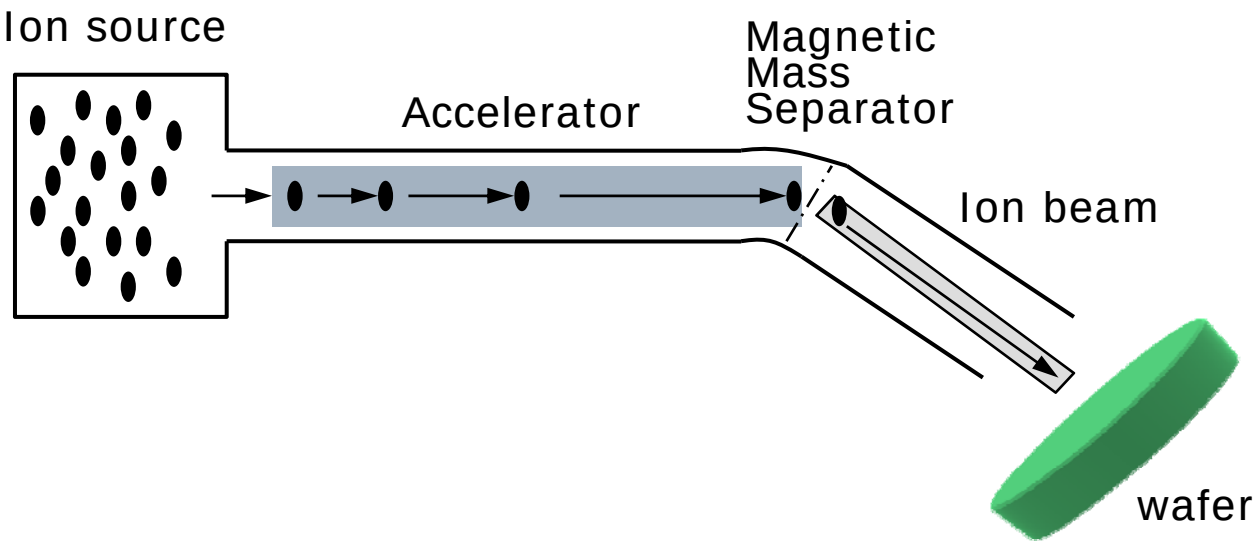
- Silicon Nitride (Si_3N_4)
  - A.k.a. nitride
  - $3SiH_4(gas)+4NH_3(gas) \rightarrow Si_3N_4(solid)+12H_2(gas)$
  - Nitrides act as strong barriers to most atoms, this makes them ideal for use as an overglass layer
- Polycrystal Silicon
  - Called polysilicon or just poly for short
  - It is used as the gate material in MOSFETs
  - $SiH_4 \rightarrow Si+2H_2$
  - It adheres well to silicon dioxide

Material Growth and Deposition

- Metals
  - Aluminum (Al) is the most common metal used for interconnect wiring in ICs
    - It is prone to electromigration
    - J=I/A; A=wt is the cross-section area
    - Layout engineers cannot alter the thickness t of the layer
    - Electromigration is thus controlled by specifying the minimum width w to keep J below a max. value
  - Copper (Cu) has recently been introduced as a replacement to aluminum
    - Its resistivity is about one-half the value of Al
    - Standard patterning techniques cannot be used on copper layers; specialized techniques had to be developed

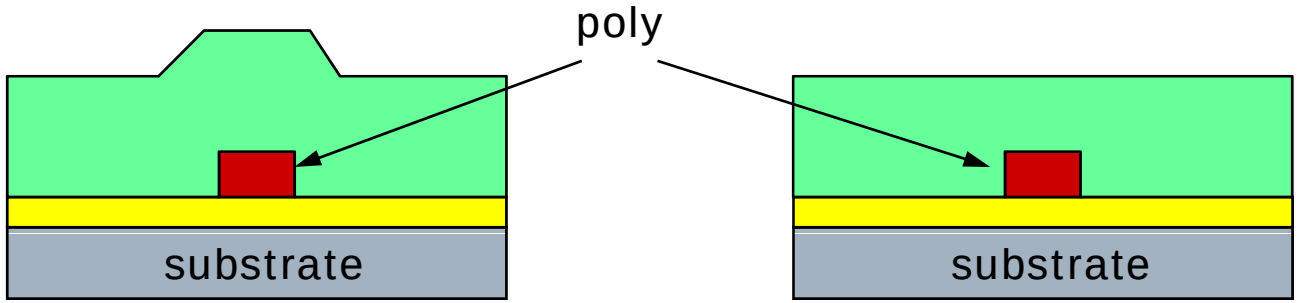
Material Growth and Deposition

- Doped Silicon Layers
  - Silicon wafer is the starting point of the CMOS fabrication process
  - A doped silicon layer is a patterned n- or p-type section of the wafer surface
  - This is accomplished by a technique called ion implantation
- Basic section of an ion implanter



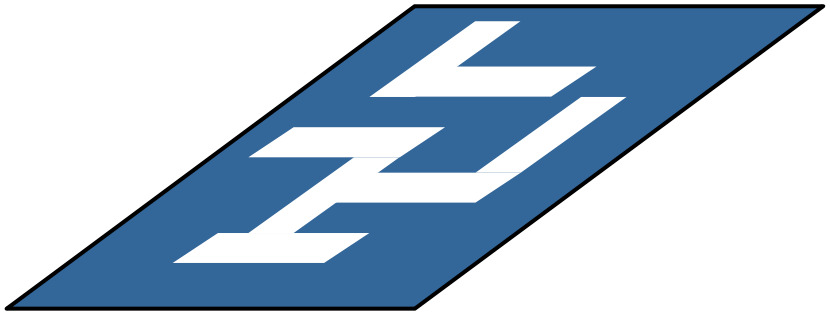
Material Growth and Deposition

- The process of deposition causes that the top surface has hillocks
  - If we continue to add layers (e.g., metal layers), the surface will get increasing rough and may lead to breaks in fine line features and other problems
  - Surface planarization is required
- Chemical-Mechanical Polishing (CMP)
  - It uses a combination of chemical etching and mechanical sanding to produce planar surfaces on silicon wafers
- Surface planarization



Lithography

- One of the most critical problems in CMOS fabrication is the technique used to create a pattern
  - Photolithography
- The photolithographic process starts with the desired pattern definition for the layer
- A mask is a piece of glass that has the pattern defined using a metal such as chromium

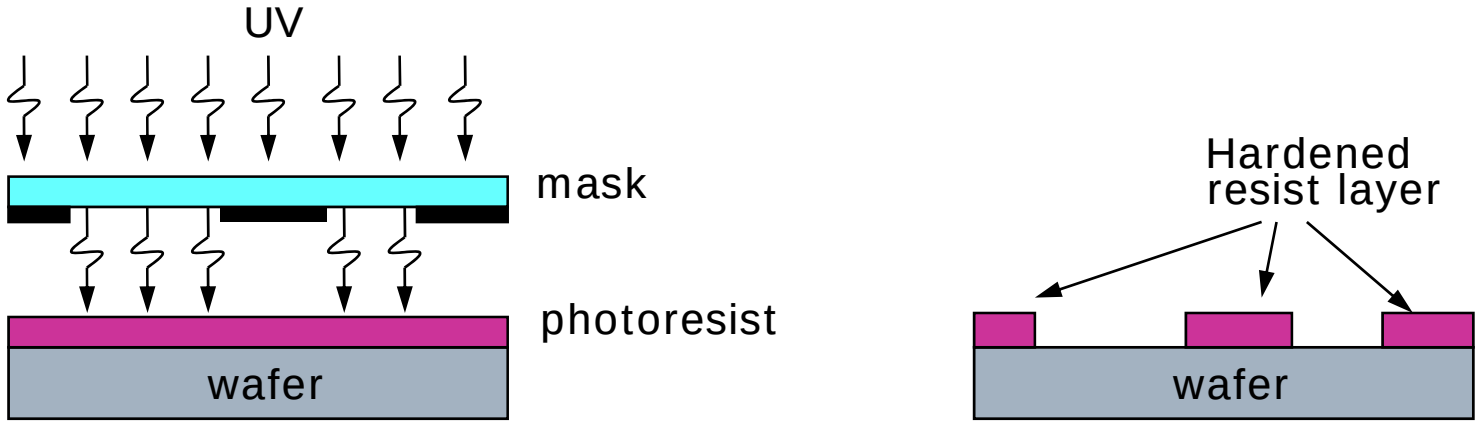


Transfer a Mask to Silicon Surface

- The process for transferring the mask pattern to the surface of a silicon region
  - Coat photoresist
  - Exposure step
  - Etching
- Coat photoresist
  - Liquid photoresist is sprayed onto a spinning wafer
- Exposure
  - Photoresist is sensitive to light, such as ultraviolet (UV)

Transfer a Mask to Silicon Surface

- The figure shown as below depicts the main idea



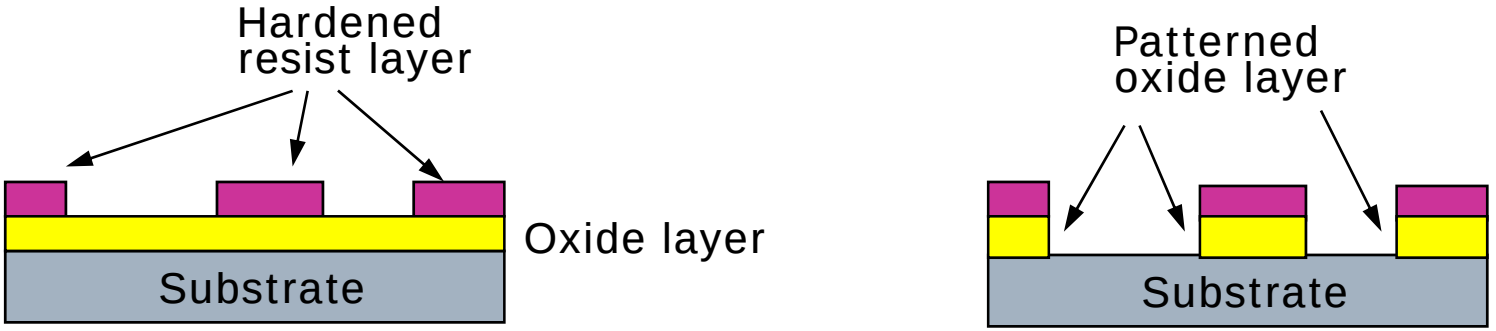
- The hardened resist layer is used to protect underlying regions from the etching process

Etching

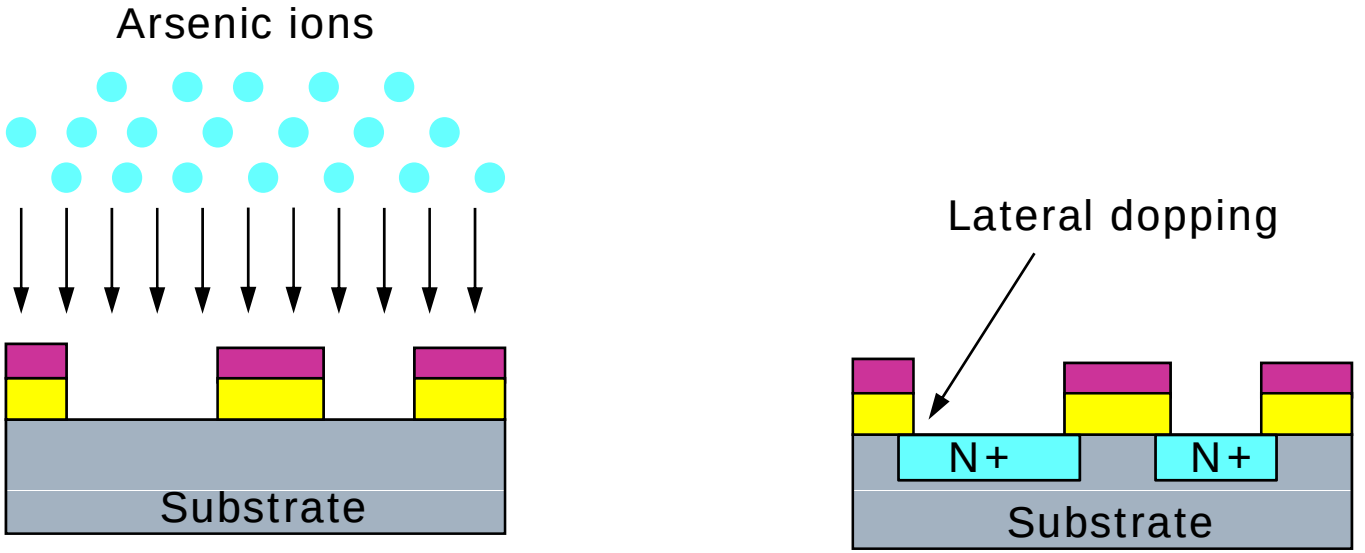
- The chemicals are chosen to attack and remove the material layer not shielded by the hardened photoresist

Dopping

- The figure shows the etching process



- Creation of doped silicon

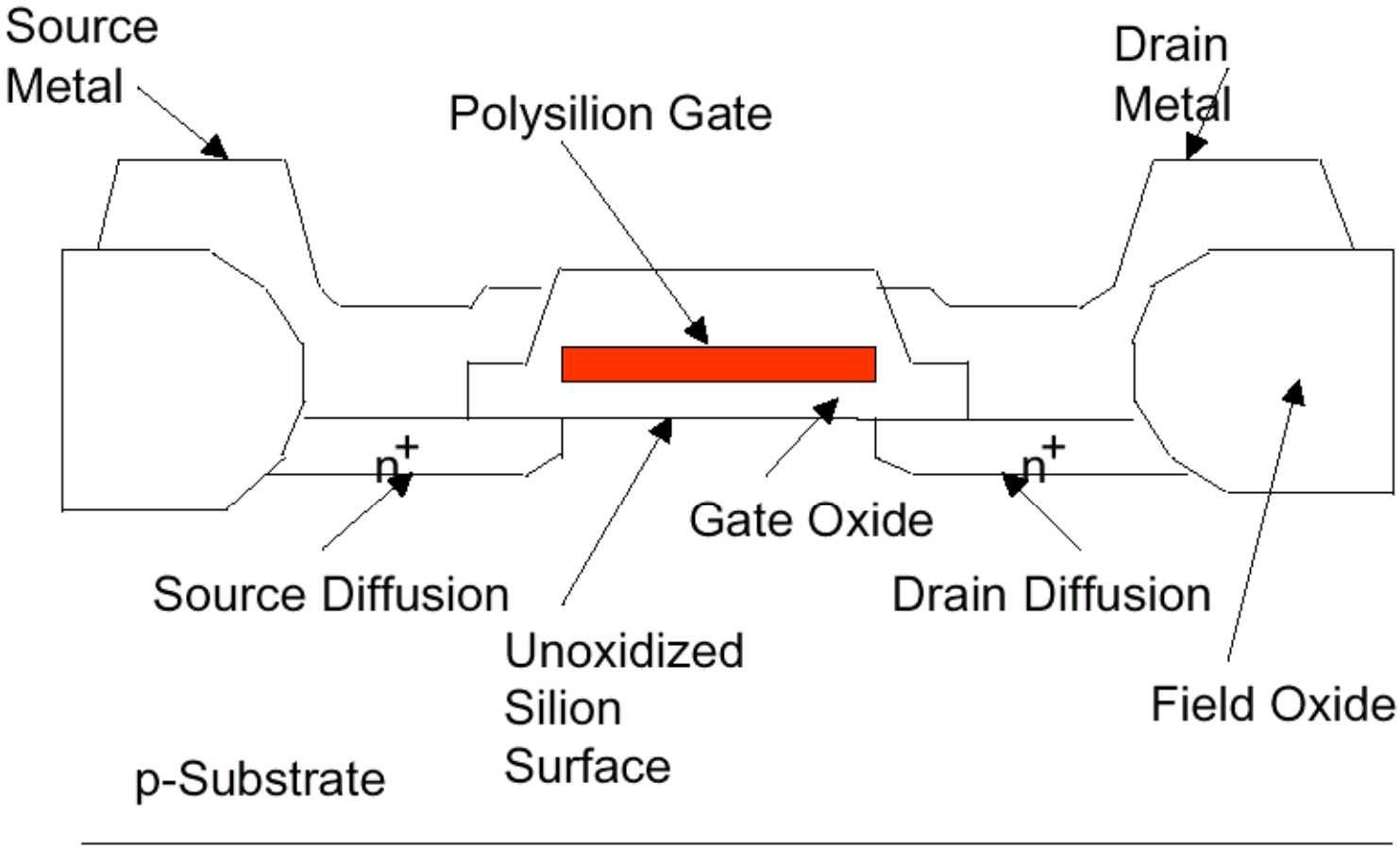


Dopping

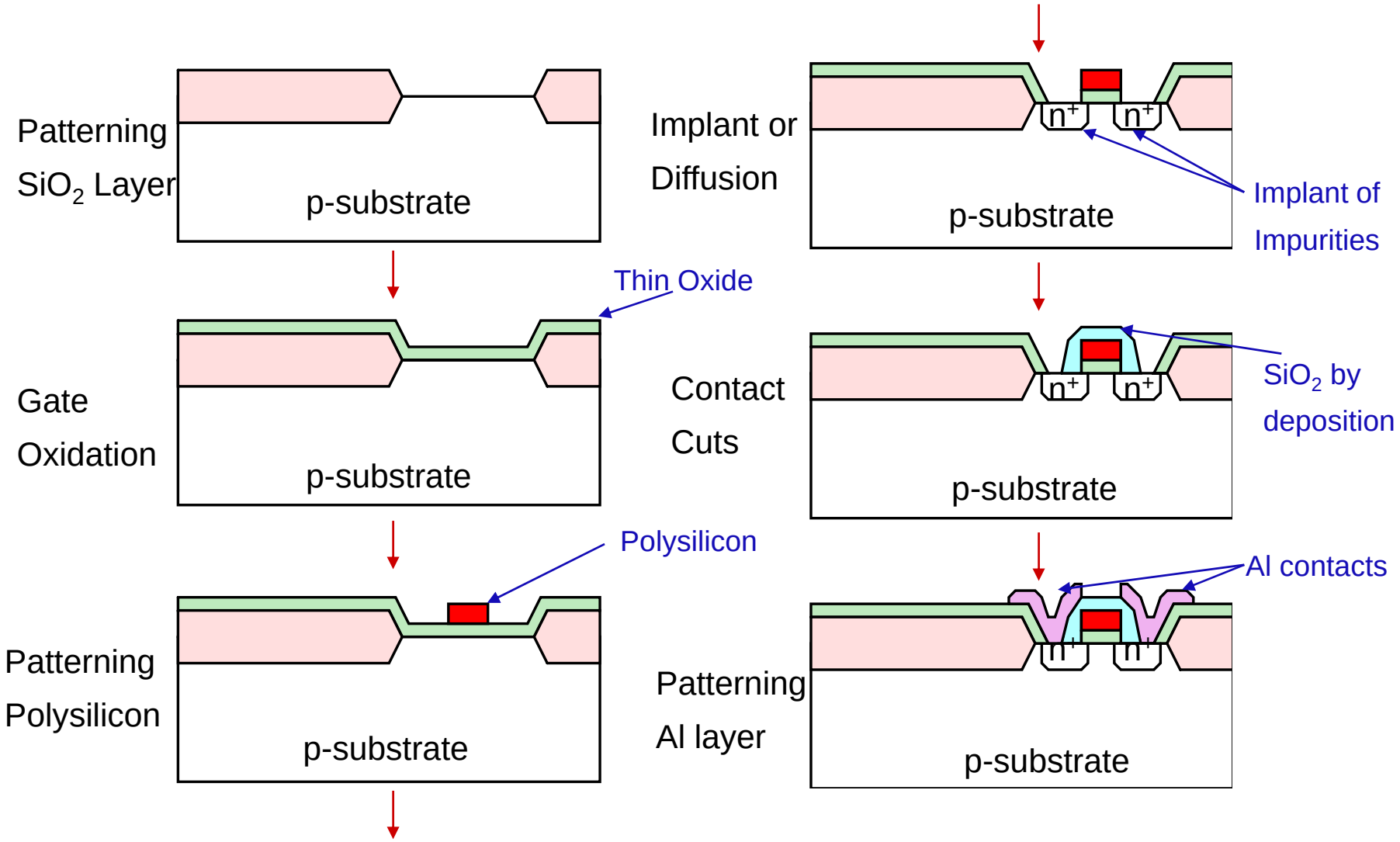
- The conductive characteristics of intrinsic silicon can be changed by introducing impurity atoms into the silicon crystal lattice
- Impurity elements that use (provide) electrons are called as acceptor (donor)
- Silicon that contains a majority of donors (acceptor) is known as n-type (p-type)
- When n-type and p-type materials are merged together, the region where the silicon changes from n-type to p-type is called junction

MOS Transistor

- Basic structure of a NMOS transistor



Fabrication Steps for an NMOS

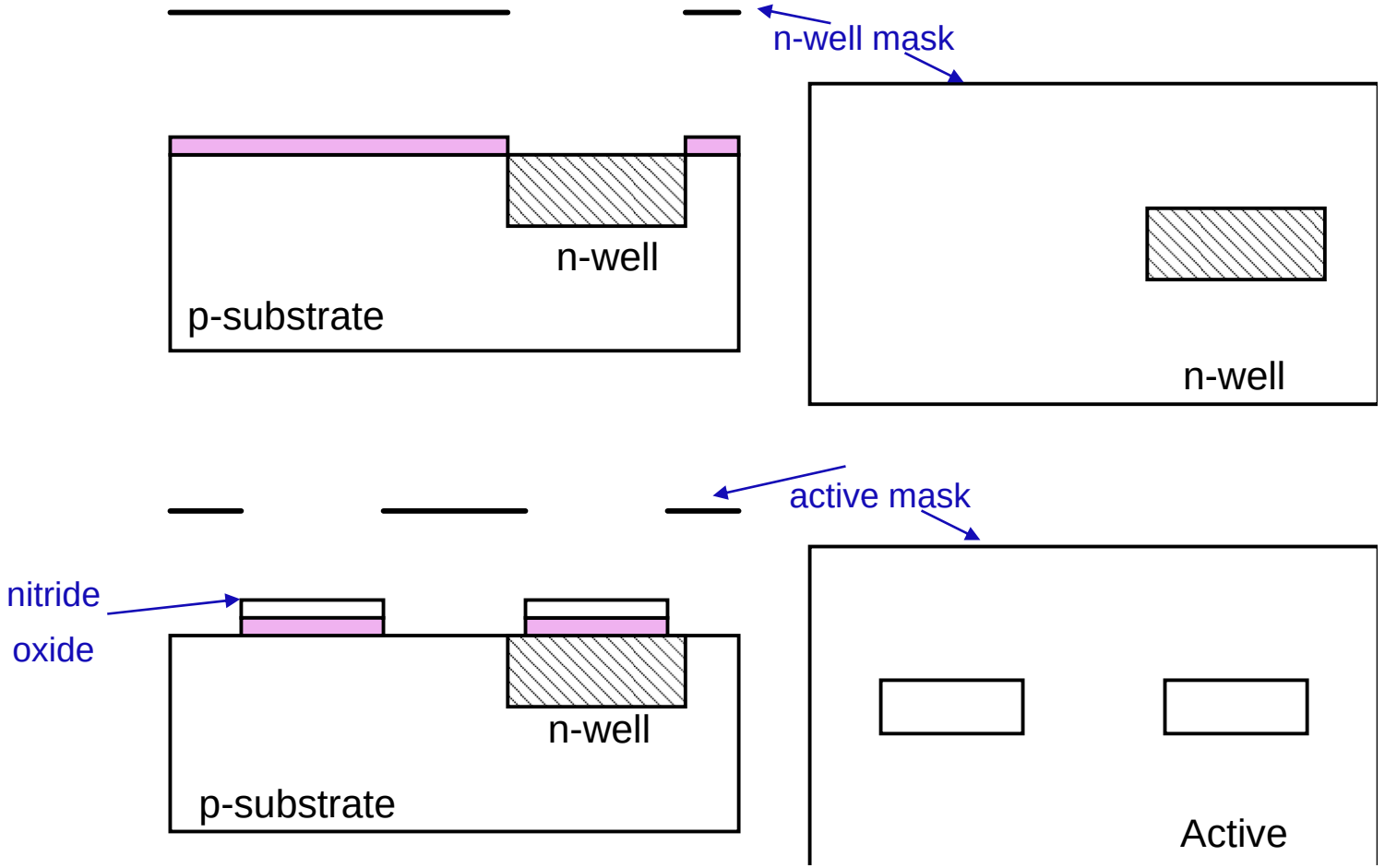


Basic CMOS Technology

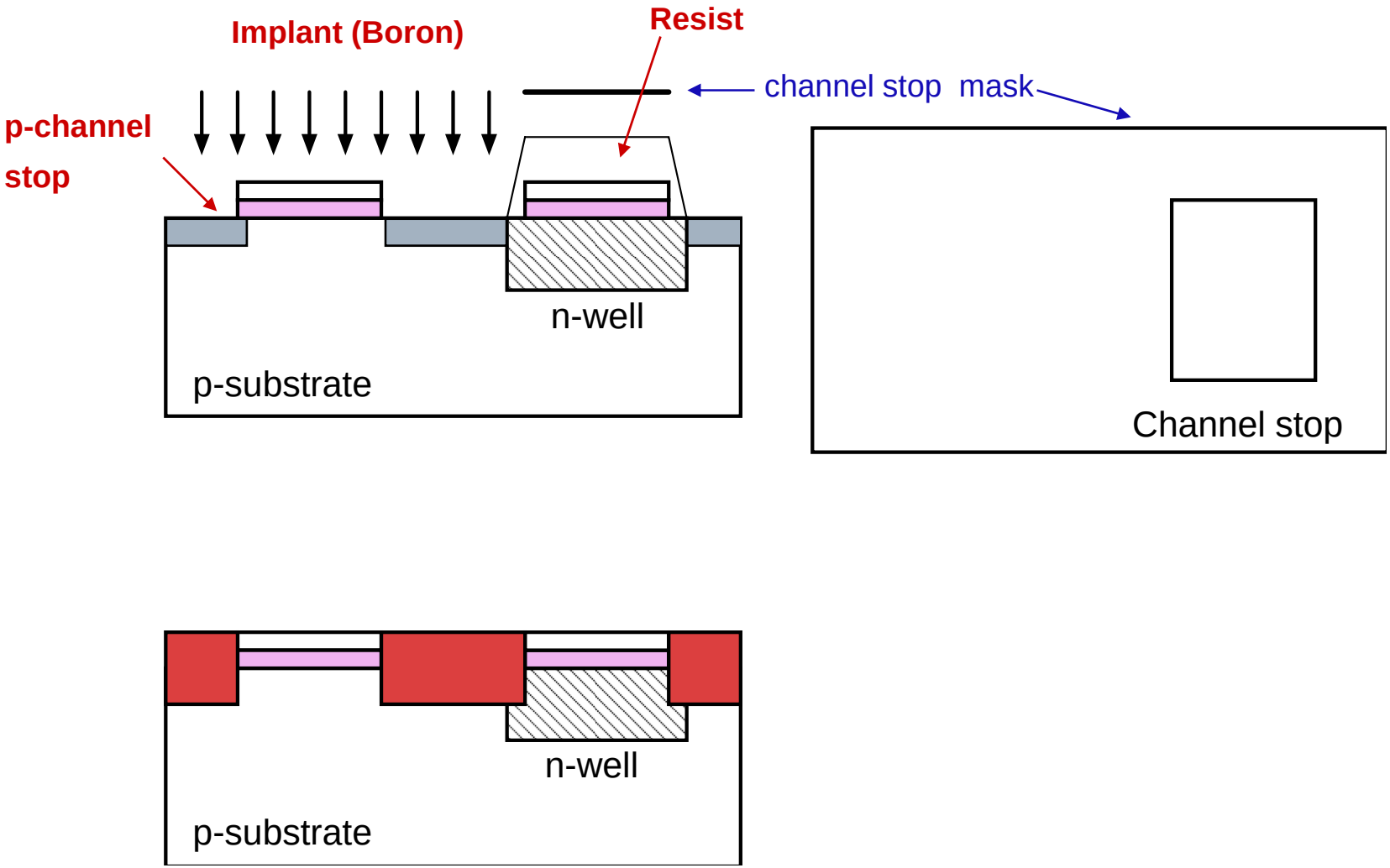
- Four dominant CMOS technologies
  - N-well process
  - P-well process
  - Twin-tub process
  - Silicon on insulator (SOI)
- N-well (P-well) process
  - Starts with a lightly doped p-type (n-type) substrate (wafer), create the n-type (p-type) well for the p-channel (n-channel) devices, and build the n-channel (p-channel) transistor in the native p-substrate (n-substrate)

N-Well CMOS Process

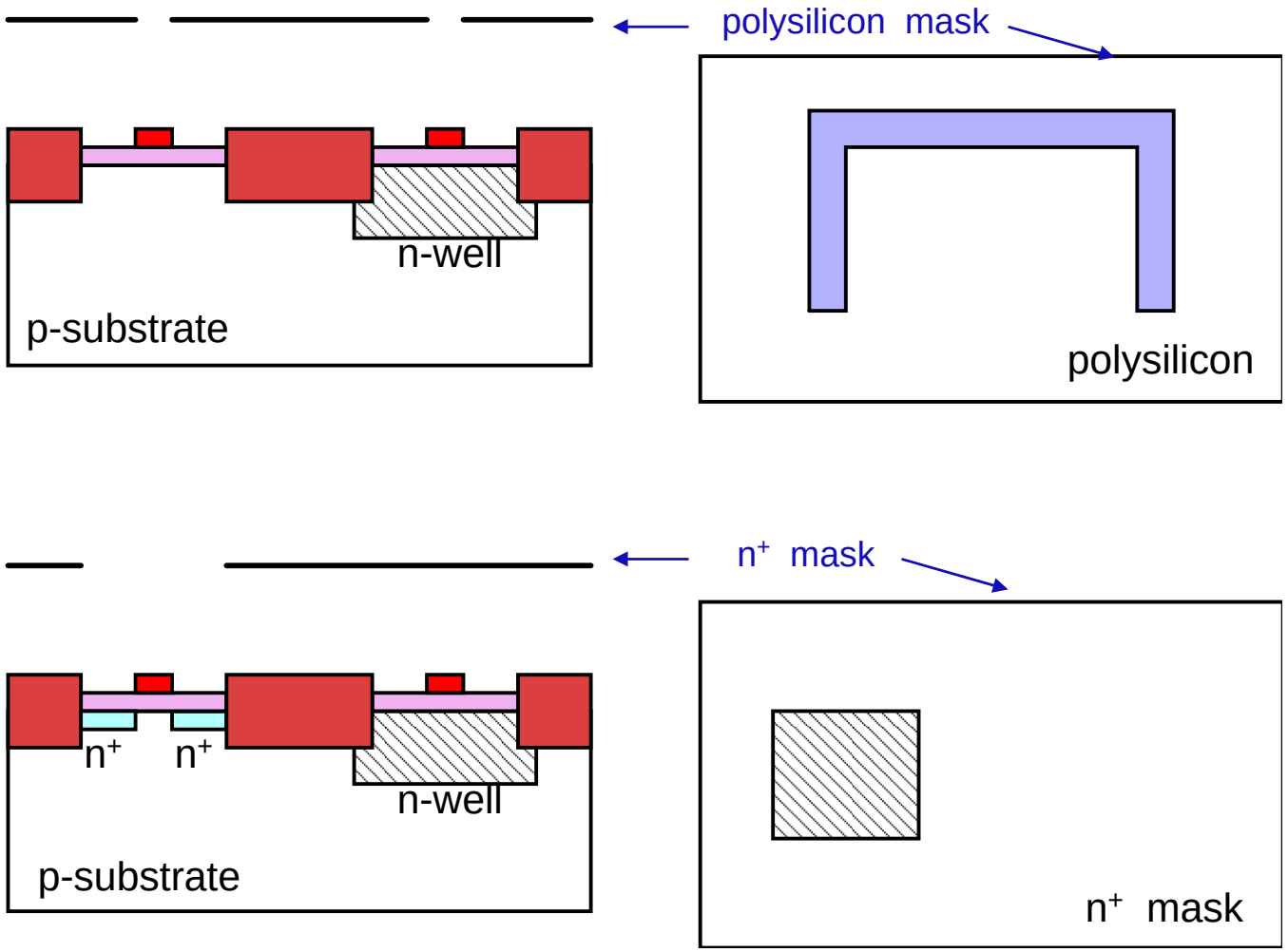
Cross Section of Physical Structure **Mask (top view)**



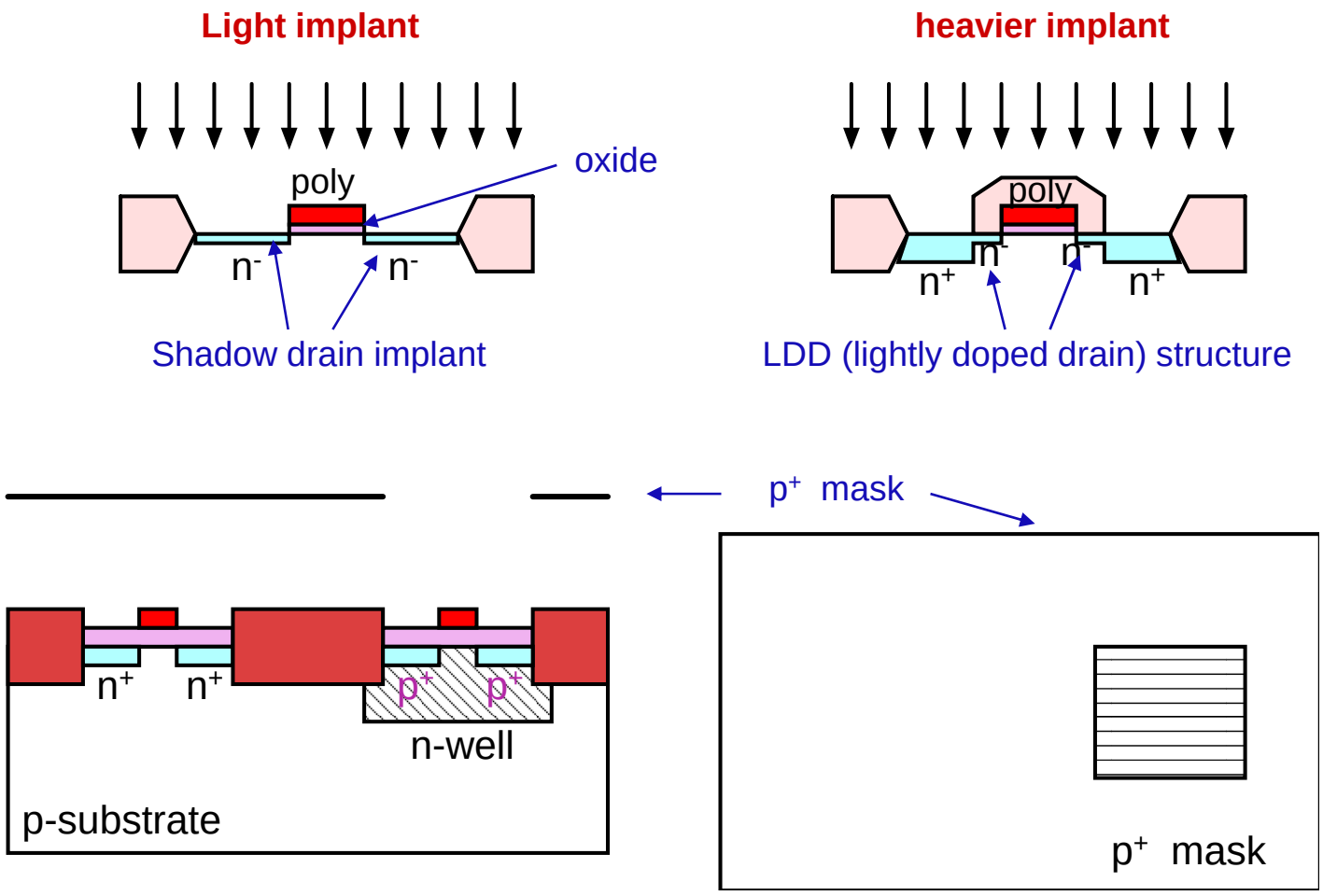
N-Well CMOS Process



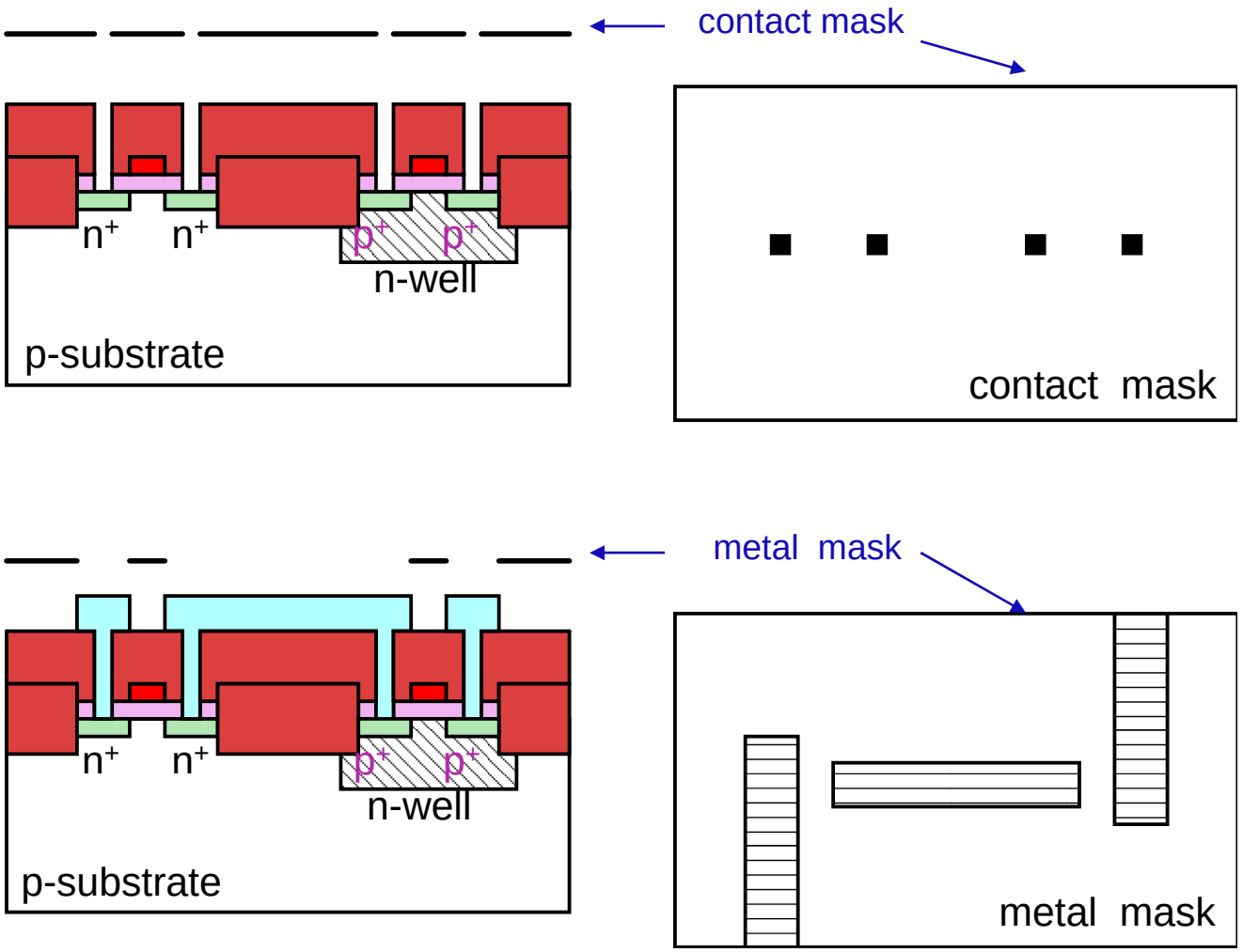
N-Well CMOS Process



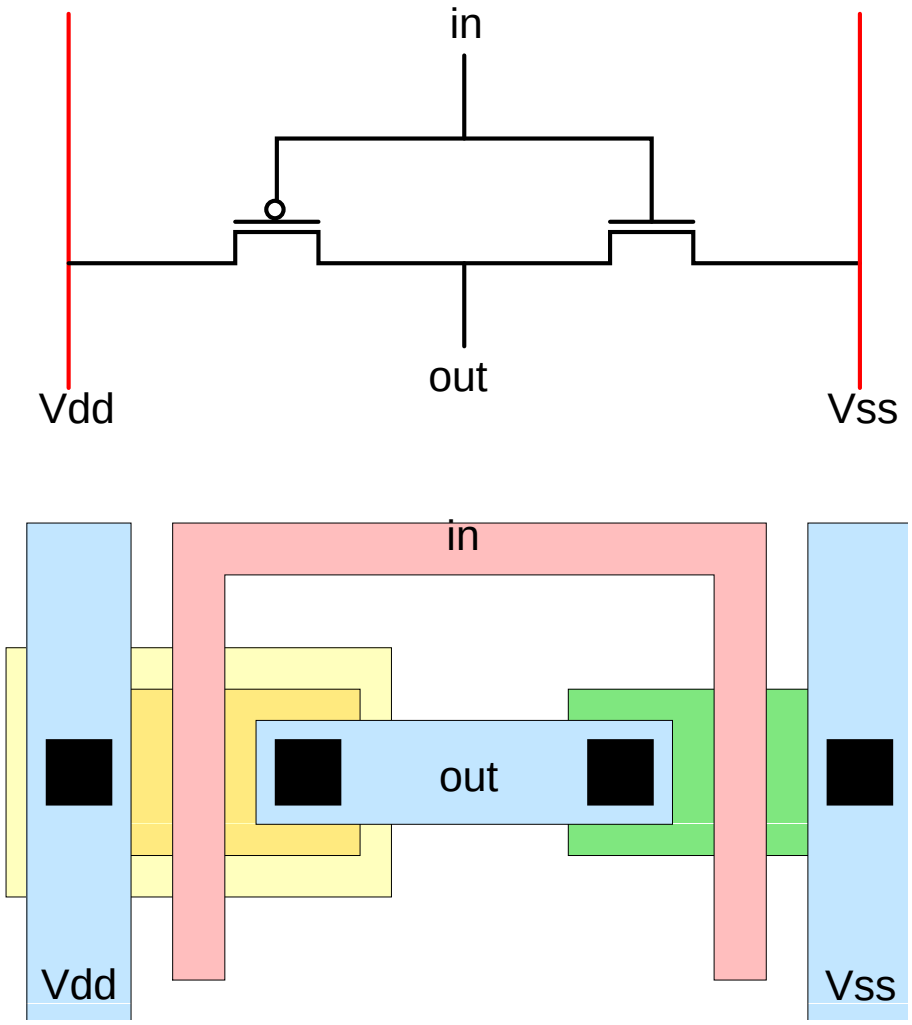
N-Well CMOS Process



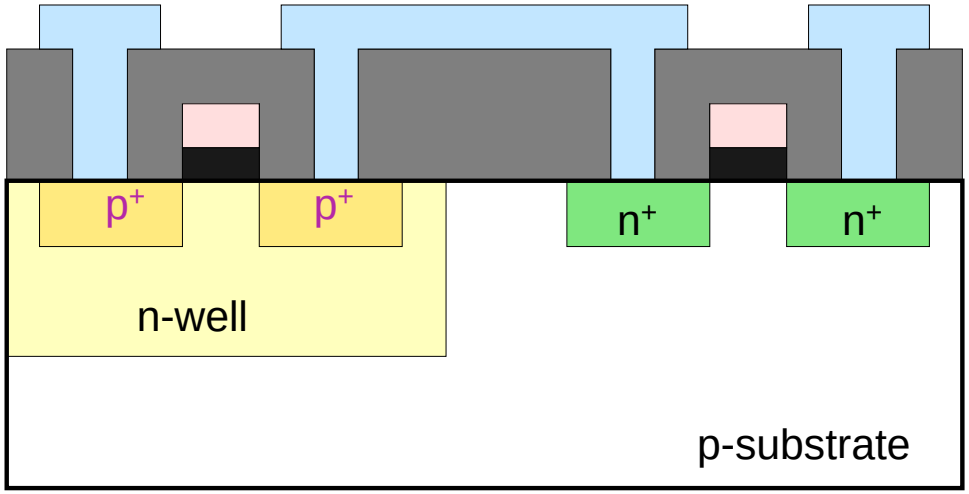
N-Well CMOS Process

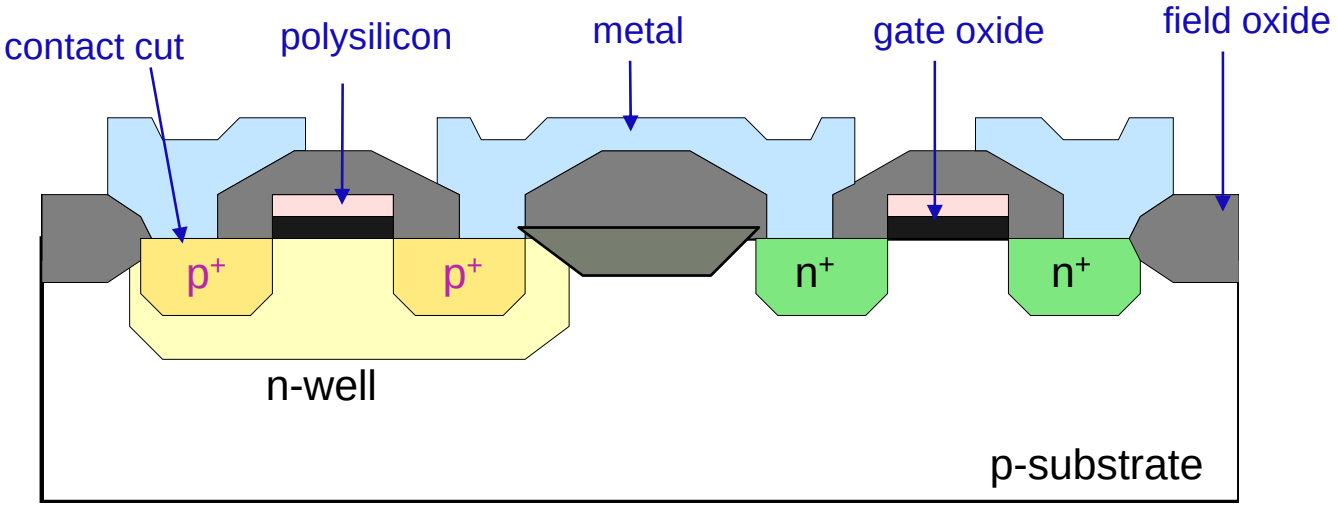


CMOS Inverter in N-Well Process

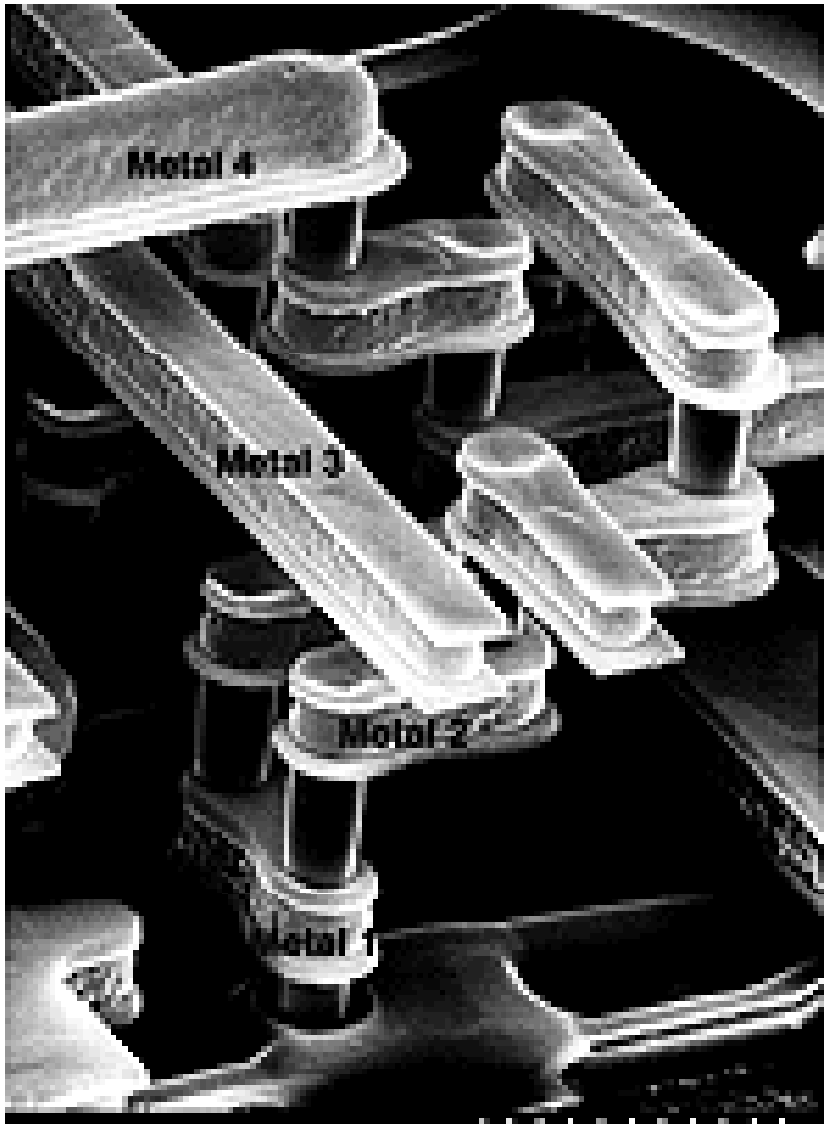


CMOS Inverter in N-Well Process





A Sample of Multi-Layer Metal



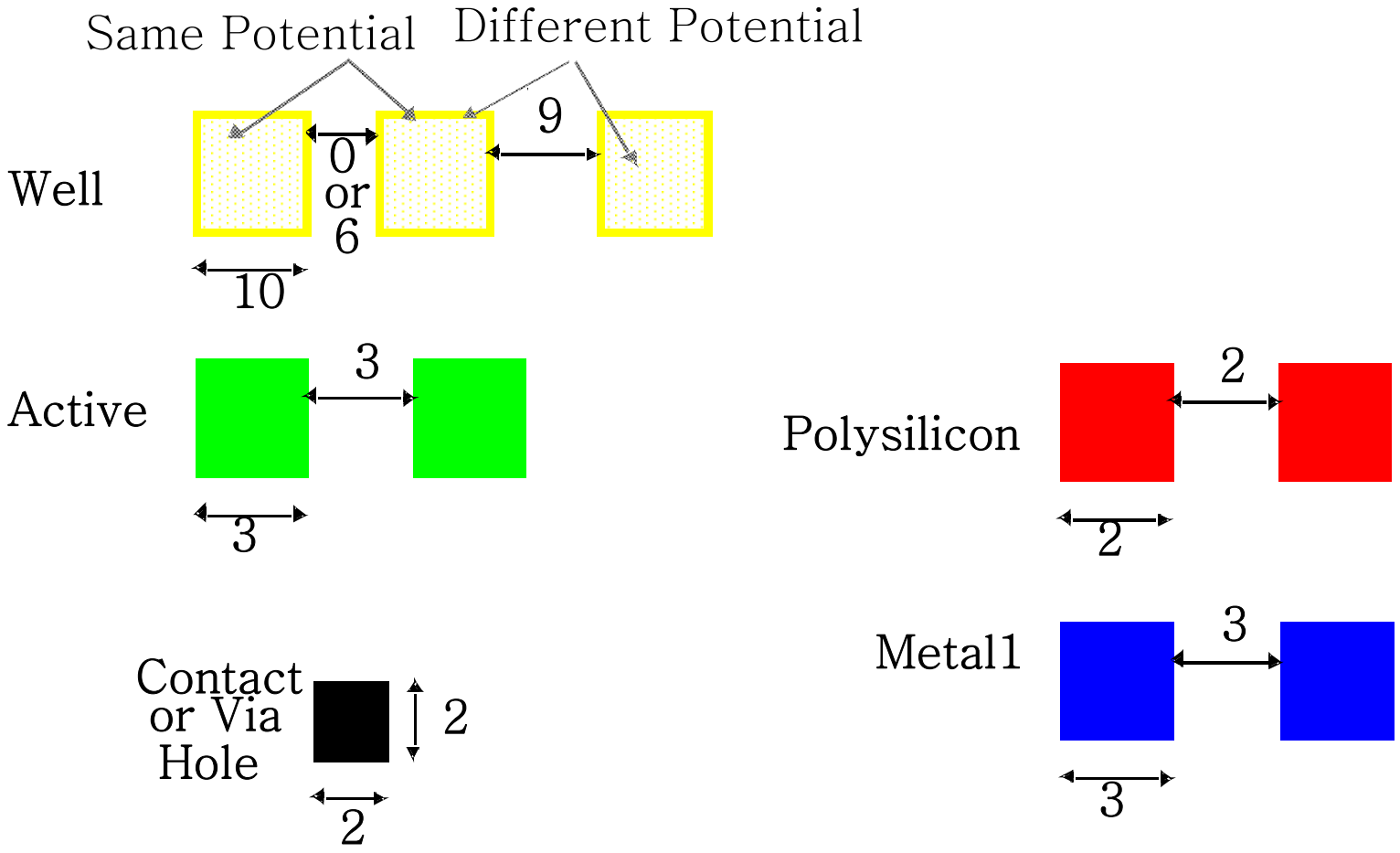
Design Rules

- Design rules (layout rules)
  - Provide a necessary communication link between circuit designers and process engineers during manufacturing phase
  - The goal of design rules is to achieve the optimum yield of a circuit with the smallest area cost
- Design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs

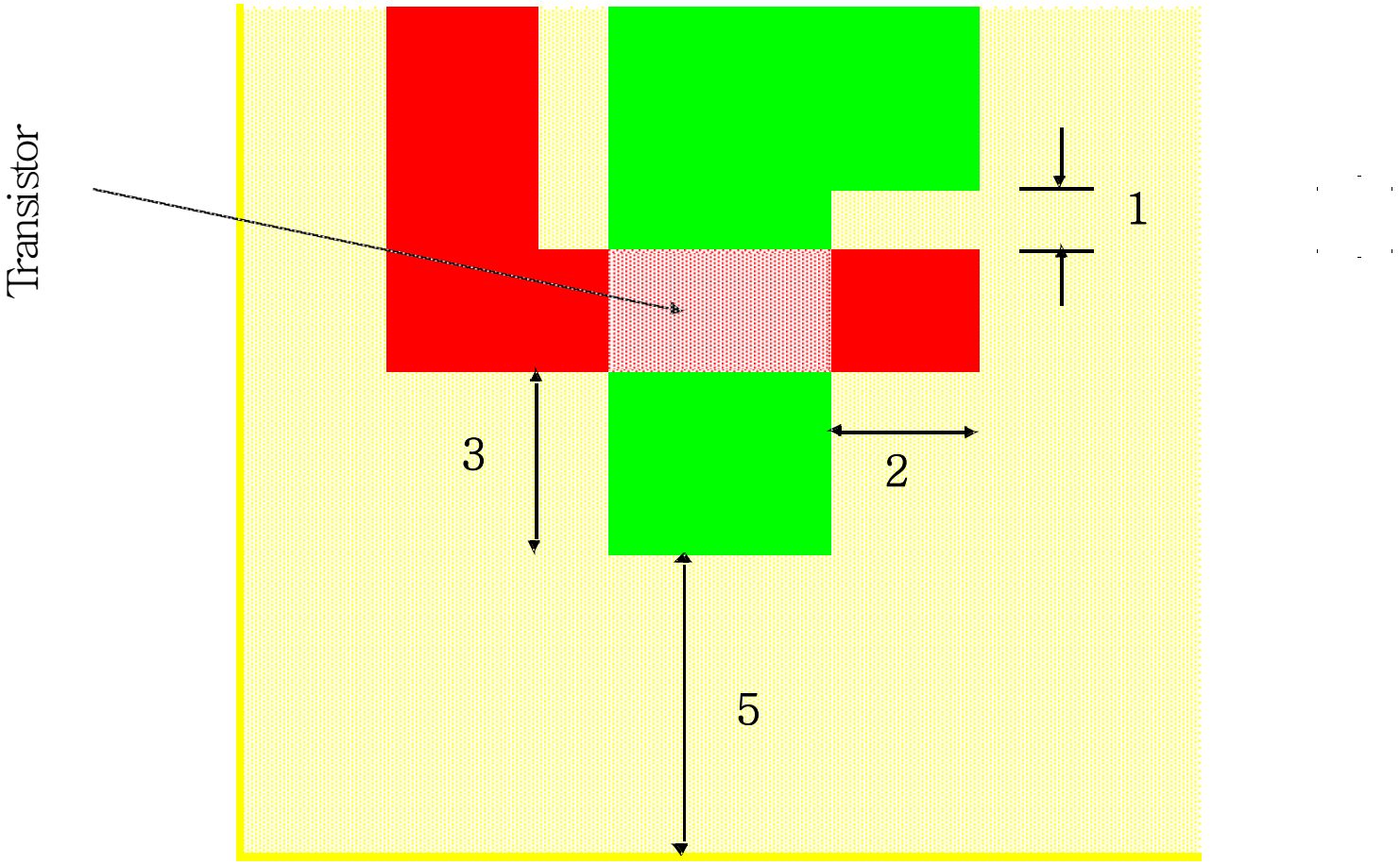
Design Rules

- The design rules primarily address two issues
  - The geometrical reproduction of features that can be reproduced by the mask-making and lithographical process
  - The interactions between different layers
- Lambda-based rules
  - Based on a single parameter, lambda, which characterizes the linear feature – the resolution of the complete wafer implementation process

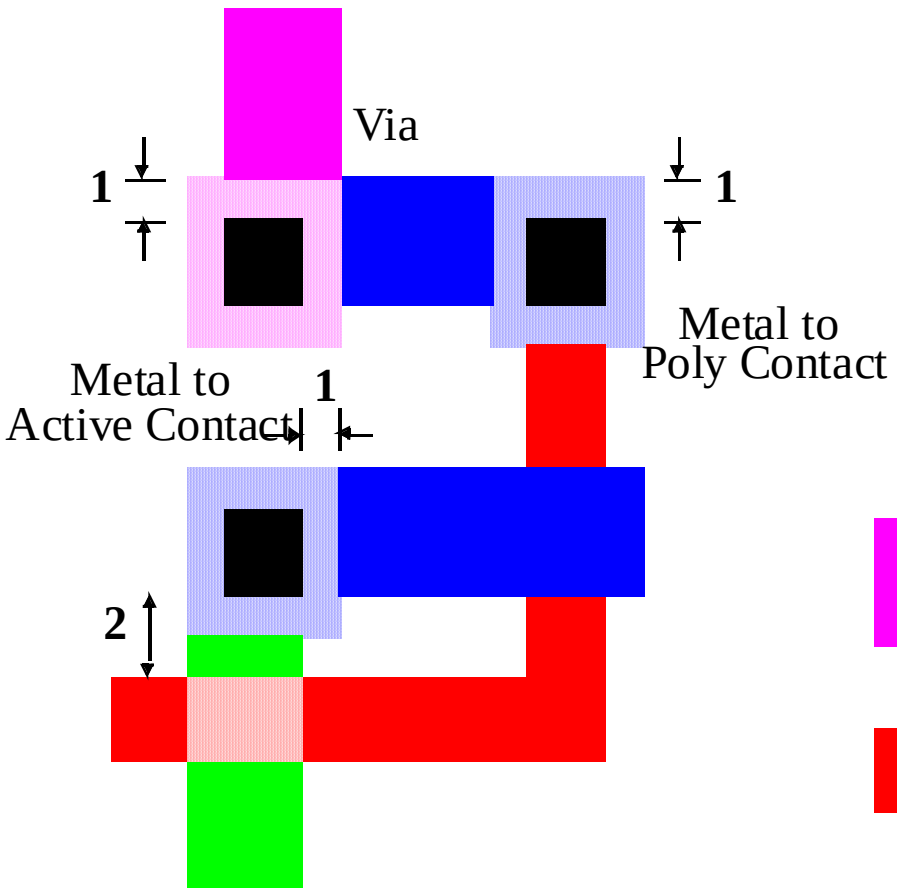
Examples of Design Rules

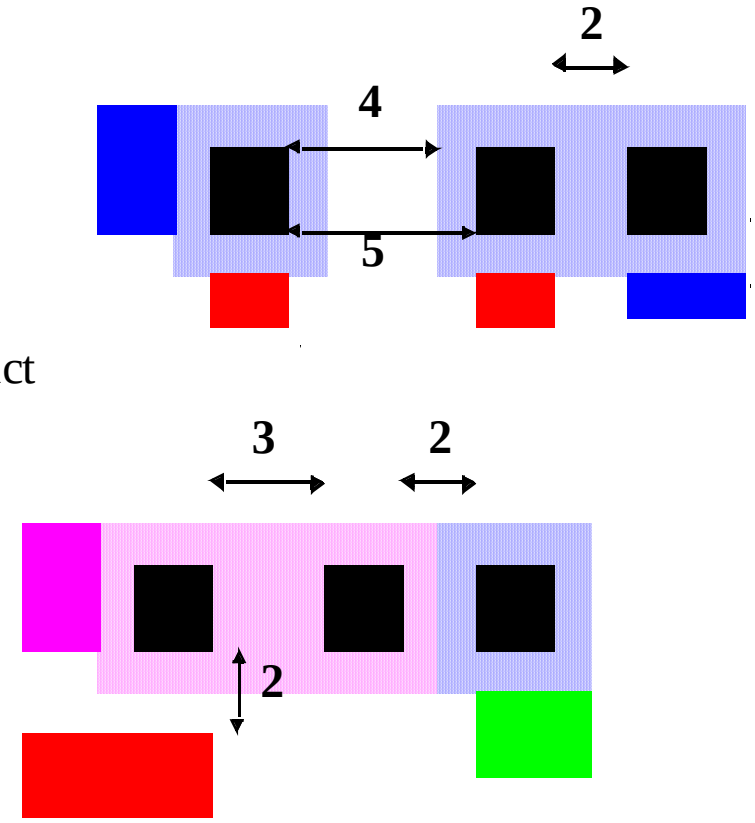


Transistor Layout

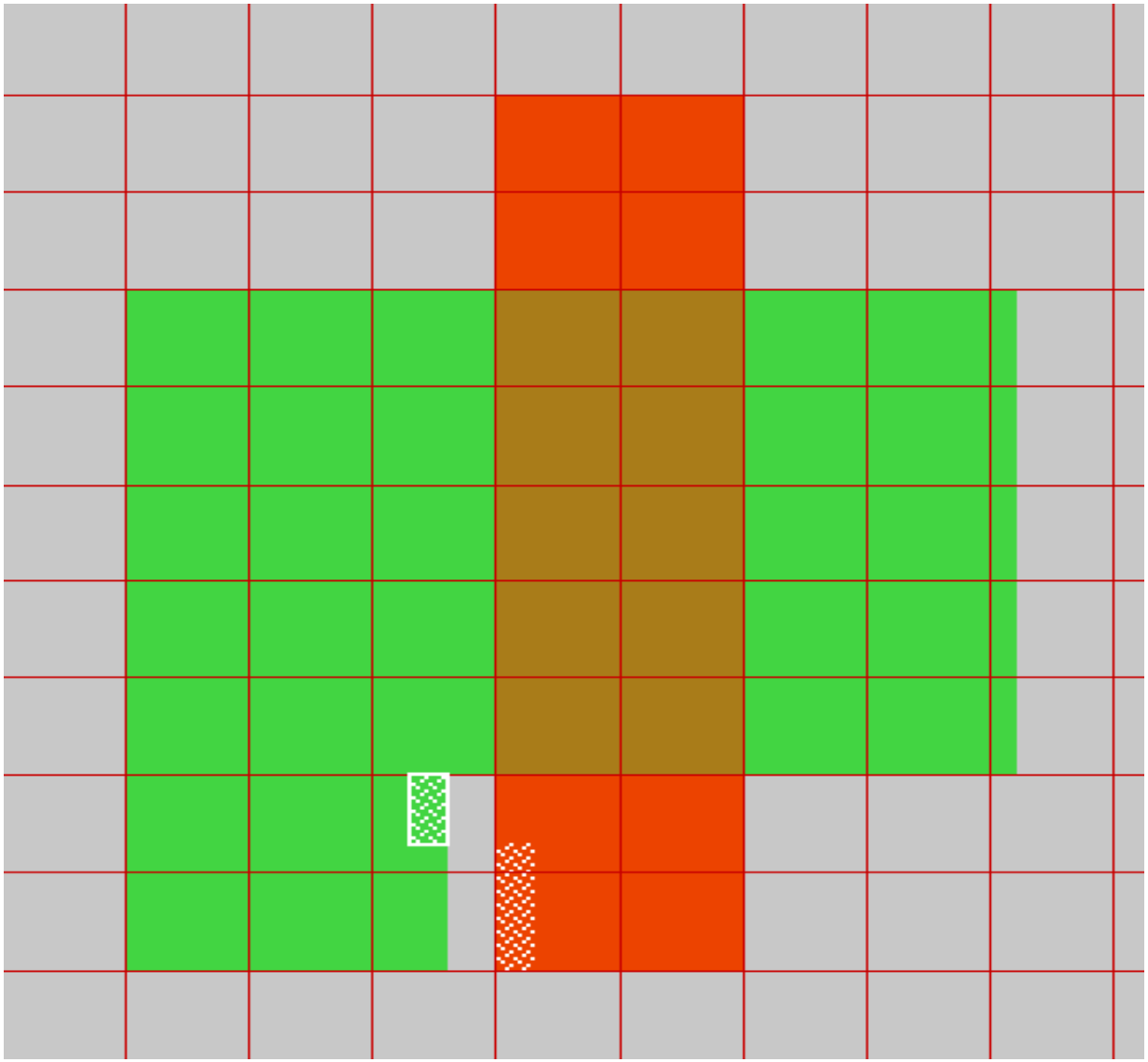


Design Rules for Vias & Contacts





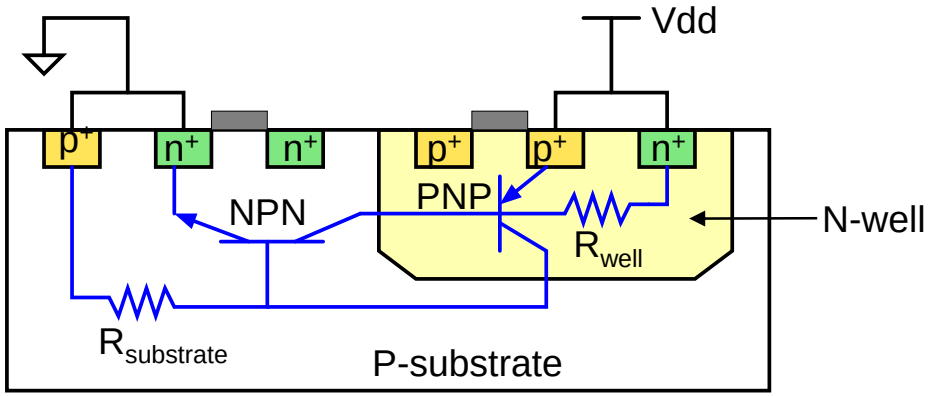
Design Rule Checker

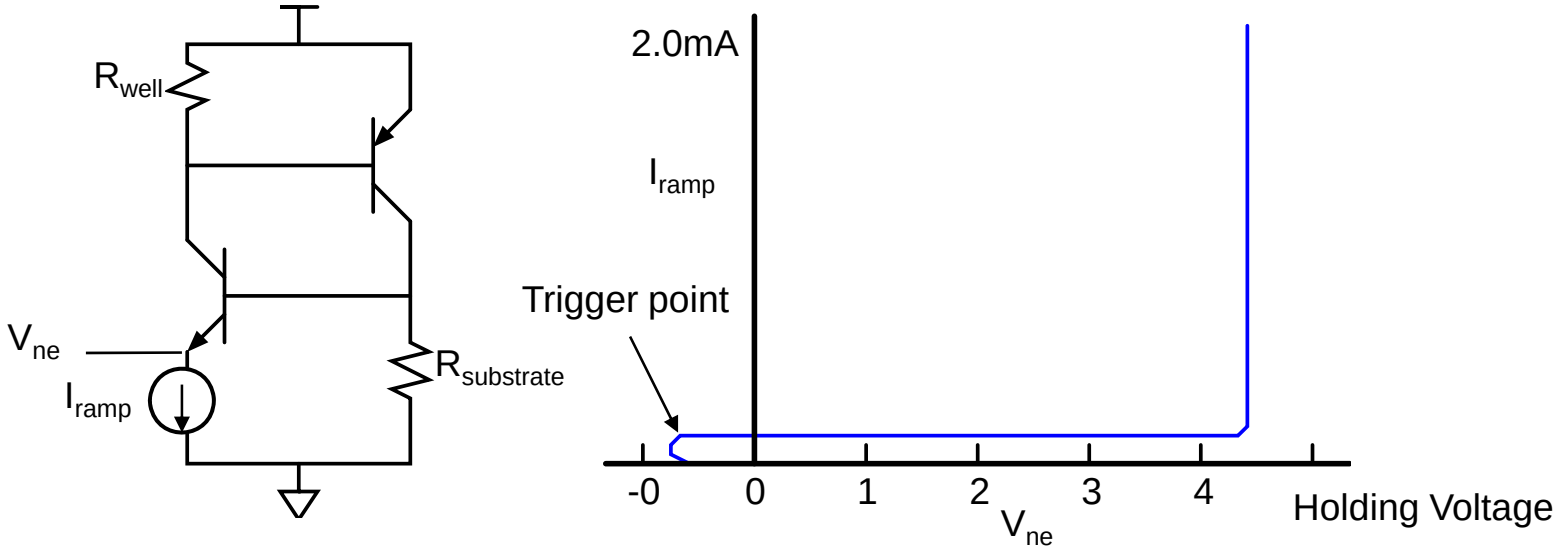


Latchup

- Latchup is defined as the generation of a low-impedance path in CMOS chips between power supply rail and the ground rail due to interaction of parasitic *pnp* and *npn* bipolar transistors
- These BJTs form a silicon-controlled rectifier (SCR) with positive feedback and virtually short circuit the power rail to ground, thus causing excessive current flows and even permanent device damage

Latchup of a CMOS Inverter





Latchup Triggering

- Latchup can be triggered by transient current or voltages that may occur internally to a chip during power-up or externally due to voltages or currents beyond normal operating ranges
- Two possible triggering mechanisms
  - Lateral triggering & vertical triggering
- Ex: the static trigger point of lateral triggering is

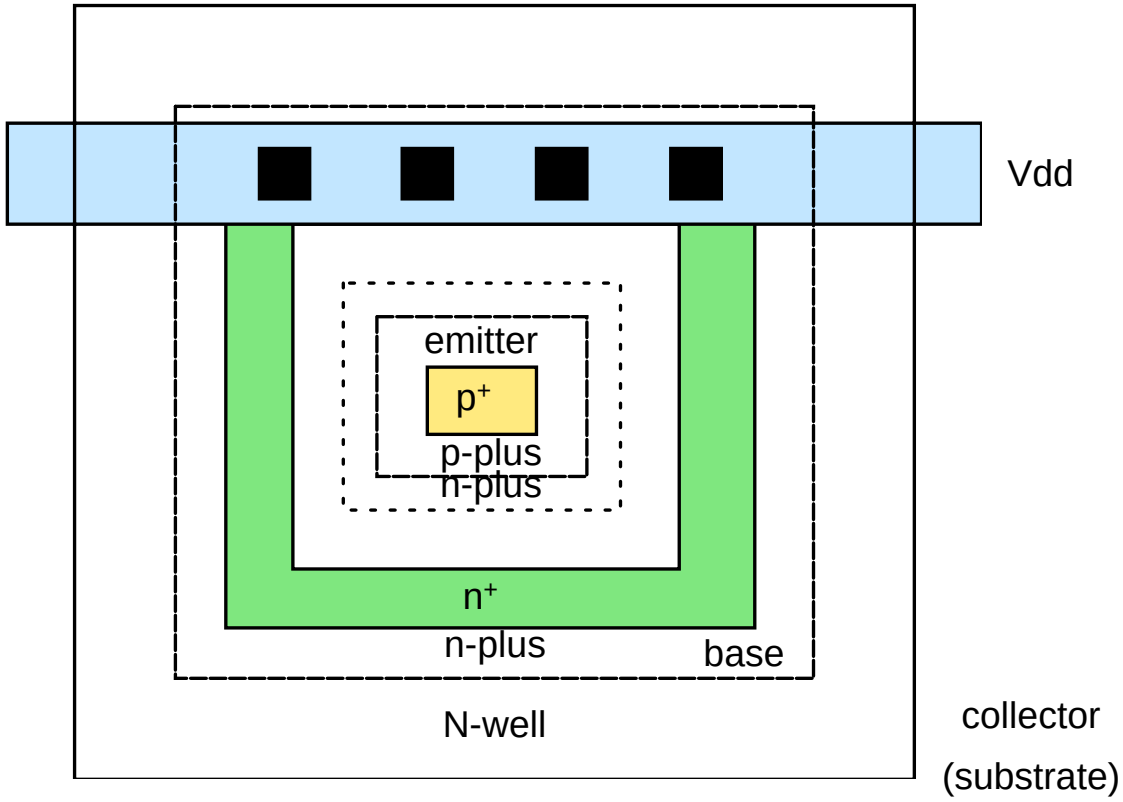
$$I_{ntrigger} \approx \frac{V_{pnp-on}}{\alpha_{npn} R_{well}}$$

Latchup Prevention

- Reducing the value of resistors and reducing the gain of the parasitic transistors are the basis for eliminating latchup
- Latchup can be prevented in two basic methods
  - Latchup resistant CMOS process
  - Layout techniques
- I/O latchup prevention
  - Reducing the gain of parasitic transistors is achieved through the use of guard rings

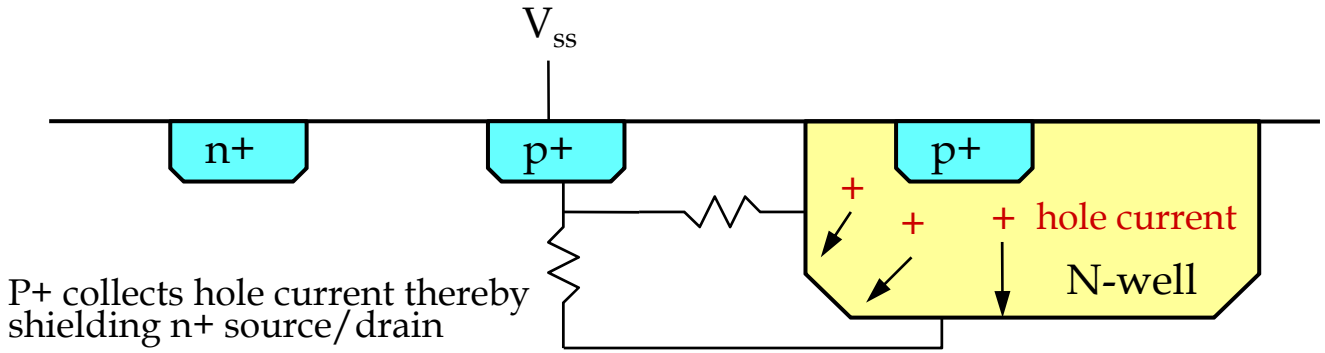
Guard Rings

- Guard rings are that p+ diffusions in the p-substrate and n+ diffusions in the n-well to collect injected minority carriers



I/O Latchup Prevention

- A p+ guard ring is shown below for an n+ source/drain



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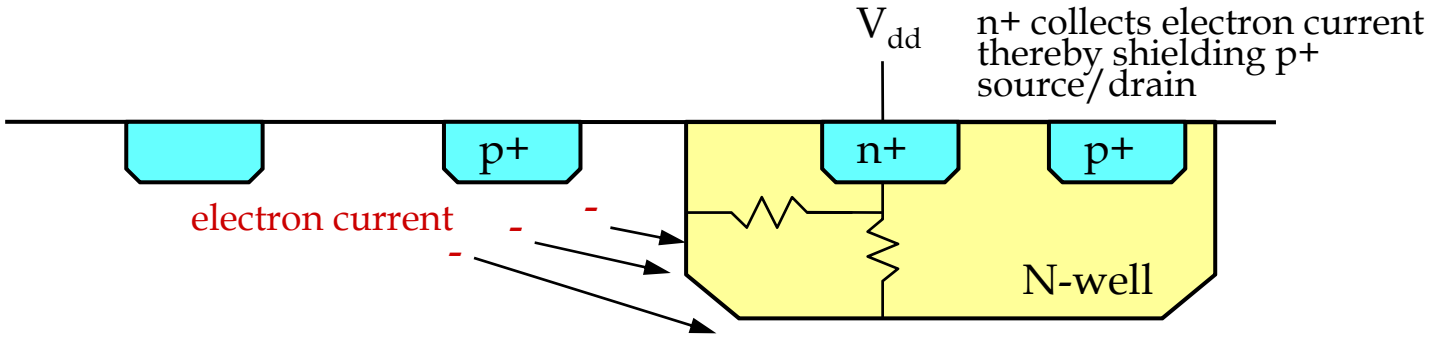
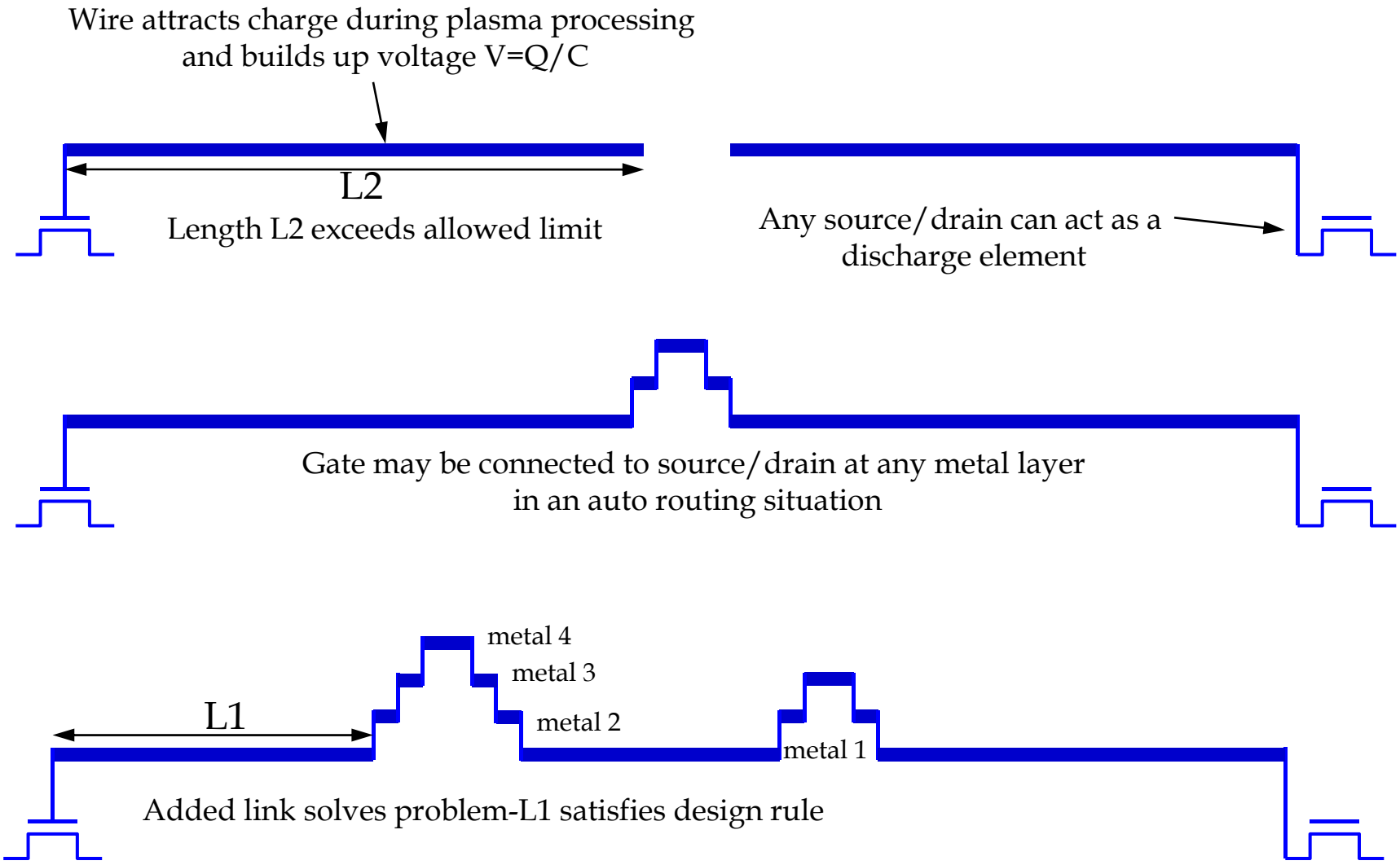


Antenna Rules

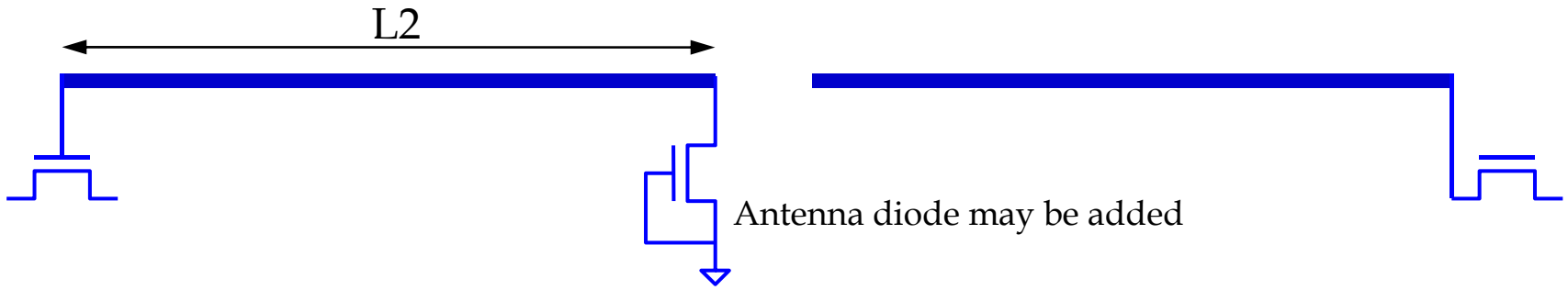
- When a metal wire contacted to a transistor gate is plasma-etched, it can charge up to a voltage sufficient to break down thin gate oxide
- The metal can be contacted to diffusion to provide a path for the charge to bleed away
- Antenna rules specify the maximum area of metal that can be connected to a gate without a source or drain to act as a discharge element
- The design rule normally defines the maximum ratio of metal area to gate area such that charge on the metal will not damage the gate
  - The ratios can vary from 100:1 to 5000:1 depending on the thickness of the gate oxide (and hence breakdown voltage) of the transistor in question

Antenna Rule Violation and Fix



Antenna Diode Addition

- An alternative method is to attach source/drain diodes to problem nets as shown below
  - These diodes can be simple junctions of n-diffusion to p-substrate rather than transistor source/drain regions



Layer Density Rules

- For advanced processes, a minimum and maximum density of a particular layer within a specific area should be specified
  - Layer density rules
- Layer density rules are required as a result of the CMP process and the desire to achieve uniform etch rates
- For example, a metal layer might have to have 30% minimum and 70% maximum fill within a 1mm by 1mm area
- For digital circuits, layer density levels are normally reached with normal routing
- Analog & RF circuits are almost spares
  - Gate and metal layers may have to be added manually or by a fill program after design has been completed

CMOS Process Enhancements

- Multiple threshold voltages
  - Low-V_t → more on current, but greater subthreshold leakage
  - High-V_t → less current, but smaller subthreshold leakage
  - User low-V_t devices on critical paths and higher-V_t devices elsewhere to limit leakage power
  - Multiple masks and implantation steps are used to set the various thresholds
- Silicon on insulator (SOI) process
  - The transistors are fabricated on an insulator
  - Two major insulators are used, SiOs and sapphire
  - Two major advantages: elimination of the capacitance between the source/drain regions and body, leading to higher-speed devices; lower subthreshold leakage

CMOS Process Enhancements

- High-k gate dielectrics
  - MOS needs high gate capacitance to attract charge to channel→very thin SiO_2 gate dieletrics
- Scaling trends indicate the gate leakage will be unacceptably large in such thin gates
  - Gates could use thicker dielectrics and hence leak less if a material with a higher dielectric constant were available

Summary

- Some of more common CMOS technologies have been covered
- A representative set of n-well process has been introduced
- Concepts of design rules have been presented
- The important condition known as latchup has been introduced with necessary design rules to avoid this condition in CMOS chips
- Antenna rules & layer density rules should be considered in modern manufacturing process