Chapter 6
Combinational CMOS Circuit and Logic Design

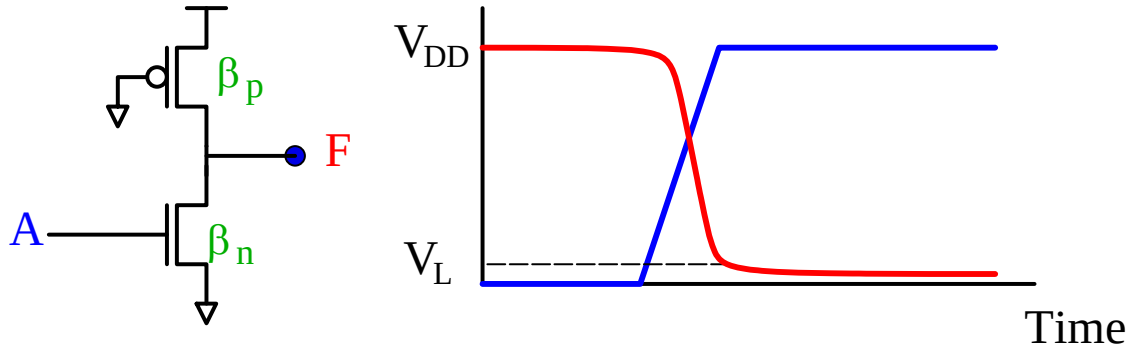
Jin-Fu Li
Advanced Reliable Systems (ARES) Laboratory
Department of Electrical Engineering
National Central University
Jhongli, Taiwan

Outline

- Advanced CMOS Logic Design
- I/O Structures

Pseudo-NMOS Logic

- A pseudo-NMOS inverter



  - The low output voltage can be calculated as

$$\beta_n (V_{DD} - V_{tn}) V_L = \frac{\beta_P}{2} (V_{DD} - |V_{tp}|)^2$$

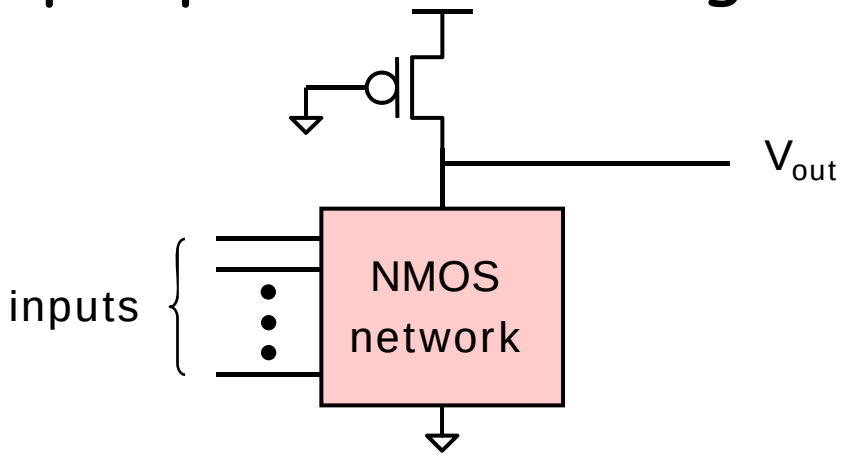
for $V_{tn} = -V_{tp} = V_t$

$$V_L = \frac{\beta_P}{2\beta_n} (V_{DD} - V_T)$$

  - Thus V_L depends strongly on the ratio β_p / β_n
  - The logic is also called ratioed logic

Pseudo-NMOS Logic

- An N-input pseudo-NMOS gate

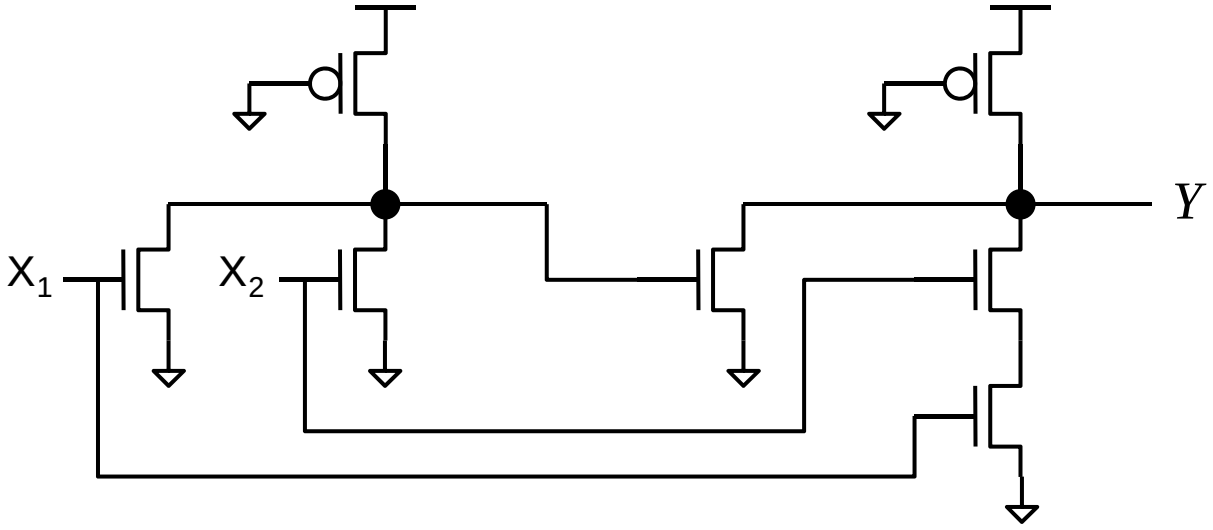


- Features of pseudo-NMOS logic
  - Advantages
    - Low area cost→only N+1 transistors are needed for an N-input gate
    - Low input gate-load capacitance→C_{gn}
  - Disadvantage
    - Non-zero static power dissipation

Pseudo-NMOS XOR Gate

- An example of XOR gate realized with pseudo-NMOS logic
  - The XOR is defined by

$$Y = X_1 \oplus X_2 = X_1\overline{X_2} + \overline{X_1}X_2 = \overline{\overline{X_1X_2 + \overline{X_1}\,\overline{X_2}}} = \overline{X_1X_2 + \overline{X_1 + X_2}}$$



Choosing Transistor Sizes

- Goals
  - Noise margin
  - Power consumption
  - Speed
- Noise margin
  - It is affected by the low output voltage (V_L)
  - V_L is determined by β_p / β_n
- Speed
  - The larger the W/L of the load transistor, the faster the gate will be, particularly when driving many other gates
  - Unfortunately, this increases the power dissipation and the area of the driver network

Choosing Transistor Sizes

- Power dissipation
  - A pseudo-NMOS logic gate having a "1" output has no static (DC) power dissipation.
  - However, a pseudo-NMOS gate having a "0" output has a static power dissipation
    - The static power dissipation is equal to the current of the PMOS load transistor multiplied by the power supply voltage. Thus, the power is given by

$$P_{dc} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_P (V_{gs} - V_{tp})^2 V_{dd}$$

  - The large PMOS results in large power dissipation
- Power-reduction methods
  - Select an appropriate PMOS
  - Increase the bias voltage of PMOS

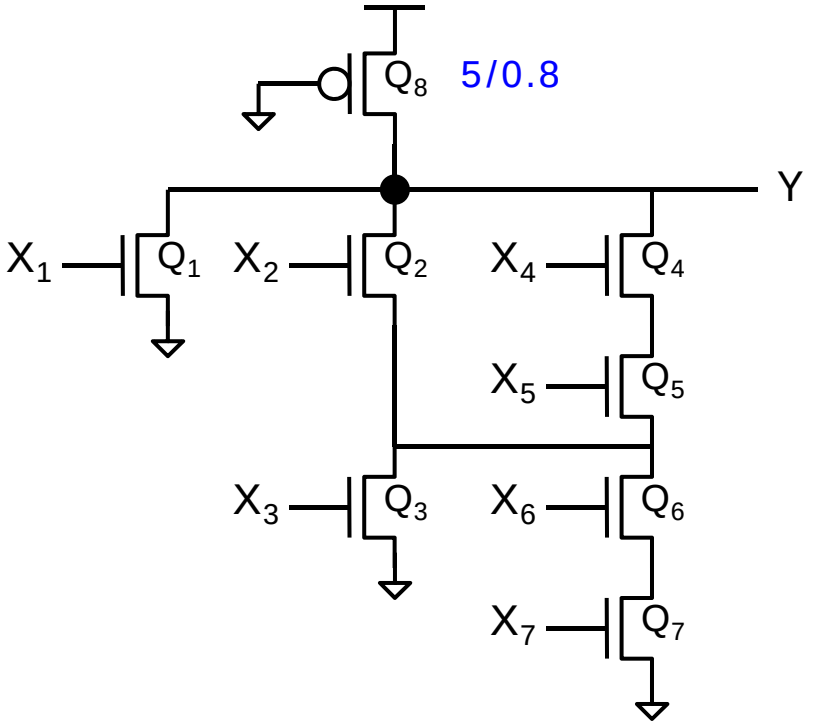
Choosing Transistor Sizes

- A simple procedure for choosing transistor sizes of pseudo-NMOS logic gates
  - The relative size (W/L) of the PMOS load transistor is chosen as a compromise between speed and size versus power dissipation
  - Once the size of the load transistor has been chosen, then a simple procedure can be used to choose the W/Ls of the NMOS transistors in the NMOS network
    - Let $(W/L)_{eq}$ be equal to one-half of the W/L of the PMOS load transistor
    - For each transistor Q_i, determine the maximum number of drive transistors it will be in series, for all possible inputs. Denote this number n_i.
    - Take $(W/L)_i=n_i(W/L)eq$

An Example

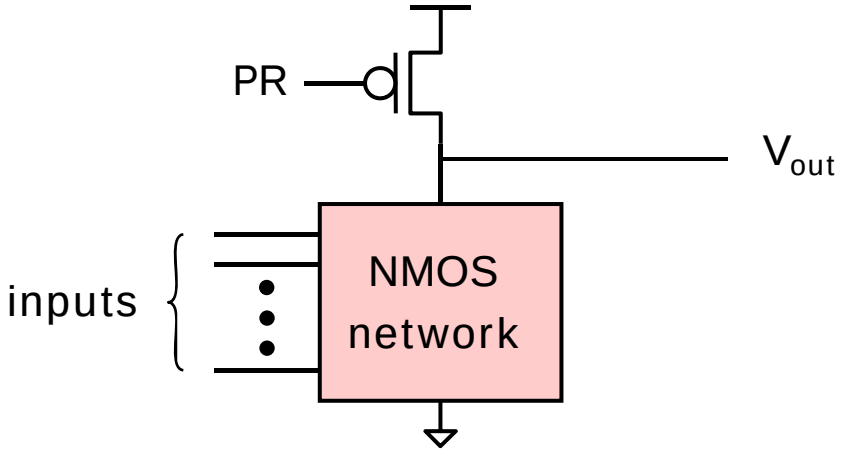
- Choose appropriate sizes for the pseudo-NMOS logic gate shown below
  - $(W/L)_8$ is 5 um/0.8 um
  - $(W/L)_{eq}$ is (5/0.8)/2=3.125
  - Gate lengths of drive transistors are taken at their minimum 0.8um
  - Thus we can obtain

Transistor	Size
Q_1	2.5um/0.8um
Q_2	5.0um/0.8um
Q_3	5.0um/0.8um
Q_4	10um/0.8um
Q_5	10um/0.8um
Q_6	10um/0.8um
Q_7	10um/0.8um



Dynamic Logic

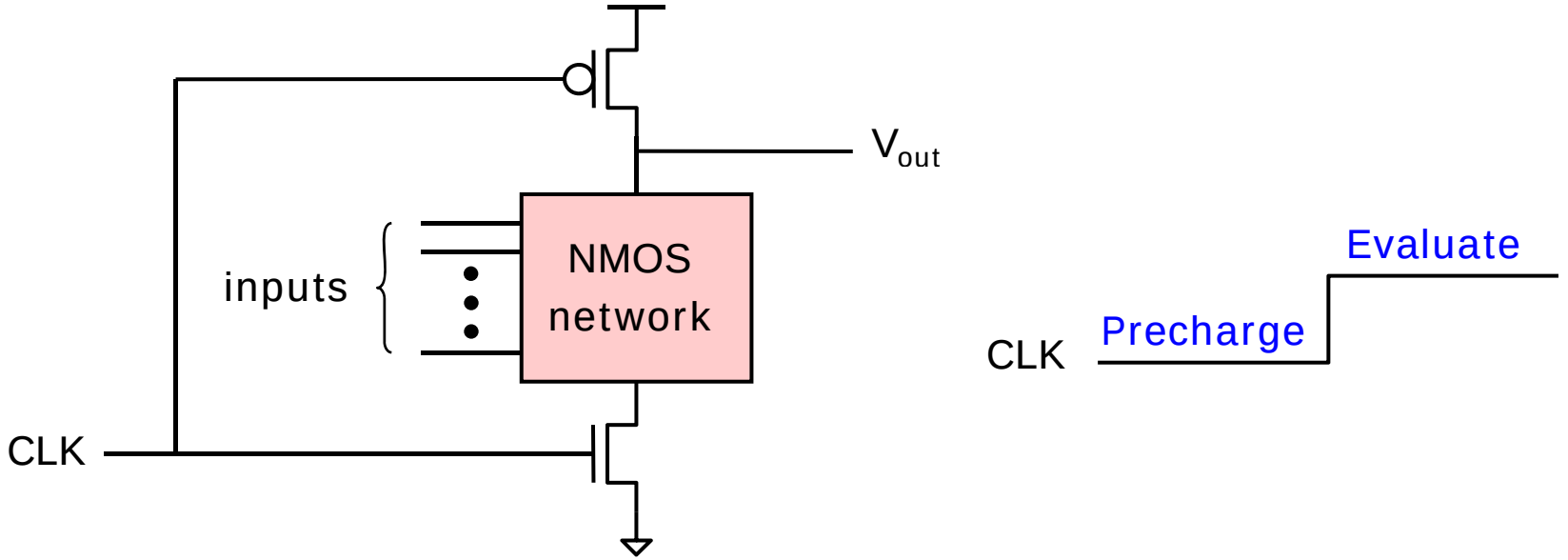
- To eliminate the static power dissipation of pseudo-NMOS logic
  - An alternative technique is to use ***dynamic precharging*** called dynamic logic as shown below



  - Normally, during the time the output is being precharged, the NMOS network should not be conducting
    - This is usually not possible

Dynamic Logic

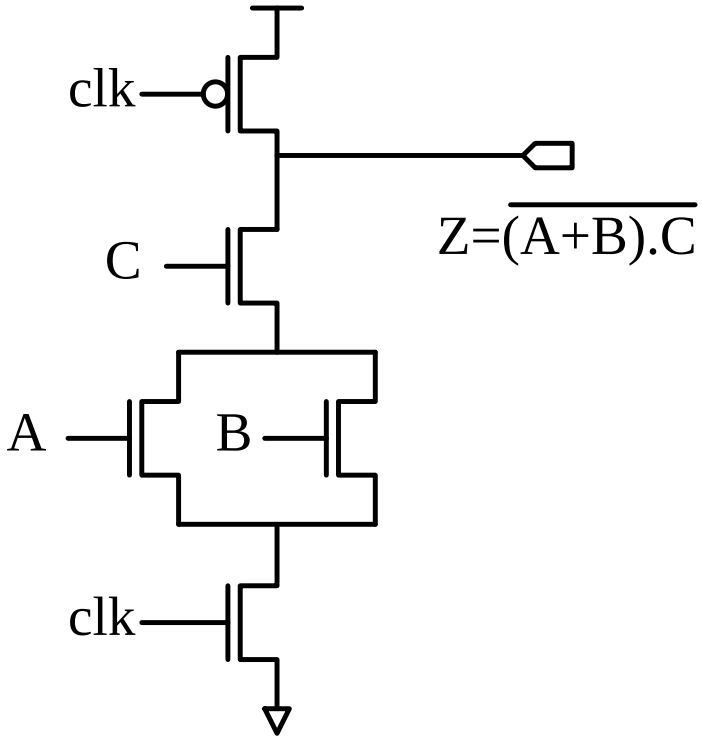
- Another dynamic logic technique

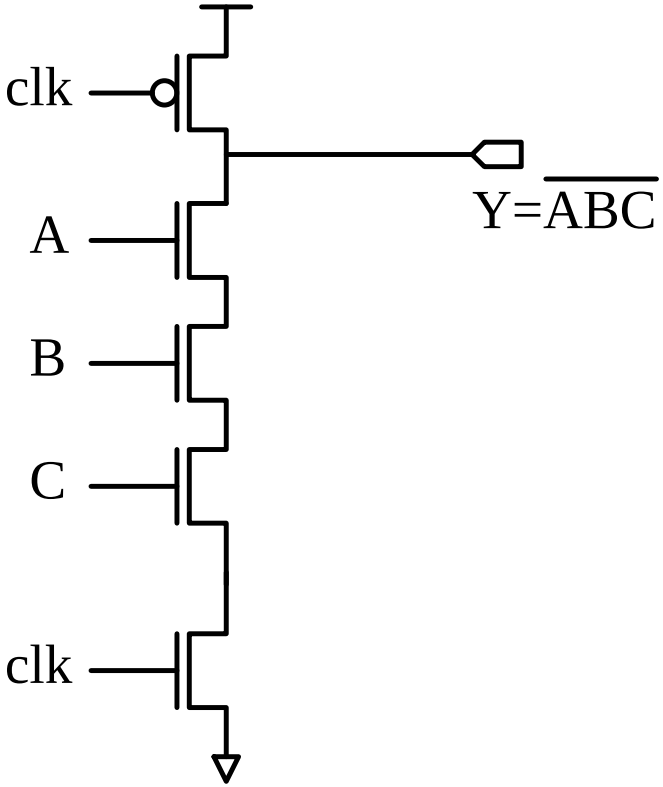


- Two-phase operation: precharge & evaluate
- This can fully eliminate static power dissipation

Examples of Dynamic Logic

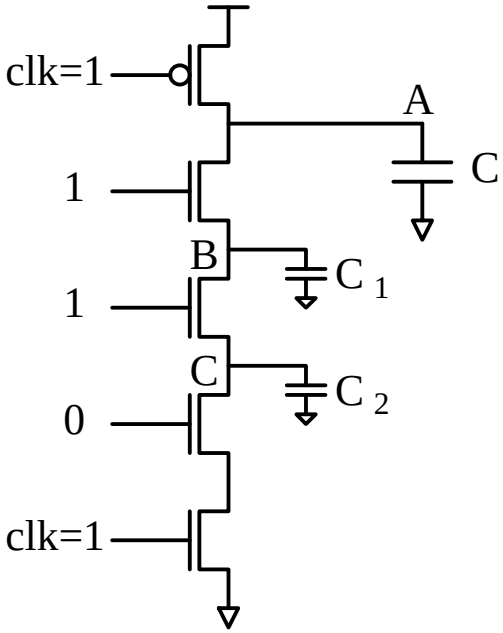
- Two examples

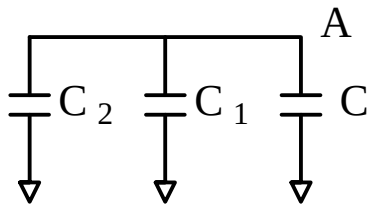




Problems of Dynamic Logic

- Two major problems of dynamic logic
  - Charge sharing
  - Simple single-phase dynamic logic can not be cascaded
- Charge sharing





charge sharing model

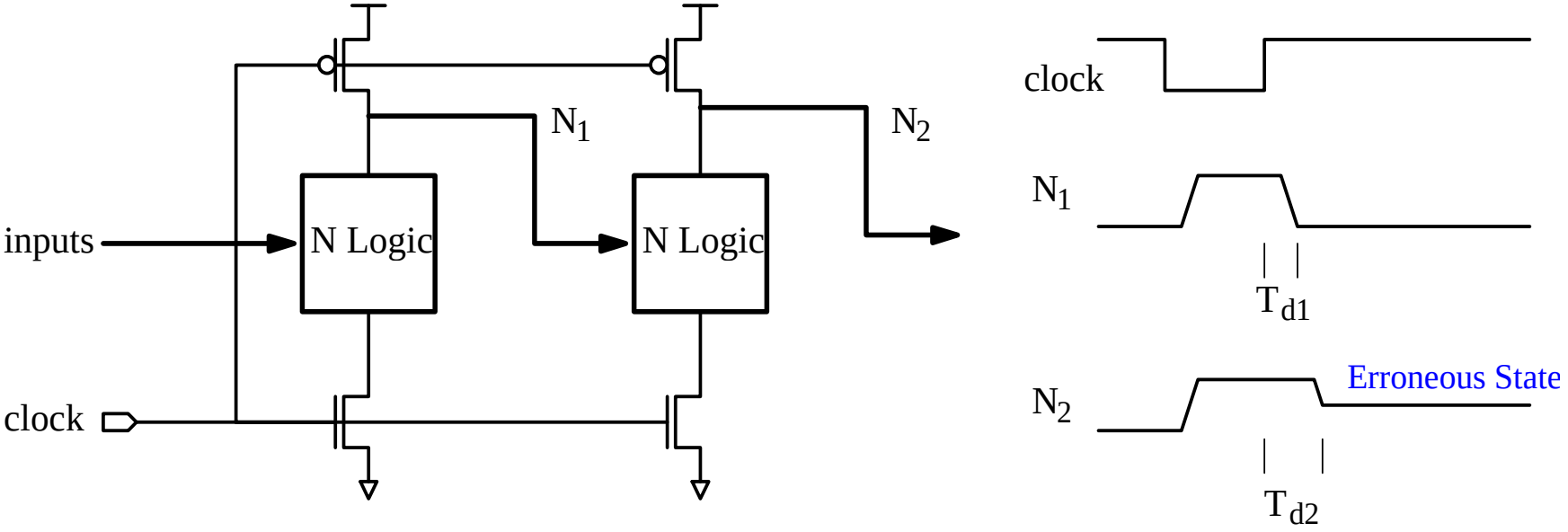
$$CV_{DD} = (C + C_1 + C_2)V_A$$

$$V_A = \frac{C}{C + C_1 + C_2} V_{DD}$$

E.g., if $C_1 = C_2 = 0.5C$ then output voltage is $V_{DD}/2$

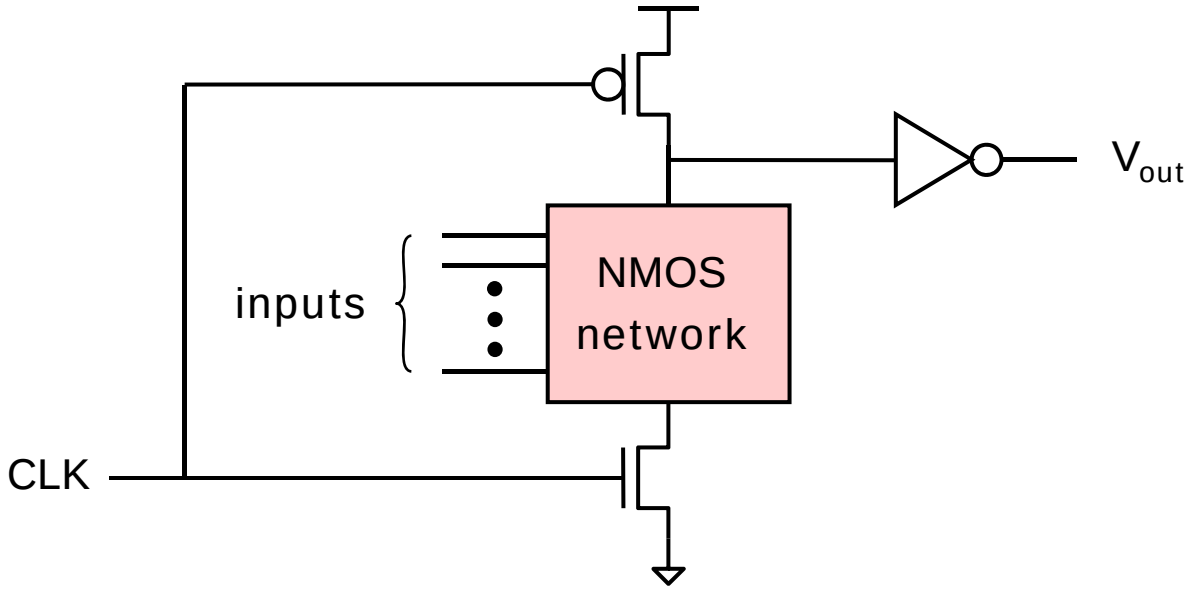
Problems of Dynamic Logic

- Simple single-phase dynamic logic can not be cascaded



CMOS Domino Logic

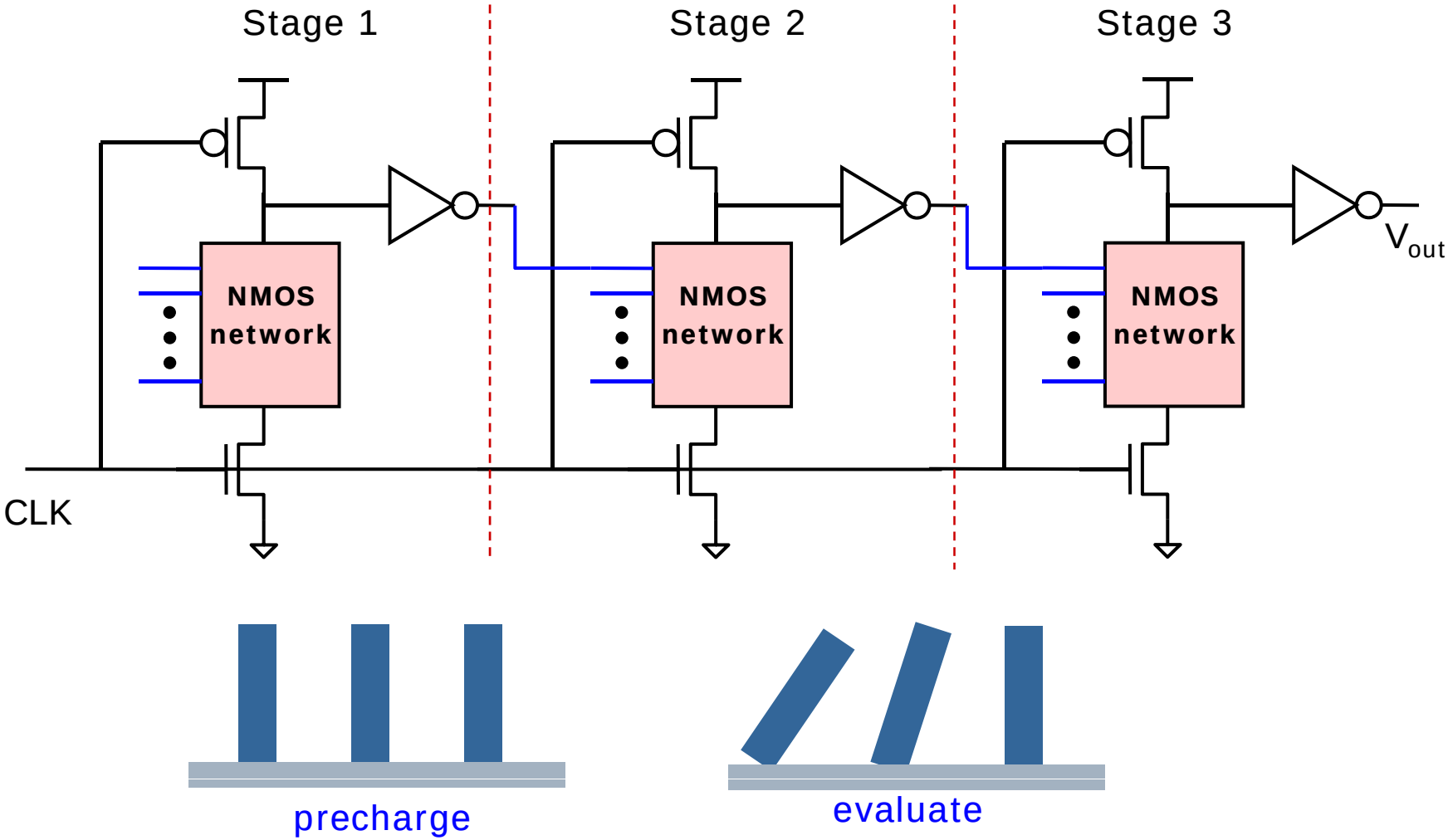
- Domino logic can be cascaded
- The basic structure of domino logic



- Some limitations of this structure
  - Each gate must be buffered
  - Only noninverting structures are possible

A Domino Cascade

- An example of cascaded domino logics

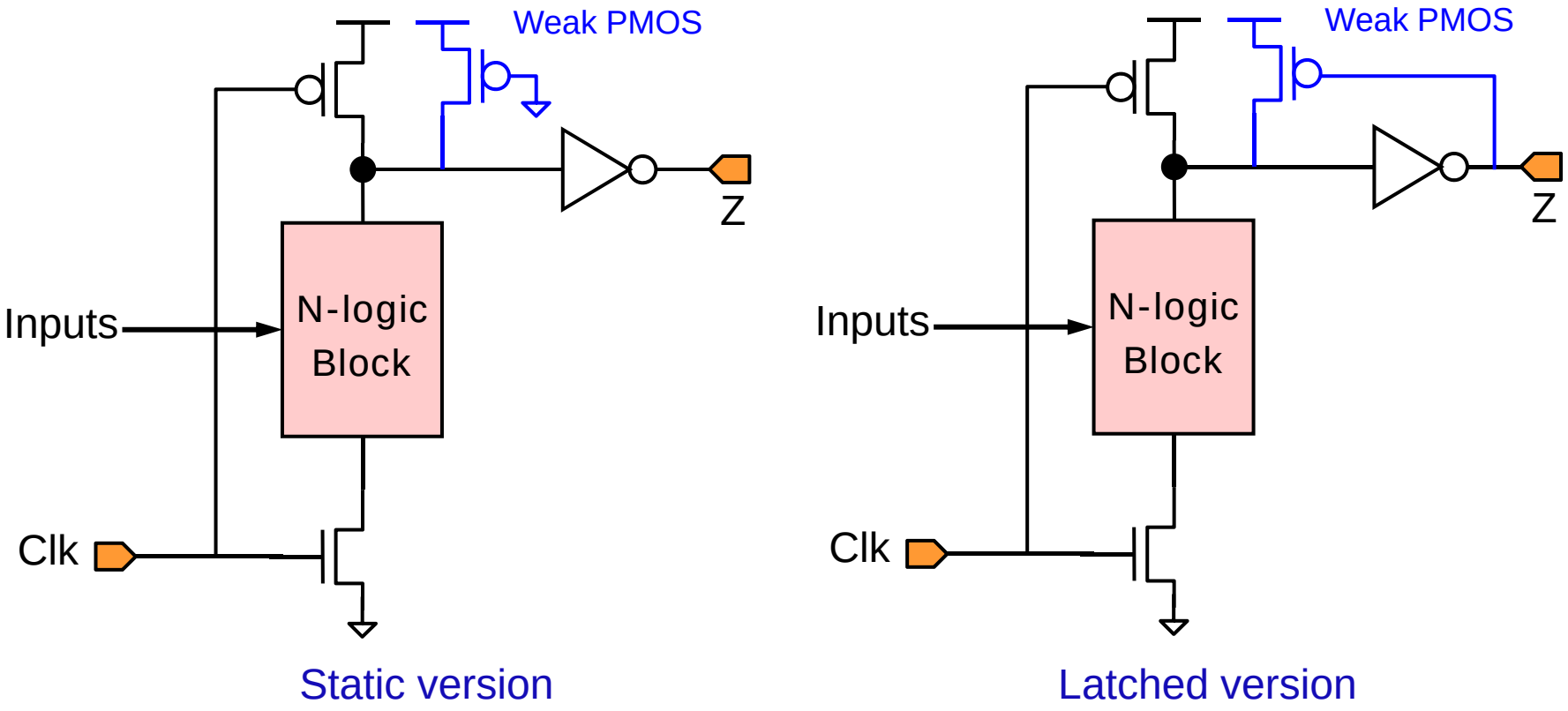


Charge-Keeper Circuits

- The domino cascade must have an evaluation interval that is long enough to allow every stage time to discharge
  - This means that charge sharing and charge leakage processes that reduce the internal voltage may be limiting factors
- Two types of modified domino logics can cope with this problem
  - Static version
  - Latched version

Charge-Keeper Circuits

- Modified domino logics



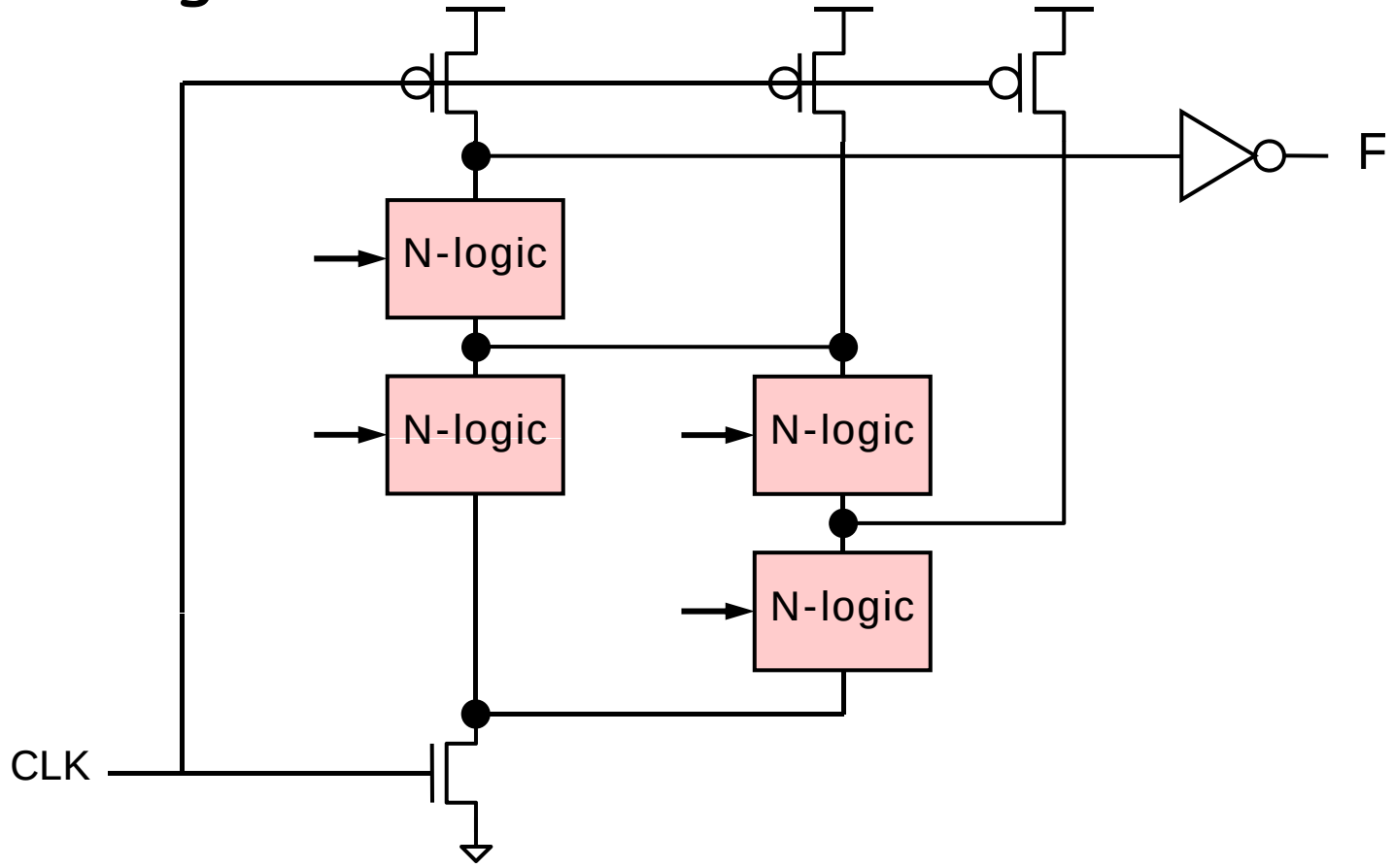
Static version

Latched version

- The aspect ratio of the charge-keeper MOS must be small so that it does not interfere with discharge event

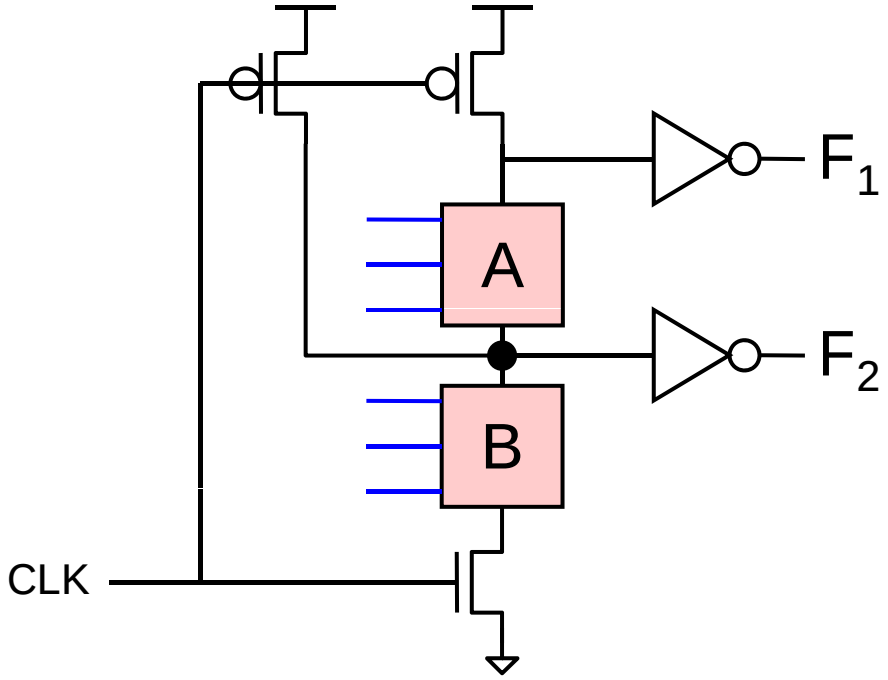
Complex Domino Gate

- In a complex domino gate, intermediate nodes have been provided with their own precharge transistor

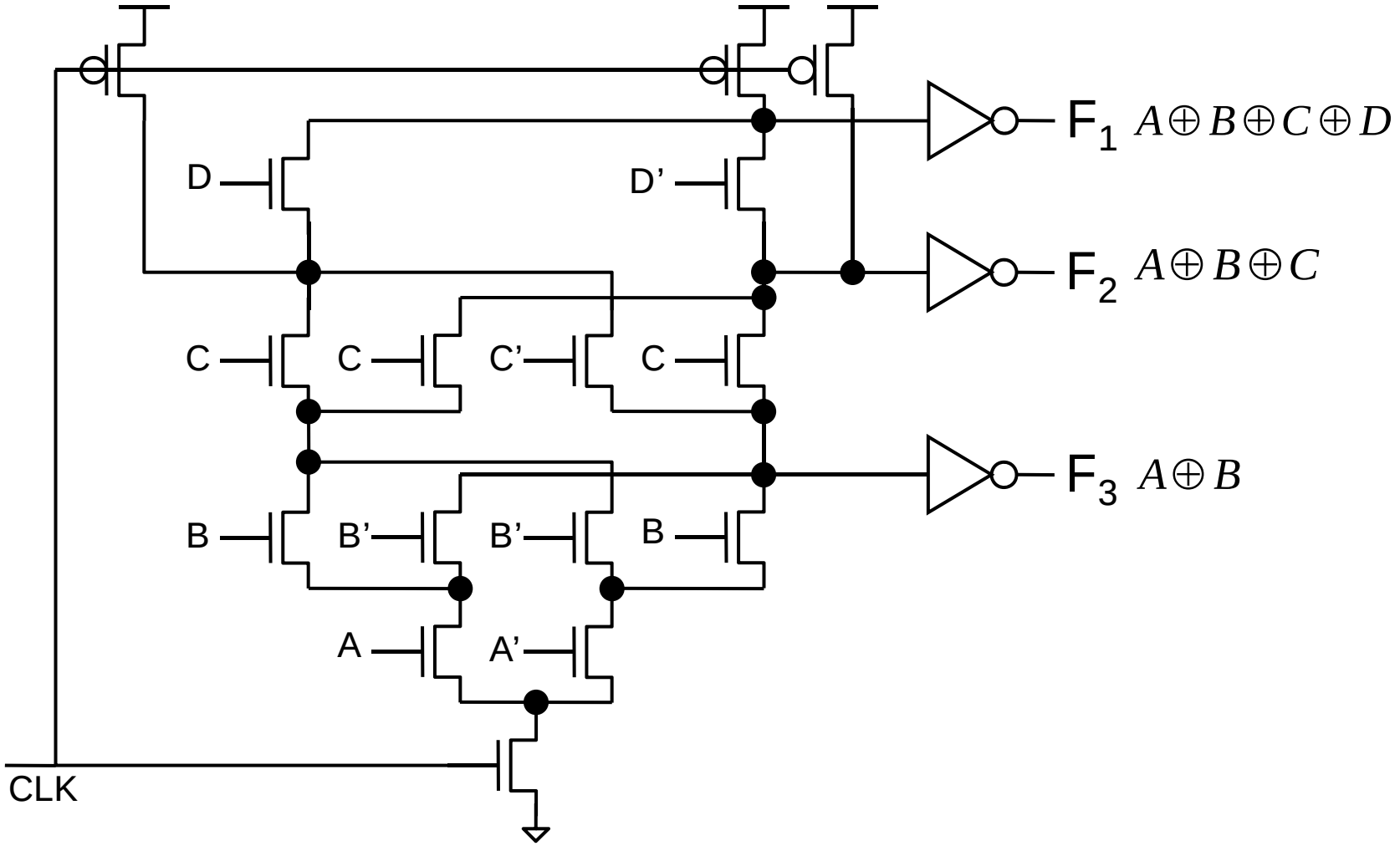


Multiple-Output Domino Logic

- Multiple-output domino logic (MODL) allows two or more outputs from a single logic gate
- The basic structure of MODL

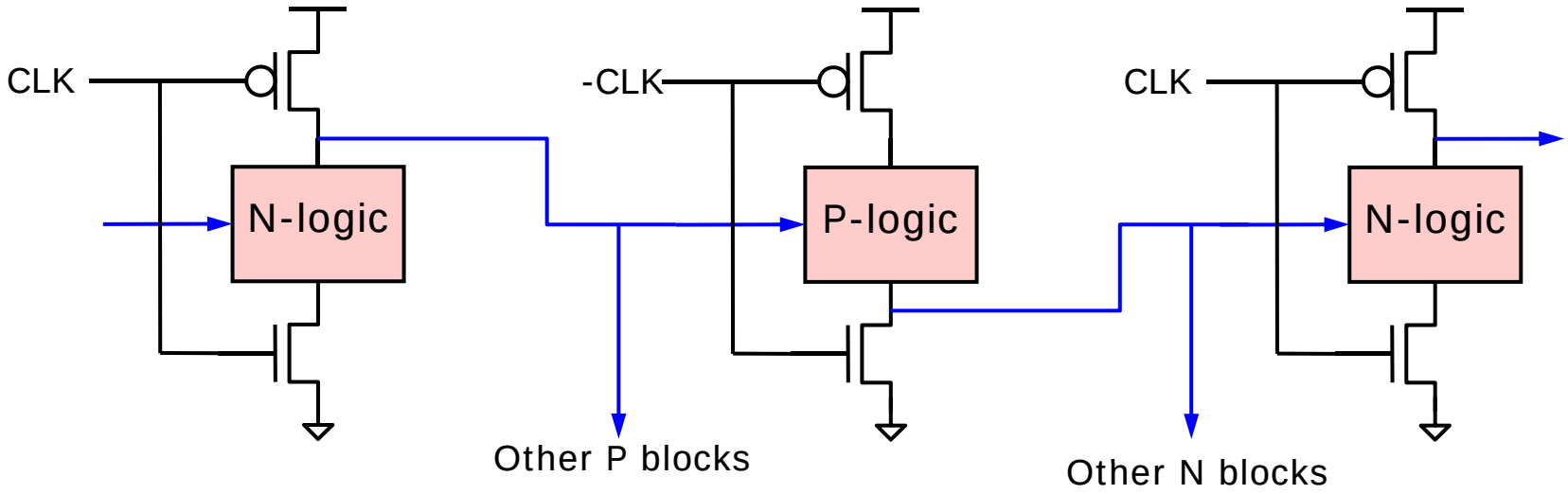


A Multiple-Output Domino Logic Gate



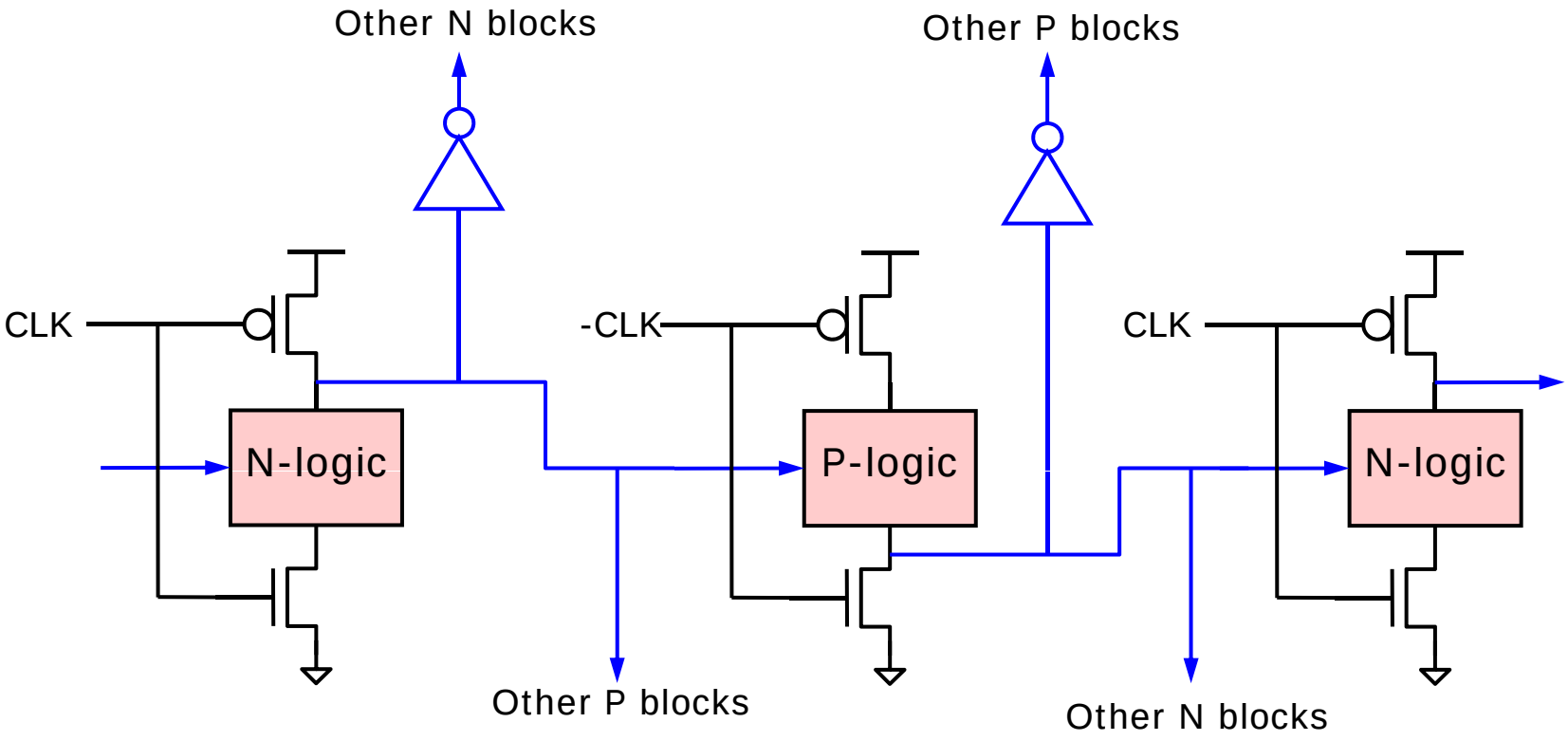
NP Domino Logic

- A further refinement of the domino logic is shown below
  - The domino buffer is removed, while cascaded logic blocks are alternately composed of P- and N-transistors



NP Domino Logic

- NP domino logic with multiple fanouts

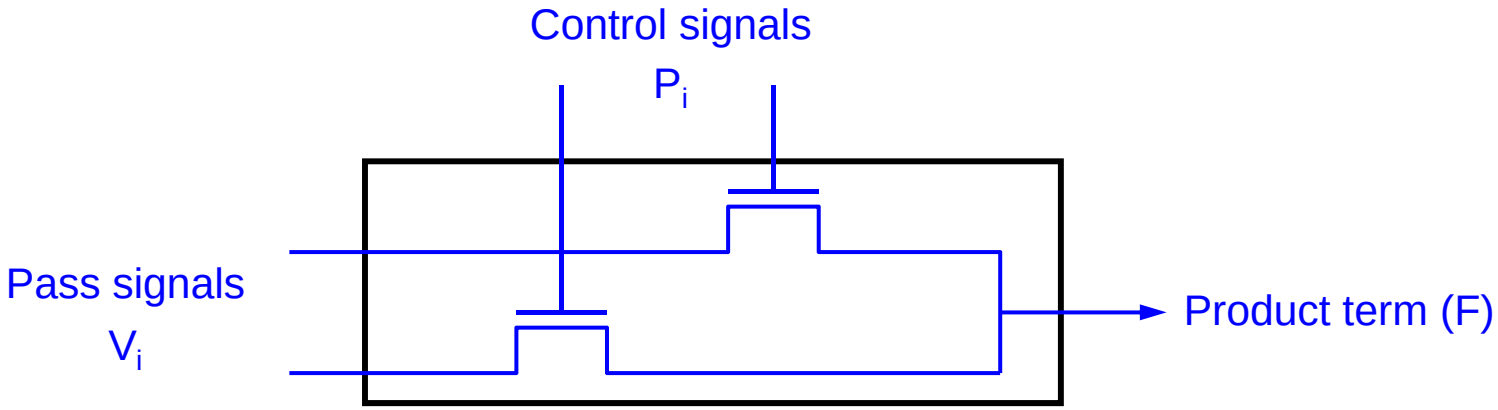


Advanced CMOS Logic Design

- Pass-Transistor Logic

Pass-Transistor Logic

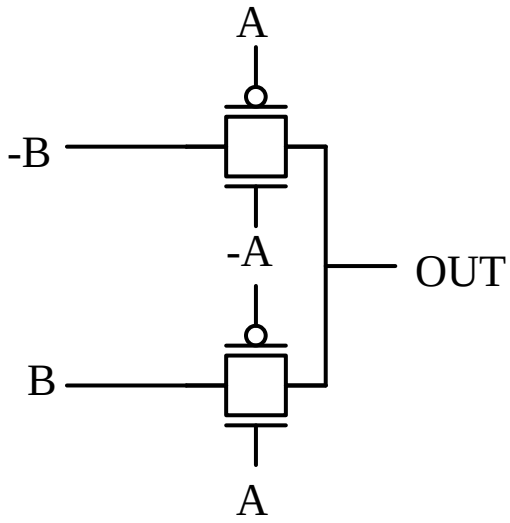
- Model for pass transistor logic



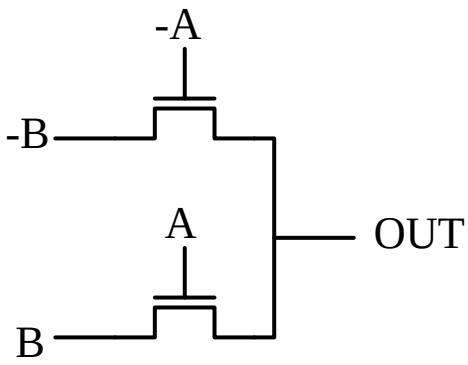
- The product term
  - $F=P_1V_1+P_2V_2+...+P_nV_n$
  - The pass variables can take the values $\{0,1,X_i,-X_i,Z\}$, where X_i and $-X_i$ are the true and complement of the ith input variable and Z is the high-impedance

Pass-Transistor Logics

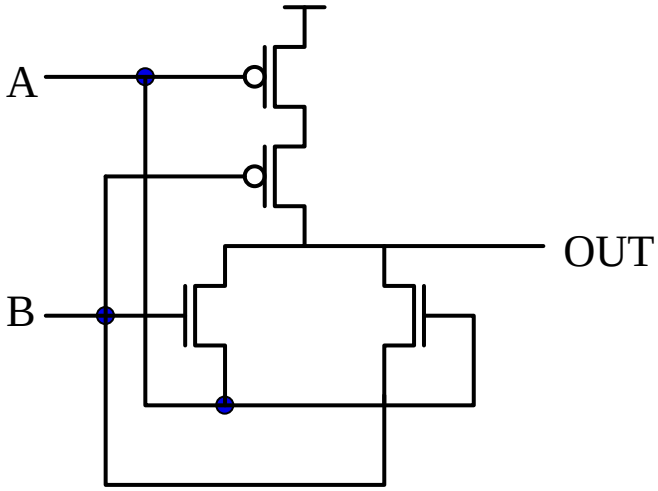
- Different types of pass-transistor logics for two-input XNOR gate implementation



Complementary



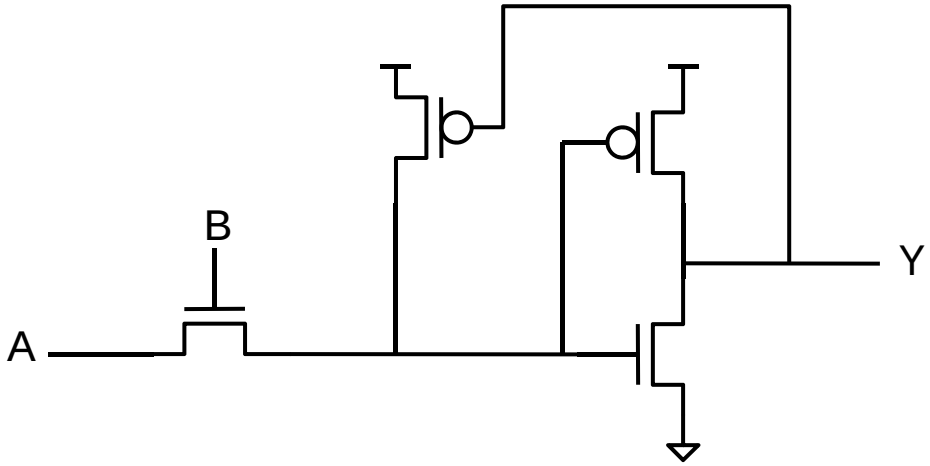
Single-polarity



Cross-coupled

Full-Swing Pass-Transistor Logic

- Modifying NMOS pass-transistor logic so full-level swings are realized



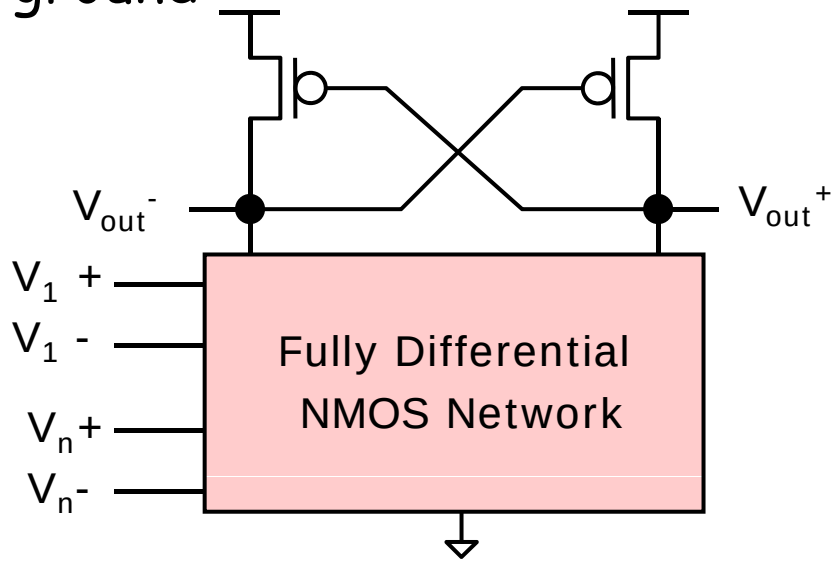
- Adding the additional PMOS has another advantages
  - It adds hysteresis to the inverter, which makes it less likely to have glitches

Differential Logic Design

- Features of the differential logic design
  - Logic inversions are trivially obtained by simply interchanging wires without incurring a time delay
  - The load networks will often consist of two cross-coupled PMOS only. This minimizes both area and the number of series PMOS transistors
- Disadvantage
  - Two wires must be used to represent every signal, the interconnect area can be significantly greater. In applications in which only a few close gates are being driven, this disadvantage is often not as significant as the advantages
- Thus differential logic circuits are often a preferable consideration

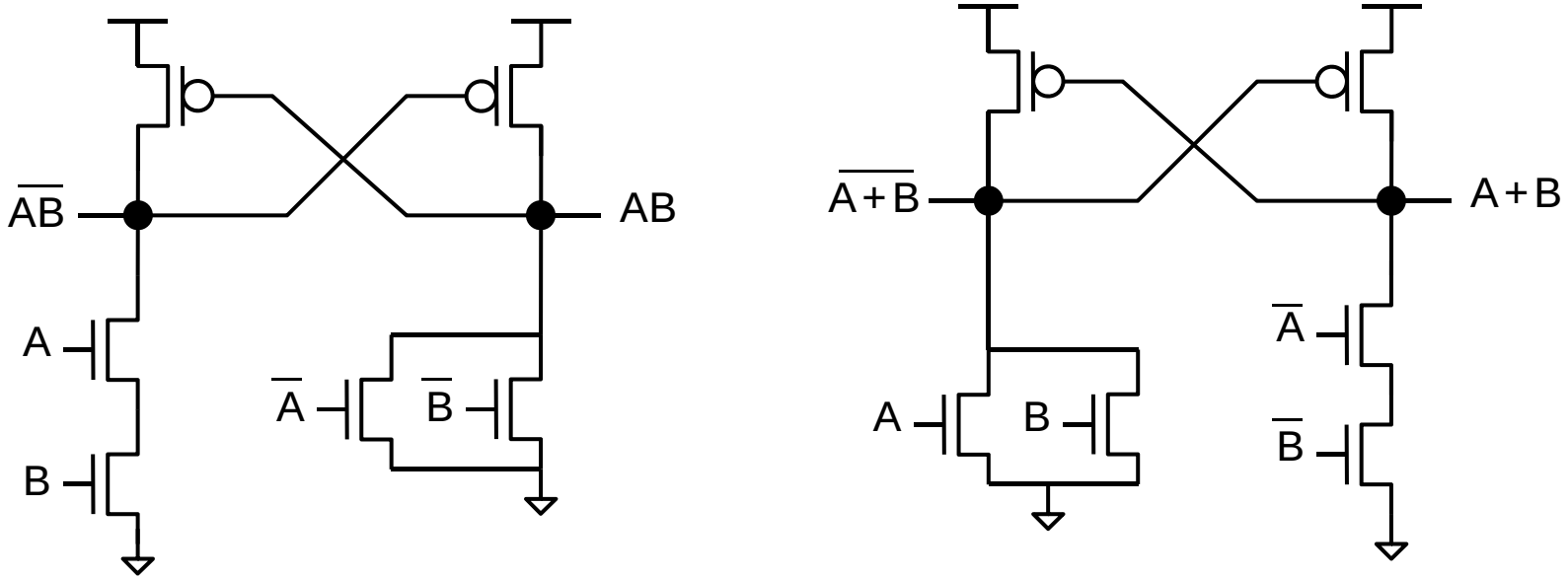
A Fully Differential Logic Circuit

- One simple and popular approach for realizing differential logic circuit is shown below
  - The inputs to the drive network come in pairs, a single-ended signal and its inverse
  - The NMOS network can be divided into two separate networks, one between the inverting output and ground, and a complementary network between the noninverting output and ground



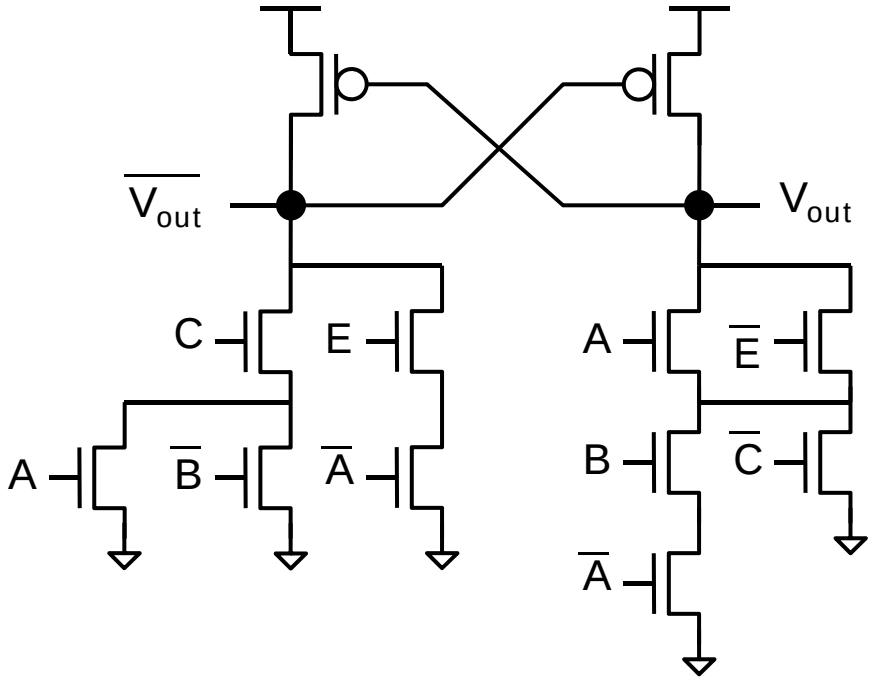
Examples

- Differential CMOS realizations of AND and OR functions



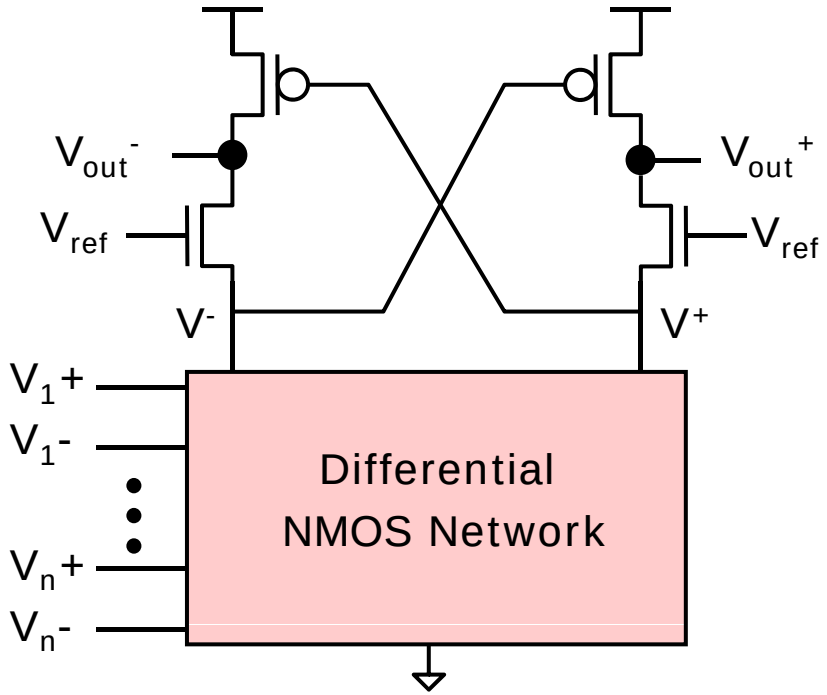
Examples

- Differential CMOS realization of the function $V_{out}=(A+B')C+A'E$



Differential Split-Level Logic

- Differential split-level (DSL) logic
  - A variation of fully differential logic
  - A compromise between a cross-coupled load with no d.c. power dissipation and a continuously-on load with d.c. power dissipation

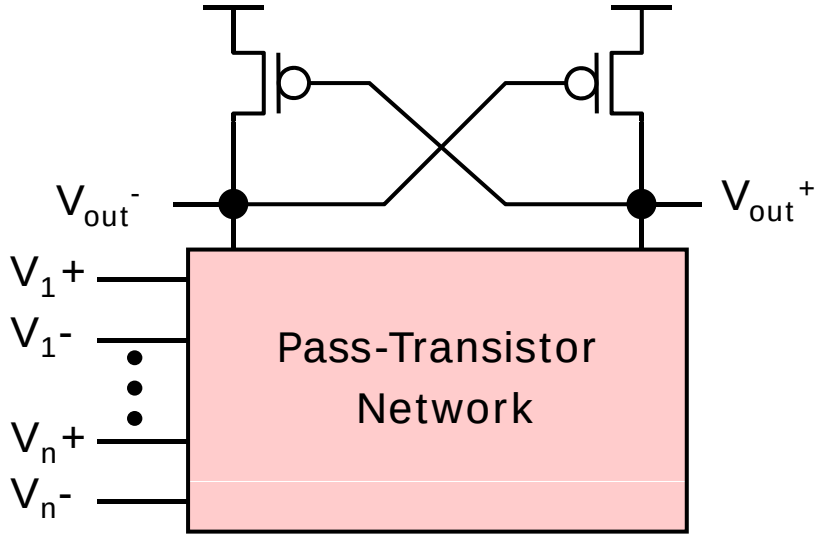


Differential Split-Level Logic

- Features of DSL logic
  - The loads have some of the features of both continuous loads and cross-coupled load
    - Both outputs begin to change immediately
    - The loads do have d.c. power dissipation, but normally much less than pseudo-NMOS gates and dynamic power dissipation
  - The nodes V+, V-, and all internal nodes of the NMOS network have voltage changes between greater than 0V and V_{ref}-V_{tn}
    - This reduced voltage swing increases the speed of the logic gates
  - The maximum drain-source voltage across the NMOS transistors is reduced by about one-half
    - This greatly minimizes the short-channel effects

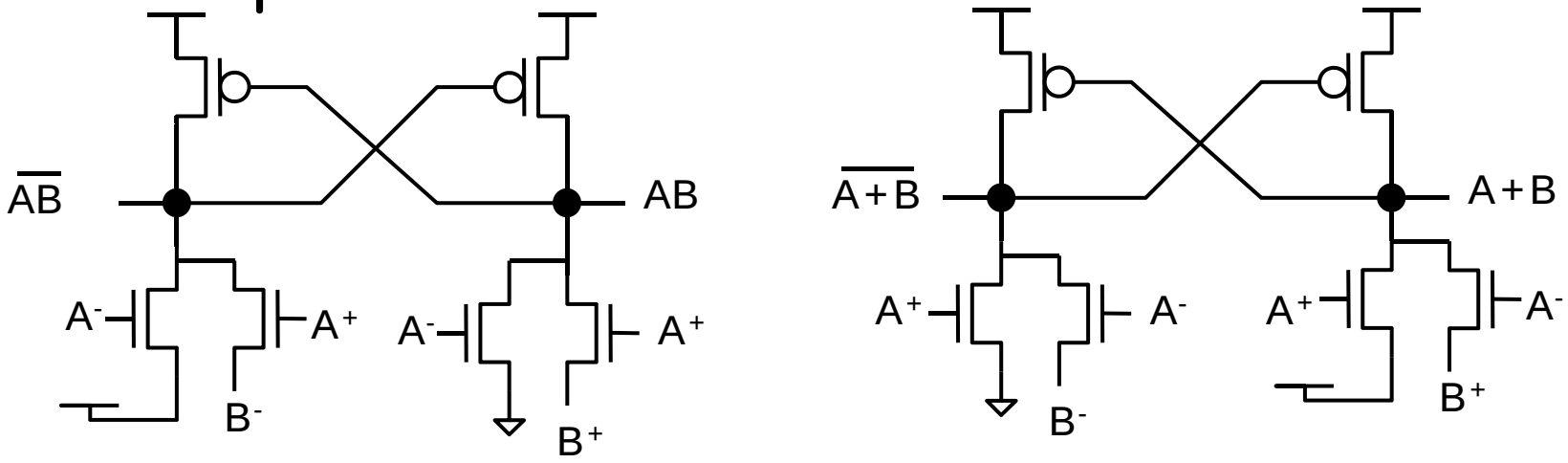
Differential Pass-Transistor Logic

- It is not necessary to wait until one side goes to low before the other side goes high
  - Pass-transistor networks for most required logic functions exist in which both sides of the cross-coupled loads are driven simultaneously
  - This minimizes the time from when the inputs changes to when the low-to-high transition occurs



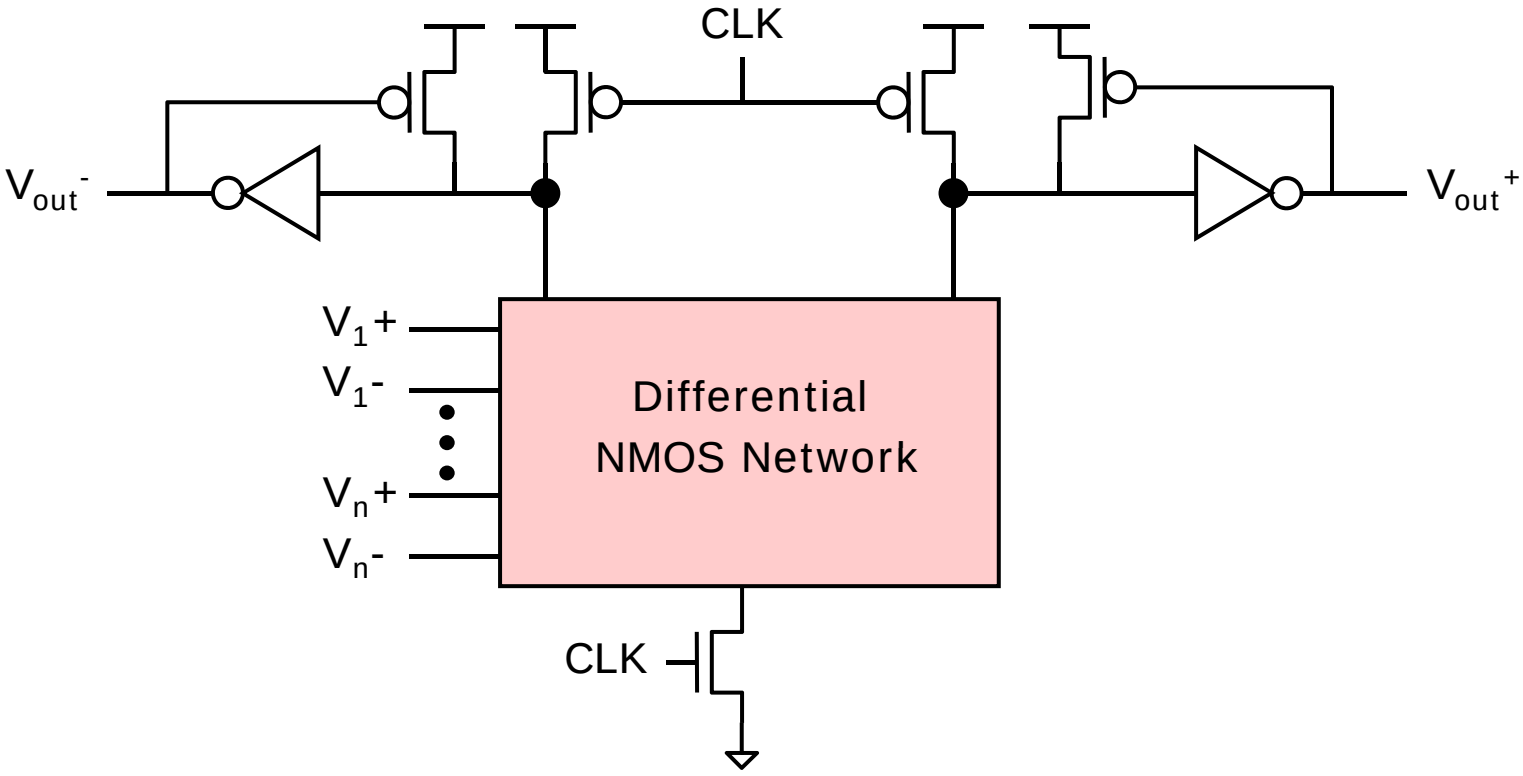
Differential Pass-Transistor Logic

- Other features of pass-transistor logic
  - It removes the ratio requirements on the logic and has guaranteed functionality
  - The cross-coupled loads restore signal levels to full V_{dd} levels, thereby eliminating the voltage drop
- Examples:



Dynamic Differential Logic

- A differential Domino logic gate

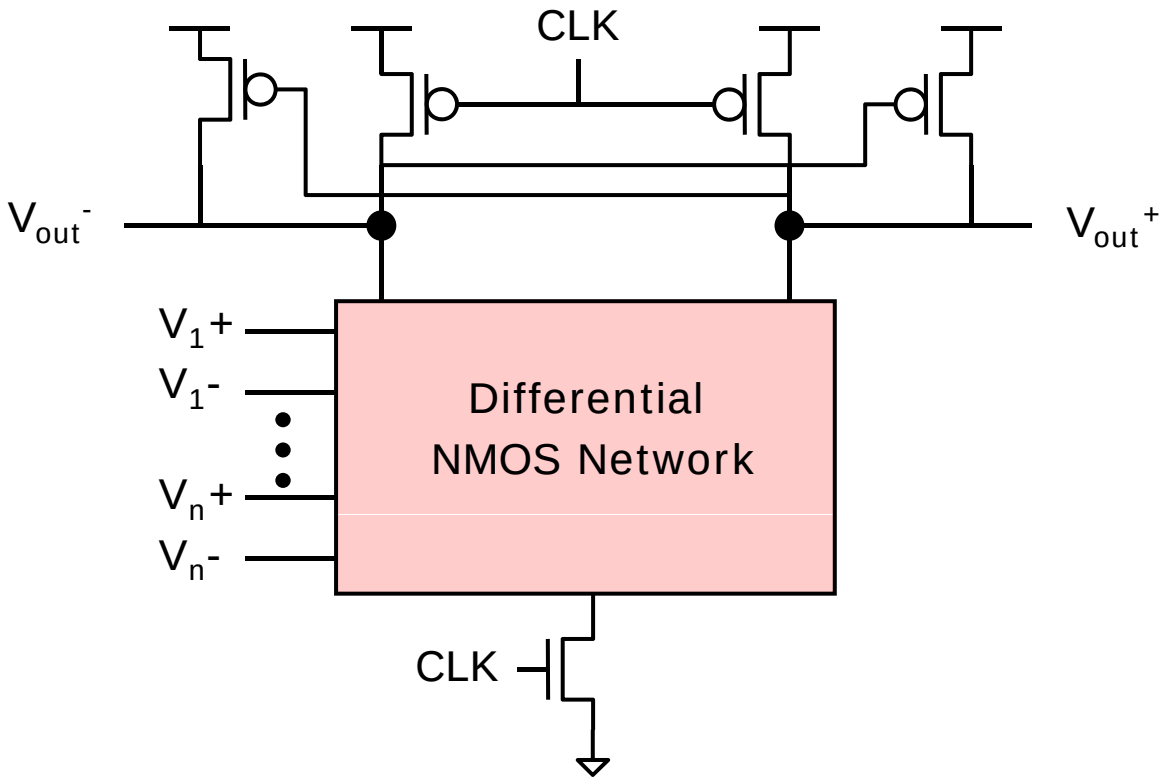


Dynamic Differential Logic

- Features of dynamic Domino logic
  - Its d.c. power dissipation is very small, whereas its its speed still quite good
  - Because of the buffers at the output, its output drive capability is also very good
  - One of major limitations of Domino logic, the difficulty in realizing inverting functions, is eliminated because of the differential nature of the circuits

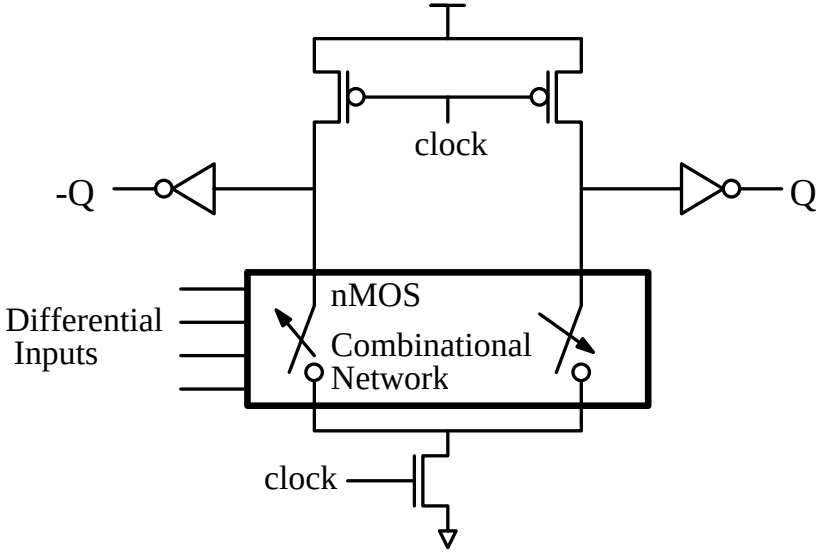
Dynamic Differential Logic

- When the fan-out is small, the inverters at the output can be eliminated and the inputs to the charge-keeper transistors can be taken from the opposite output



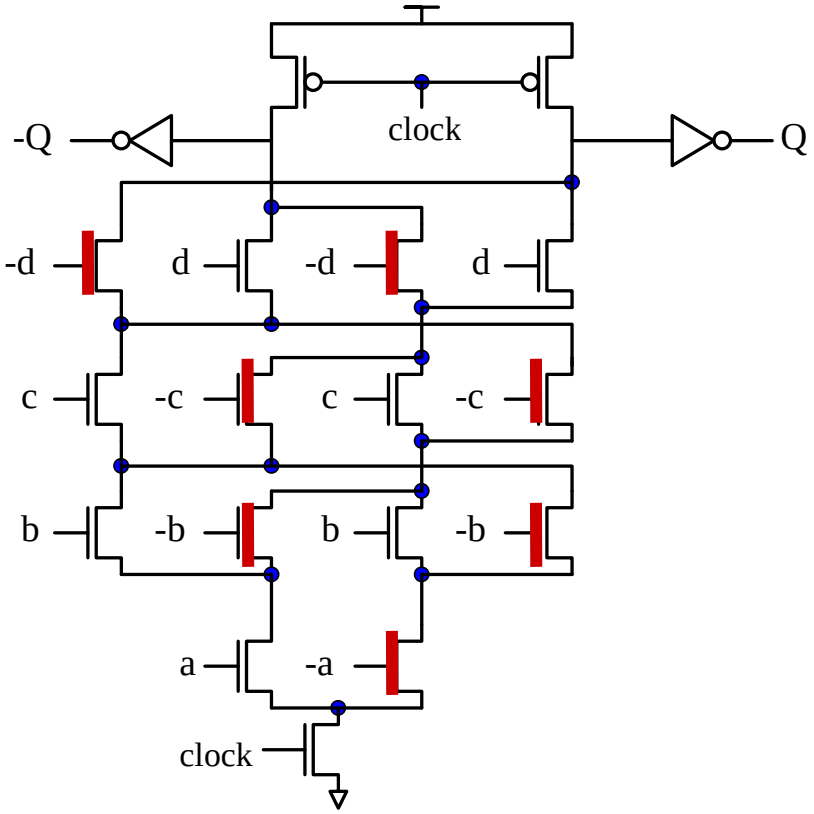
Dynamic Differential Logic

- Dynamic differential logics without charge-keeper circuit



Clocked version

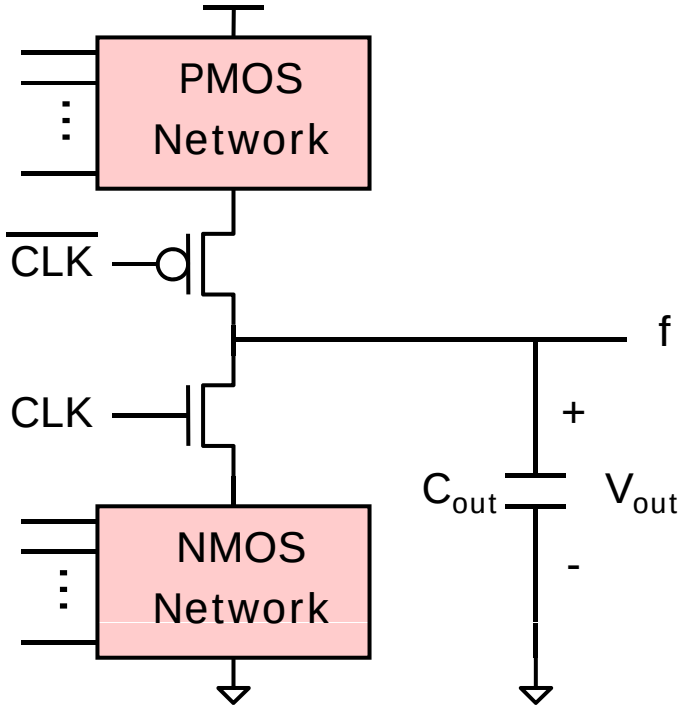
(abcd)=(0000)



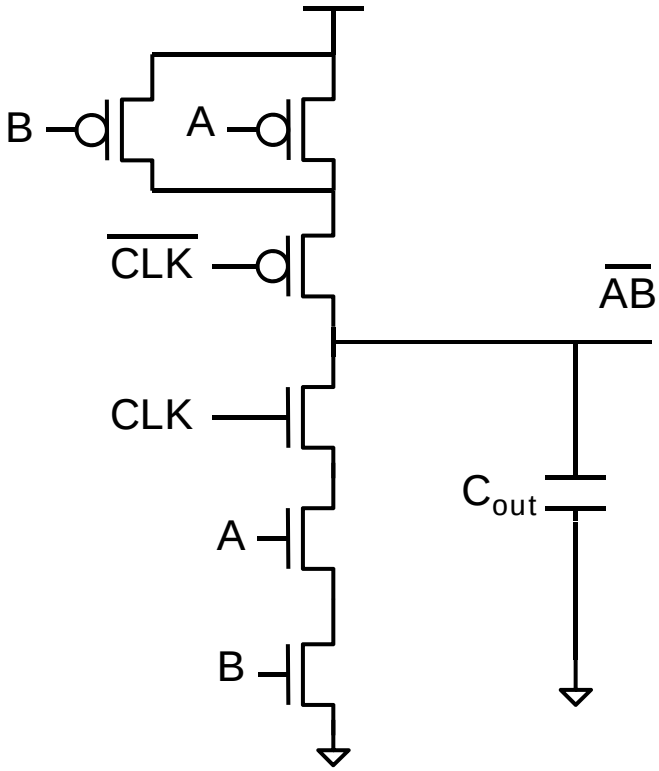
A 4-way XOR gate

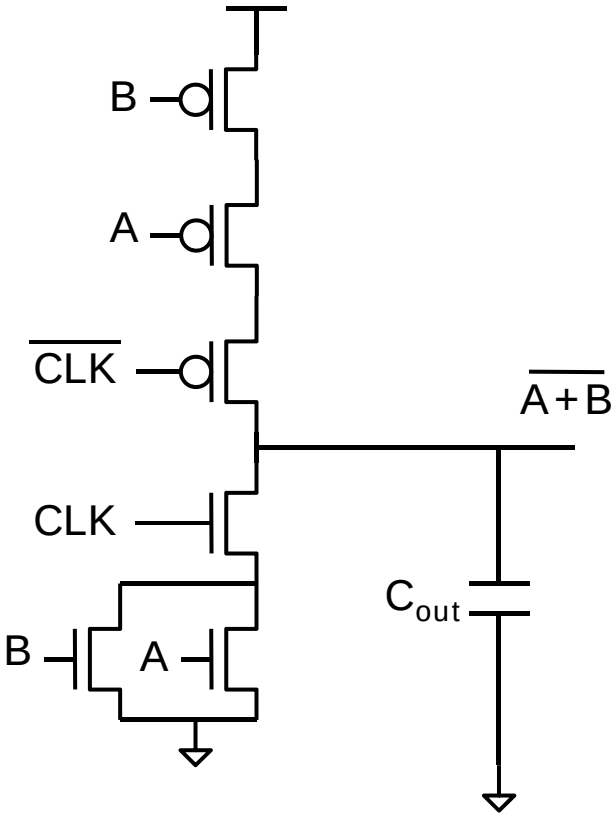
Clocked CMOS (C^2MOS)

- Structure of a C^2MOS gate
  - Ideally, clocks are non-overlapping → $\overline{CLK}$ X CLK = 0
  - CLK=1, f is valid
  - CLK=0, the output is in a high-impedance state. During this time interval, the output voltage is held on C_{out}



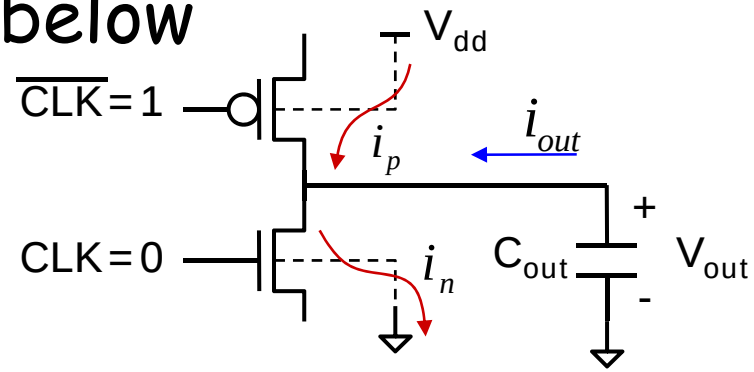
Examples of C²MOS Logic Gates

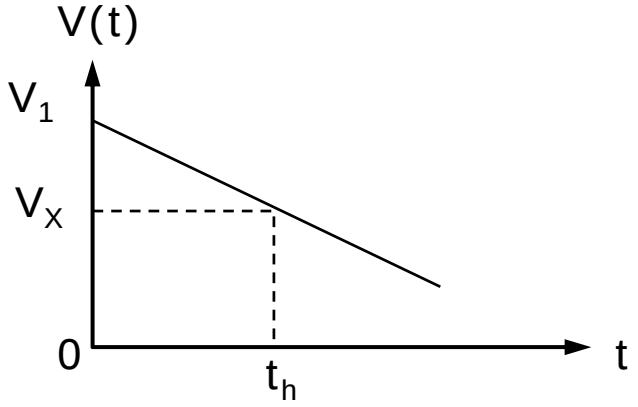




Gates

- The problem of charge leakage
  - Cause that the output node cannot hold the charge on V_{out} very long
- The basics of charge leakage are shown below





$$i_{out} = i_n - i_p = -C_{out}\frac{dV}{dt}$$

$$\Rightarrow dV = -\frac{i_{out}}{C_{out}}dt$$

Assume i_{out} is a constant I_L

$$\int_{V_1}^{V(t)} dV = -\int_0^t \frac{I_L}{C_{out}}dt \Rightarrow V(t) = V_1 - \frac{I_L}{C_{out}}t$$

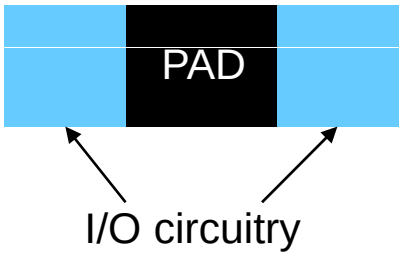
$$V(t_h) = V_1 - \frac{I_L}{C_{out}}t_h = V_X$$

$$\Rightarrow t_h = \frac{C_{out}}{I_L}(V_1 - V_X)$$

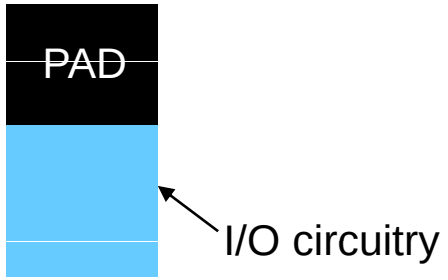
I/O Pads

- Types of pads
  - V_{dd}, V_{ss} pad
  - Input pad (ESD)
  - Output pad (driver)
  - I/O pad (ESD+driver)
- All pads need guard ring for latch-up protection
- Core-limited pad & pad-limited pad

Core-limited pad

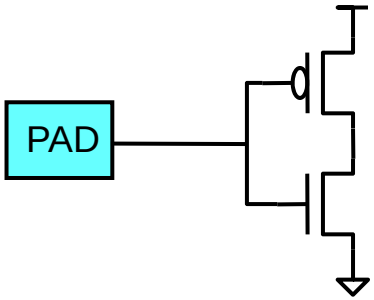


Pad-limited pad



ESD Protection

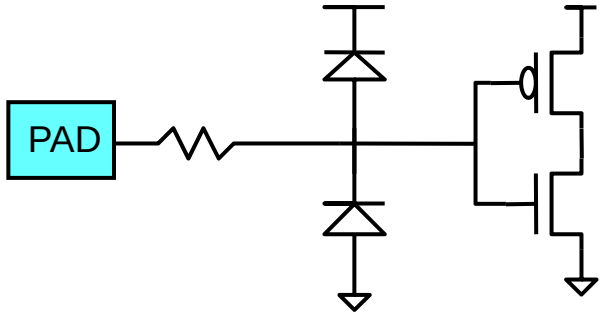
- Input pad without *electrostatic discharge* (ESD) protection



Assume I=10uA, C_g=0.03pF, and t=1us

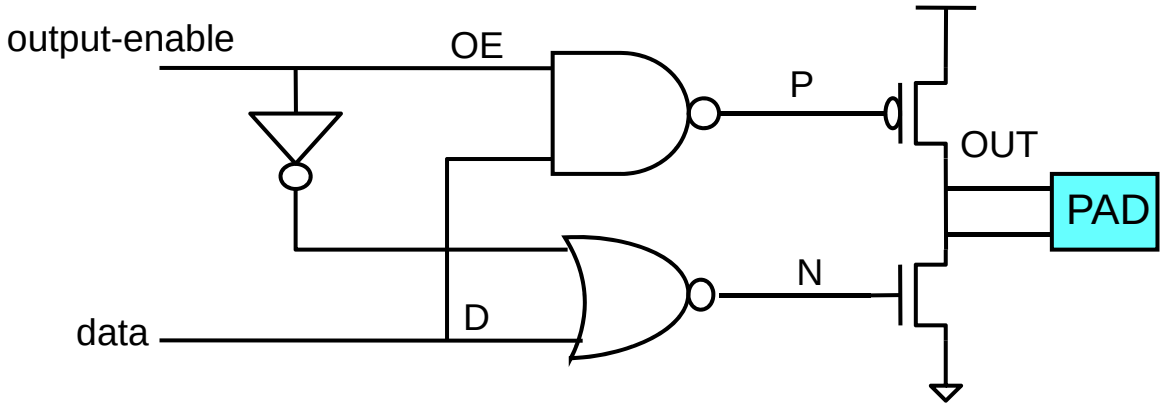
The voltage that appears on the gate is about 330volts

- Input pad with ESD protection



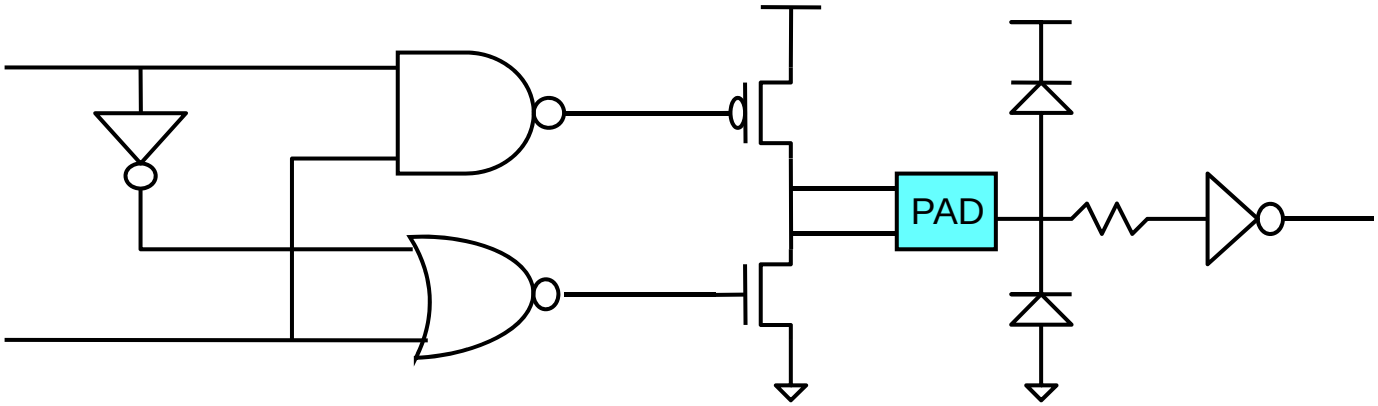
Tristate & Bidirectional Pads

- Tristate pad



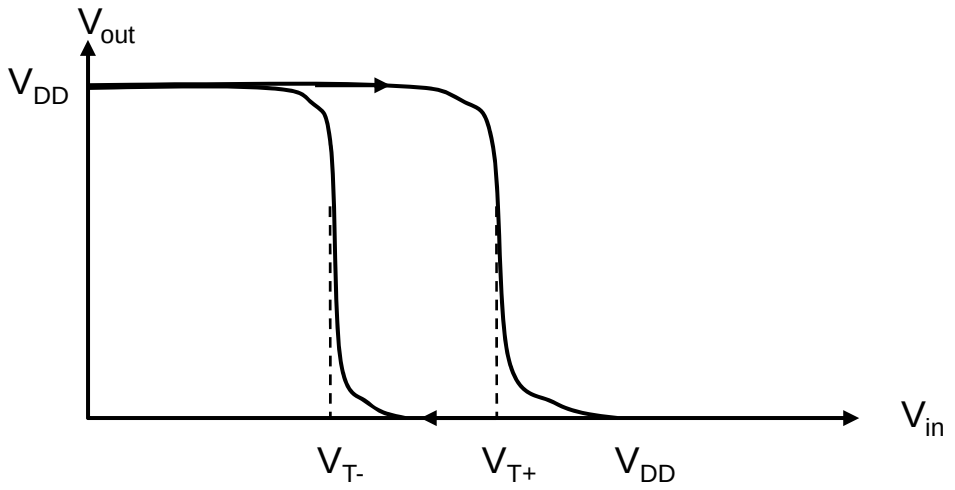
OE	D	N	P	OUT
0	X	0	1	Z
1	0	1	1	0
1	1	0	0	1

- Bidirectional pad



Schmitt Trigger Circuit

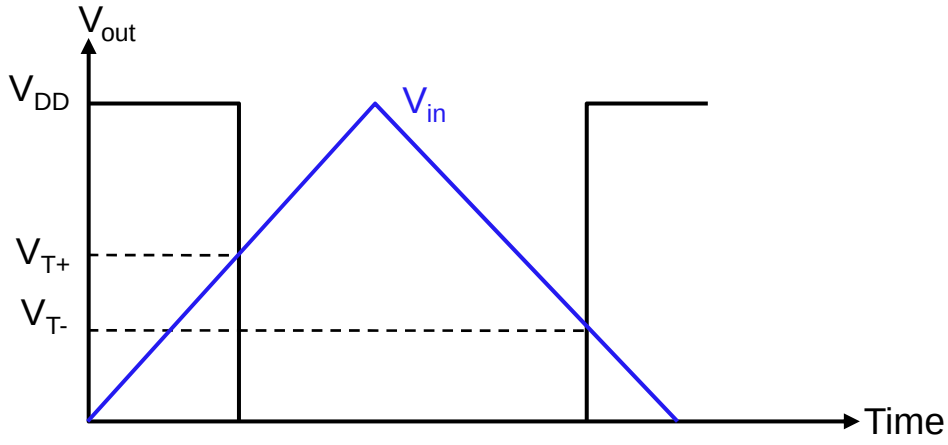
- Voltage transfer curve of Schmitt circuit



  - Hysteresis voltage $V_H=V_{T+}-V_{T-}$
  - When the input is rising, it switches when $V_{in}=V_{T+}$
  - When the input is falling, it switches when $V_{in}=V_{T-}$

Schmitt Trigger Circuit

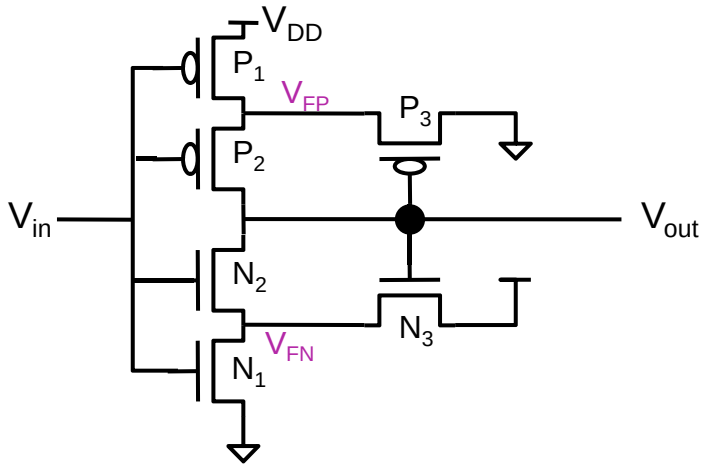
- Voltage waveform for slow input



- Schmitt trigger turns a signal with a very slow transition into a signal with a sharp transition

Schmitt Trigger Circuit

- A CMOS version of the Schmitt trigger circuit



- When the input is rising, the V_{GS} of the transistor N_2 is given by $V_{GS2}=V_{in}-V_{FN}$
- When $V_{in}=V_{T+}$, N_2 enters in conduction mode which means $V_{GS2}=V_{Tn}$
- Then $V_{FN}=V_{T+}-V_{Tn}$

Summary

- The following topics have been introduced in this chapter
  - CMOS Logic Gate Design
  - Advanced CMOS Logic Design
  - Clocking Strategies
  - I/O Structures