Chapter 7
Sequential Circuits

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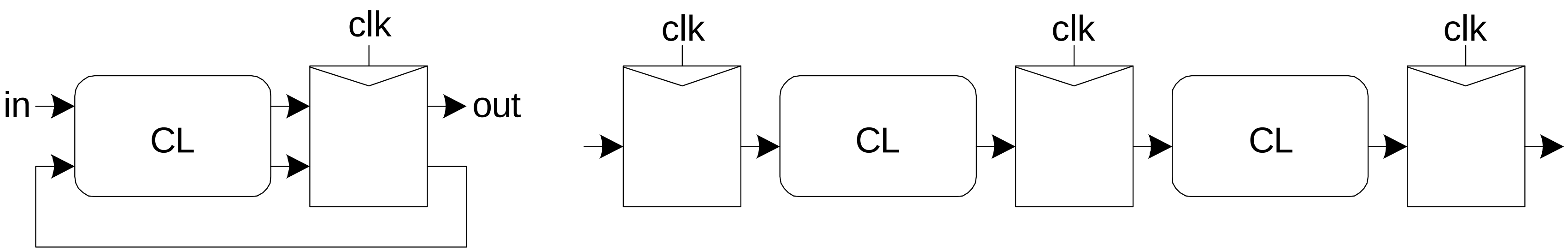
Outline

- Latches & Registers
- Sequencing Timing Diagram

Sequencing

- *Combinational logic*
  - Output depends on current inputs
- *Sequential logic*
  - Output depends on current and previous inputs
  - Requires separating previous, current, future
  - Called *state* or *tokens*
  - Ex: FSM, pipeline

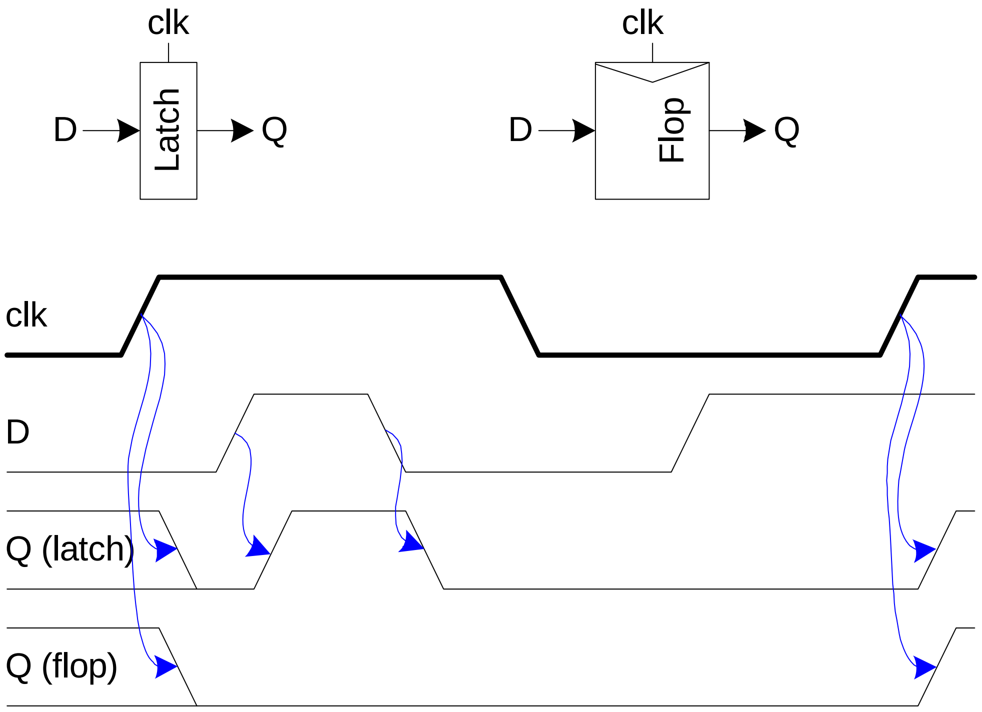


Finite State Machine

Pipeline

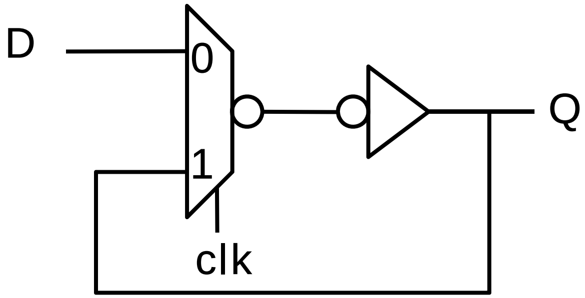
Sequencing Elements

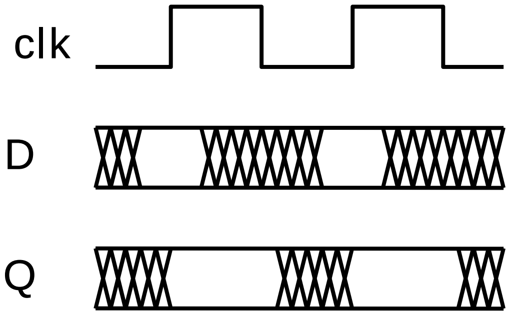
- **Latch**: Level sensitive
  - A.k.a. transparent latch, D latch
- **Flip-flop**: edge triggered
  - A.k.a. master-slave flip-flop, D flip-flop, D register
- Timing Diagrams
  - Transparent
  - Opaque
  - Edge-trigger



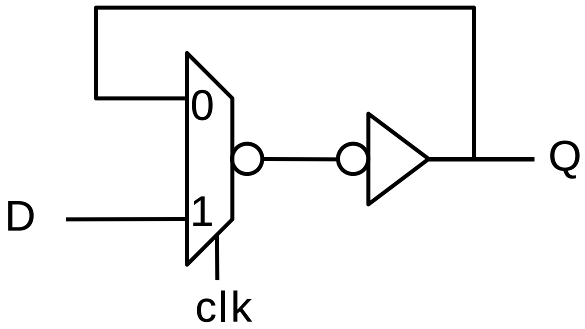
Latches

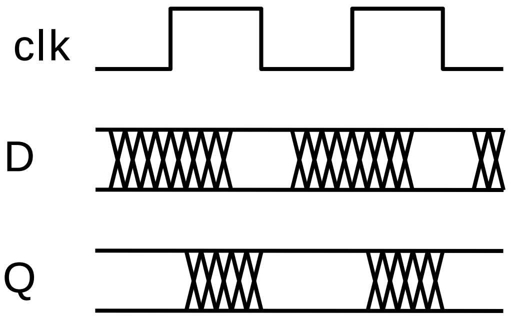
- Negative-level sensitive latch





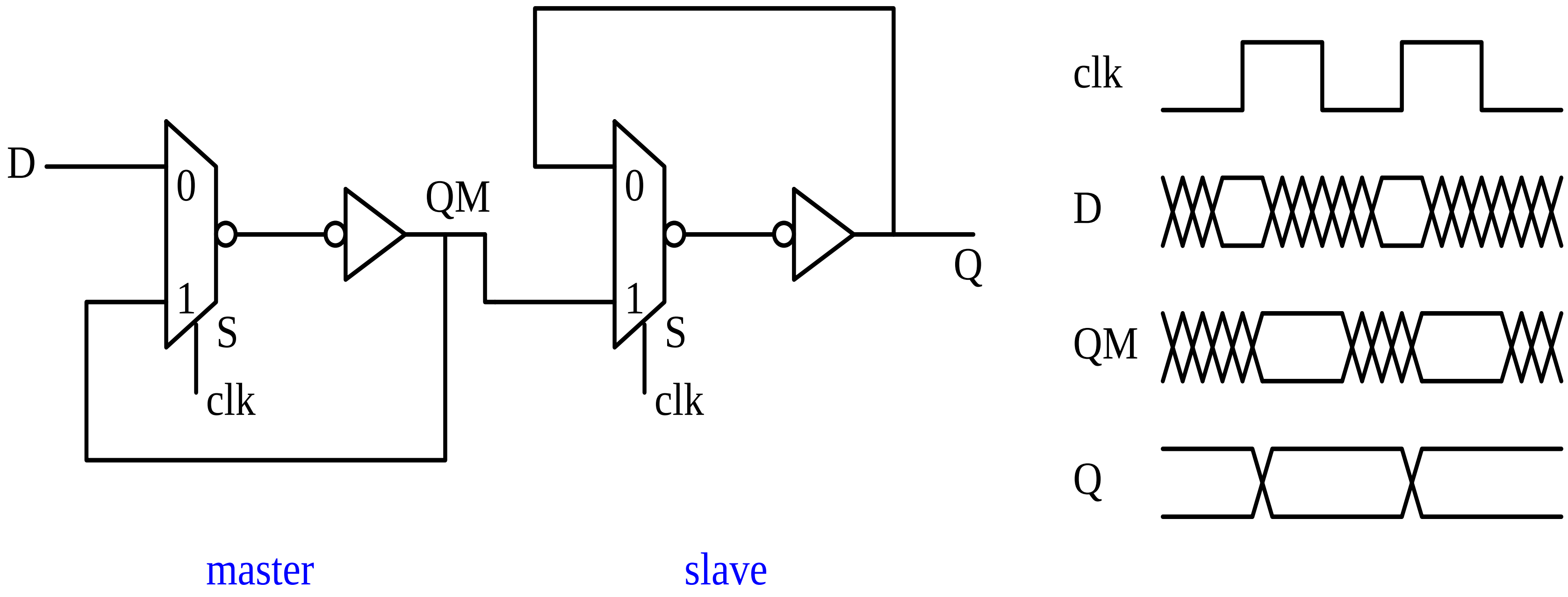
- Positive-level sensitive latch





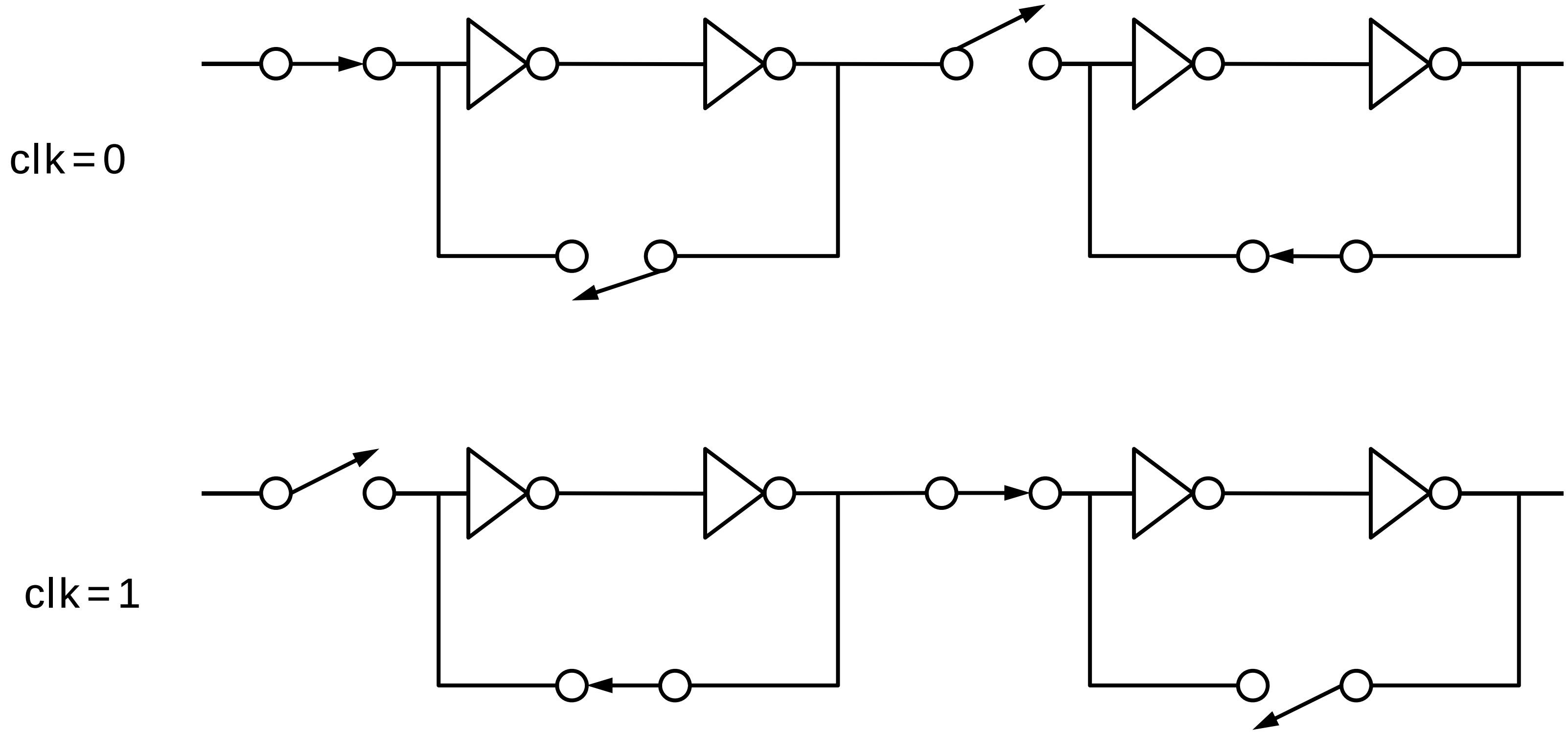
Registers

- Positive-edge triggered register (single-phase clock)



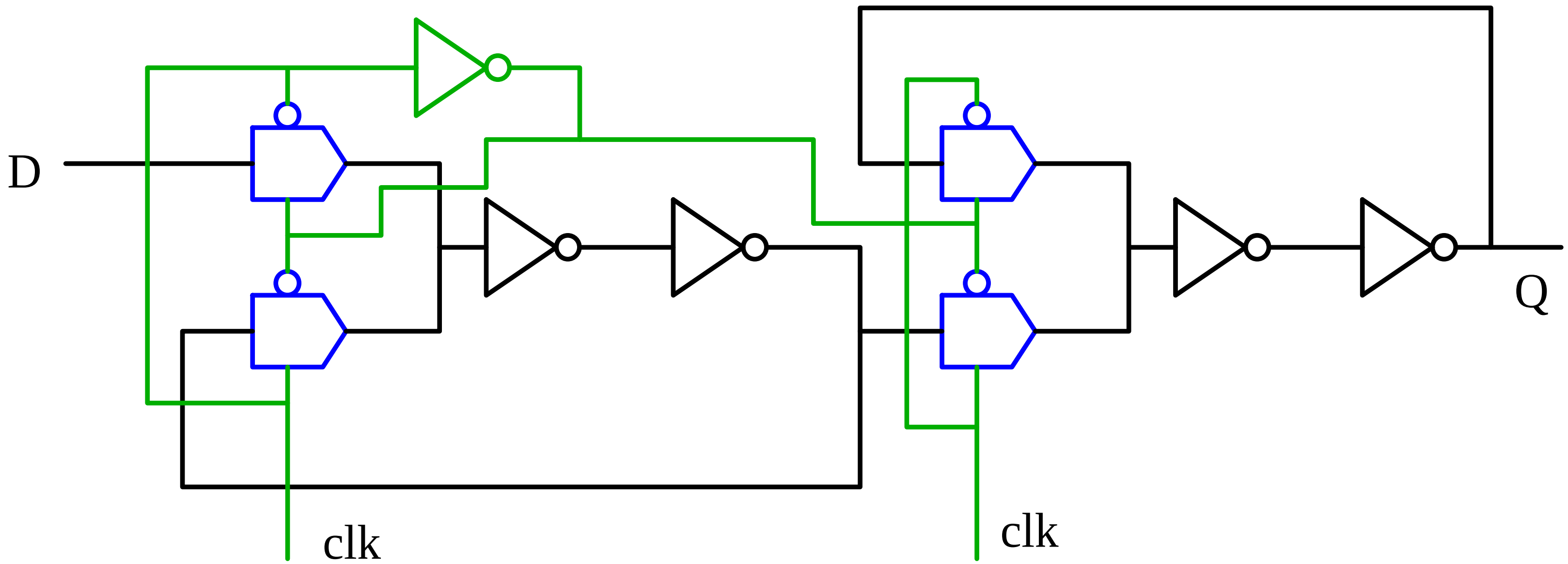
Registers

- Operations of the positive-edge triggered register



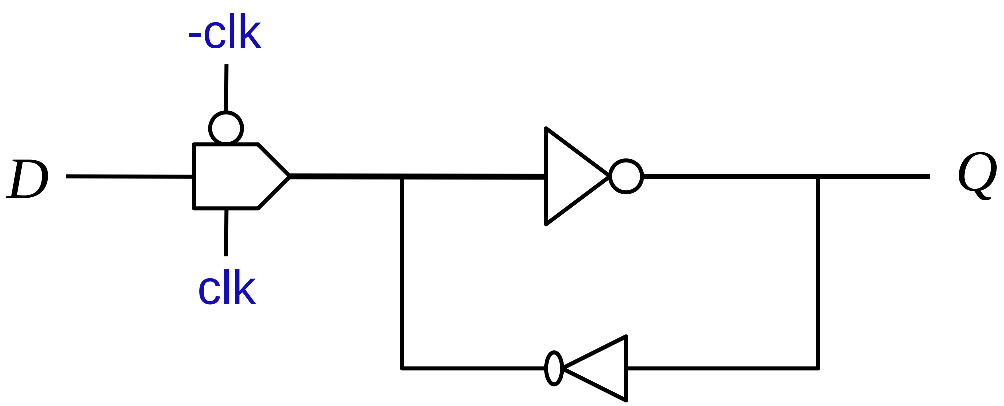
Registers

- CMOS circuit implementation of the positive-edge triggered register

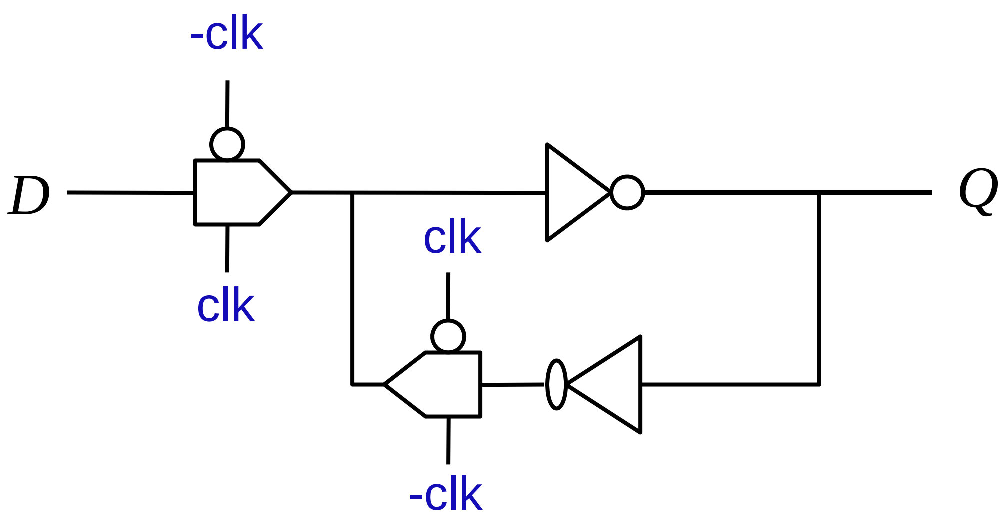


Single-Phase Latch

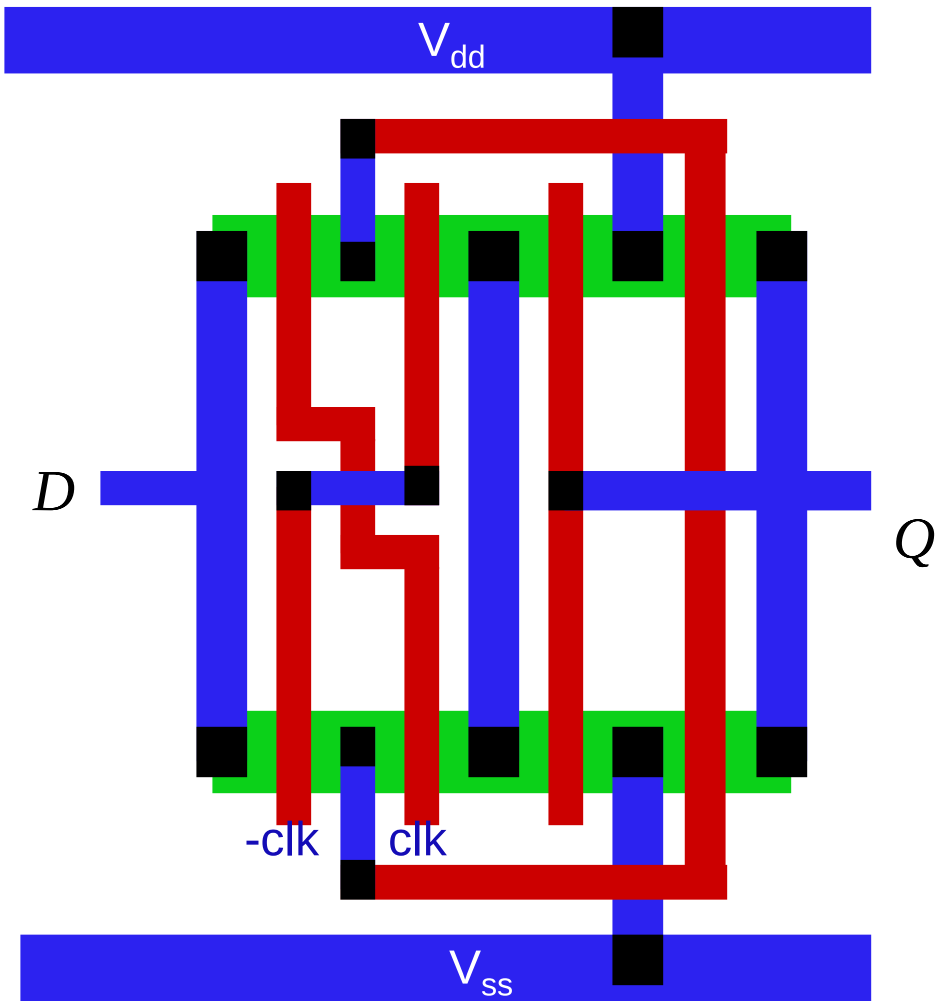
- Positive active-static latch

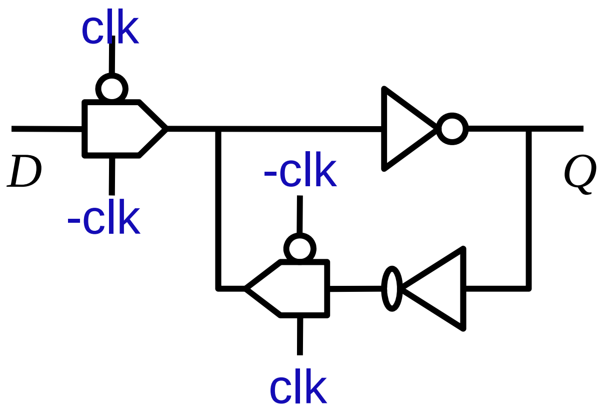


1. Low area cost
2. Driving capability of D must override the feedback inverter



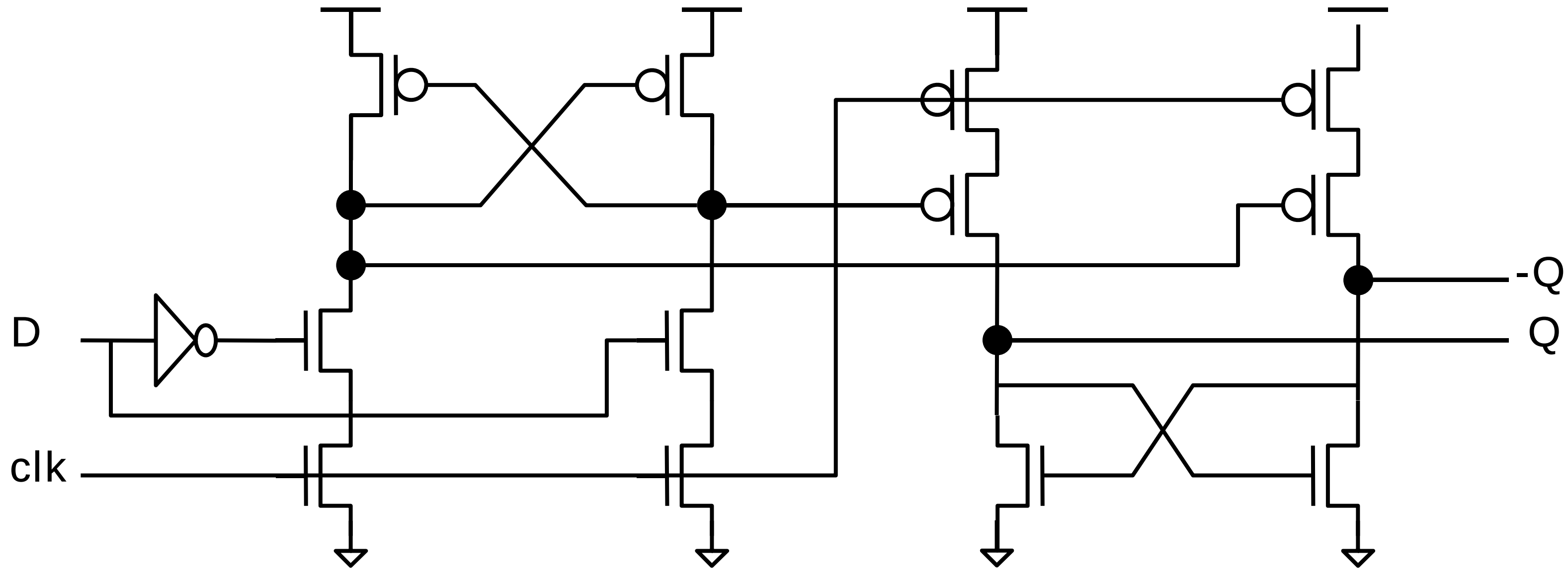
Typical Latch Symbolic Layouts





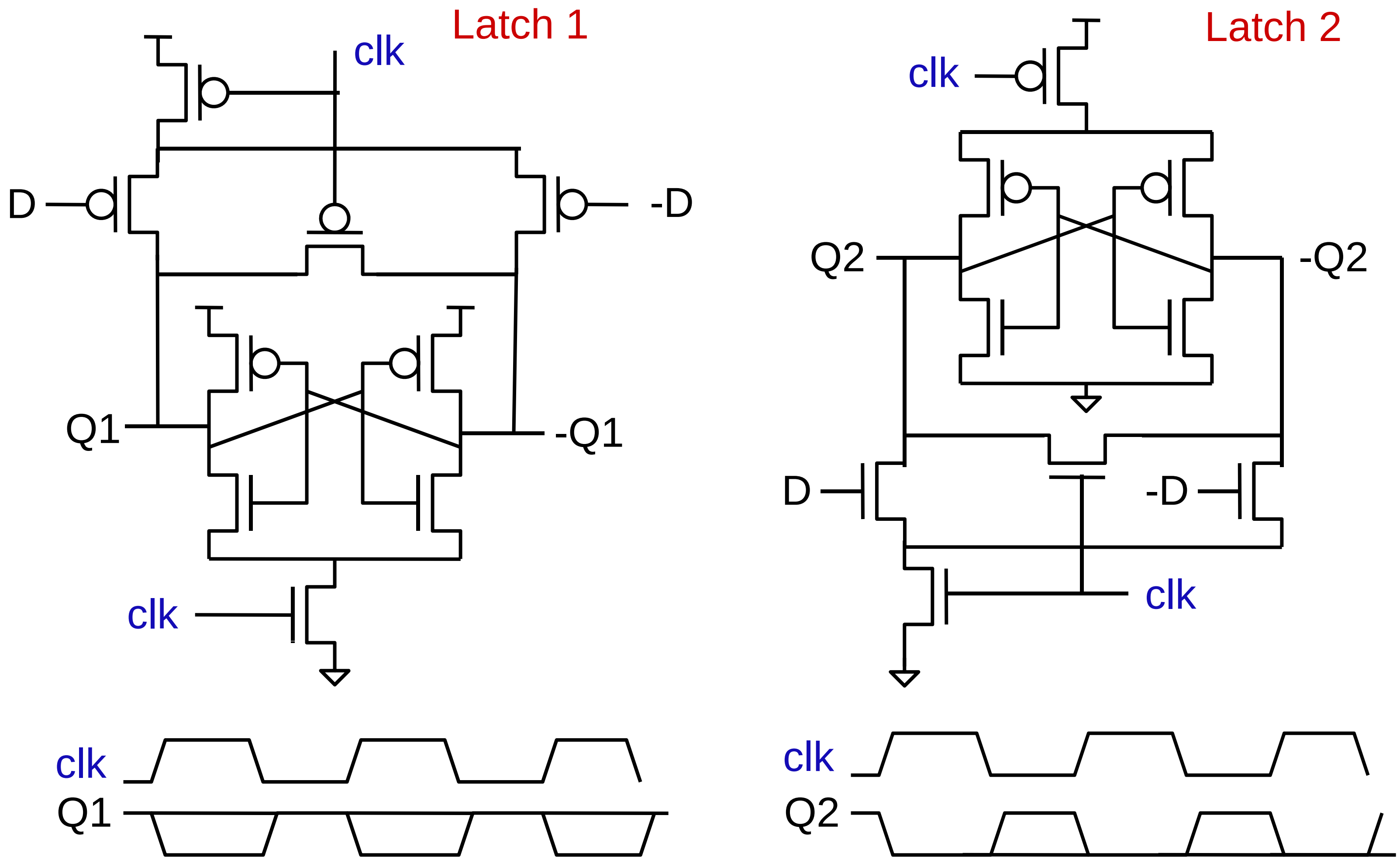
CVSL (Differential) Style Register

- The following figure shows latches based on a CVSL structure
  - An N and a P version are shown that are cascaded to form a register



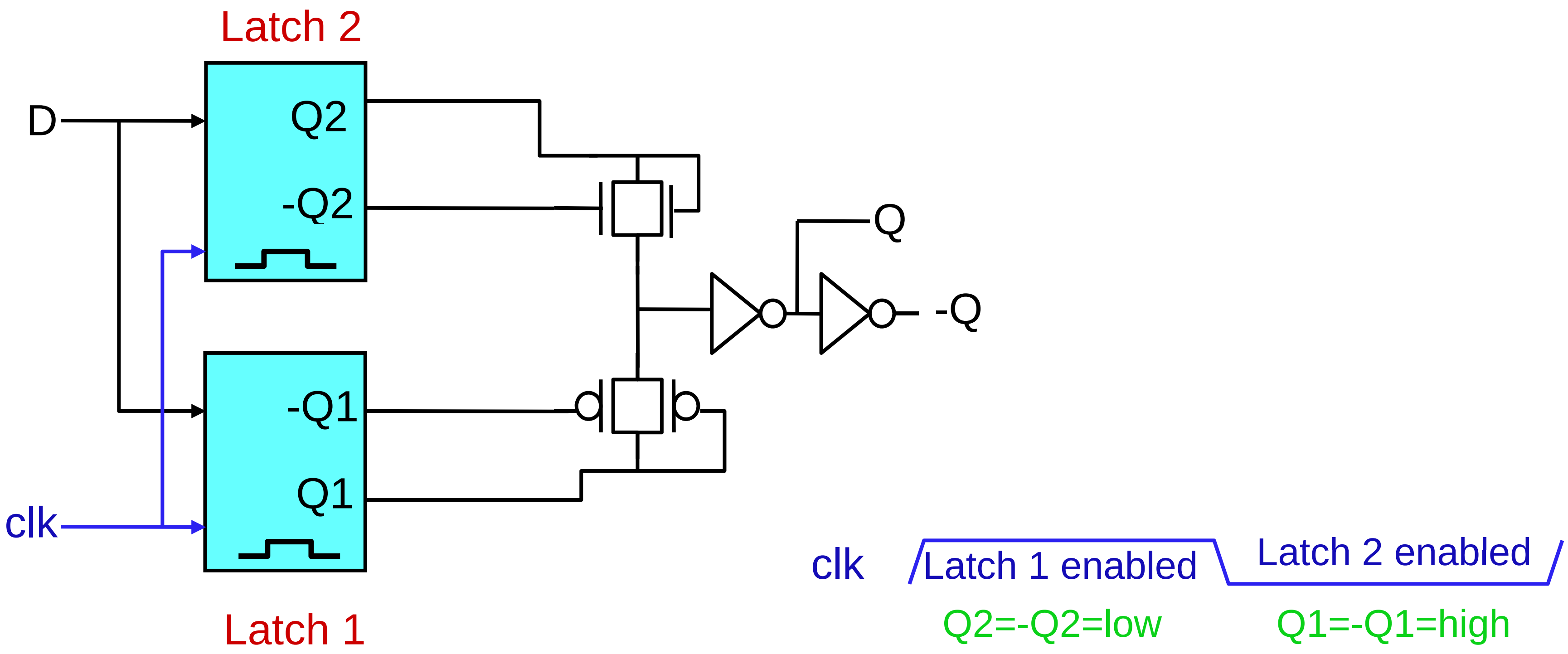
Double-Edge Triggered Register

- The following figure shows latches that may be used to clock data on both edges of the clock



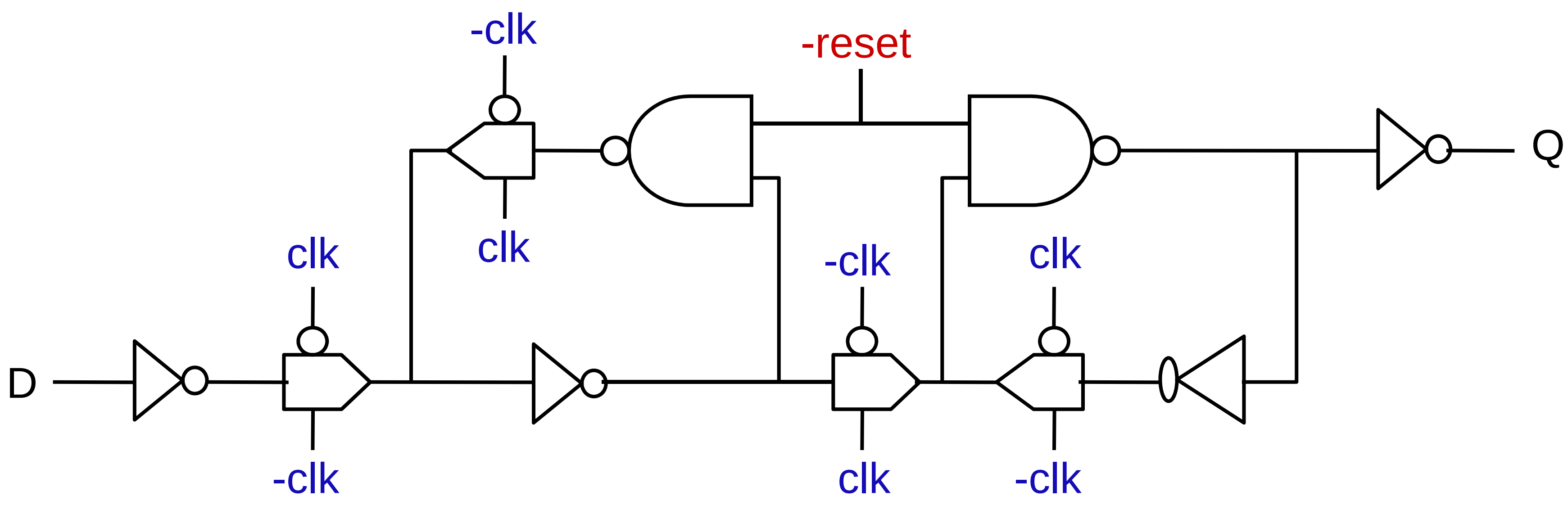
Double-Edge Triggered Register

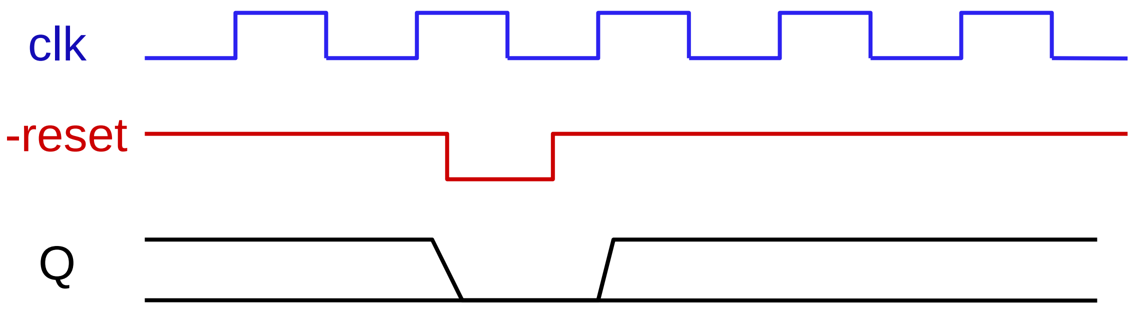
- Double-edge triggered register can be implemented by combining Latch 1 & Latch 2 as follows



Asynchronously Register

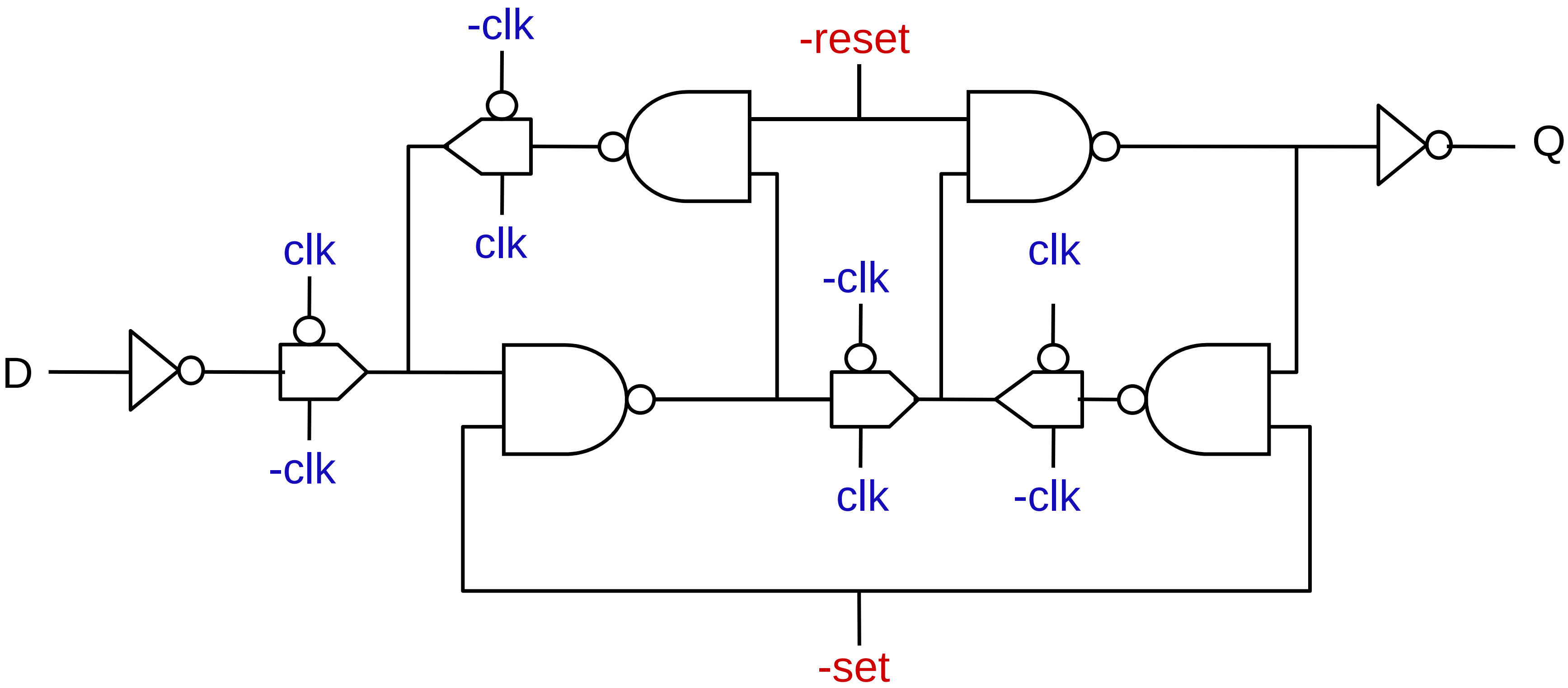
- Asynchronously resettable register





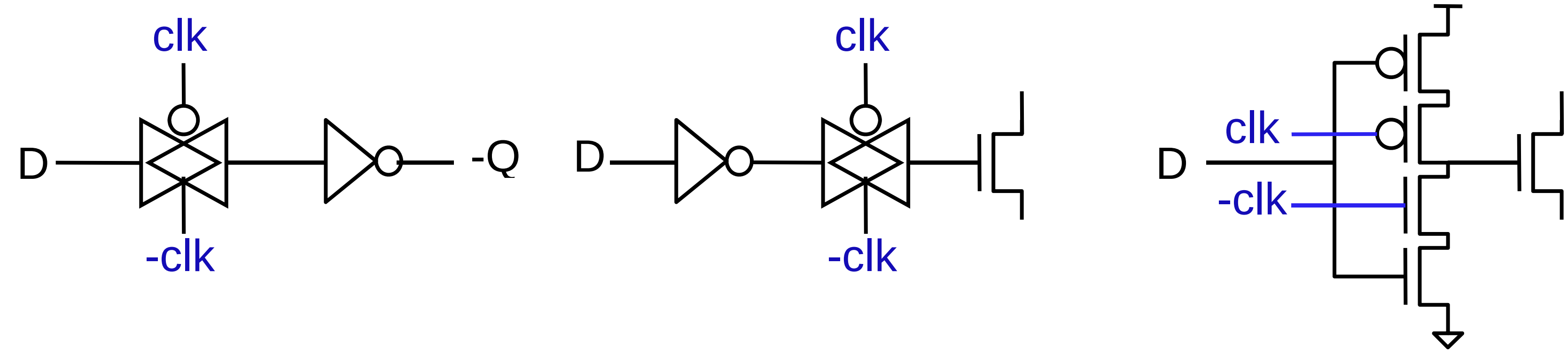
Asynchronously Register

- Asynchronously resettable and settable register

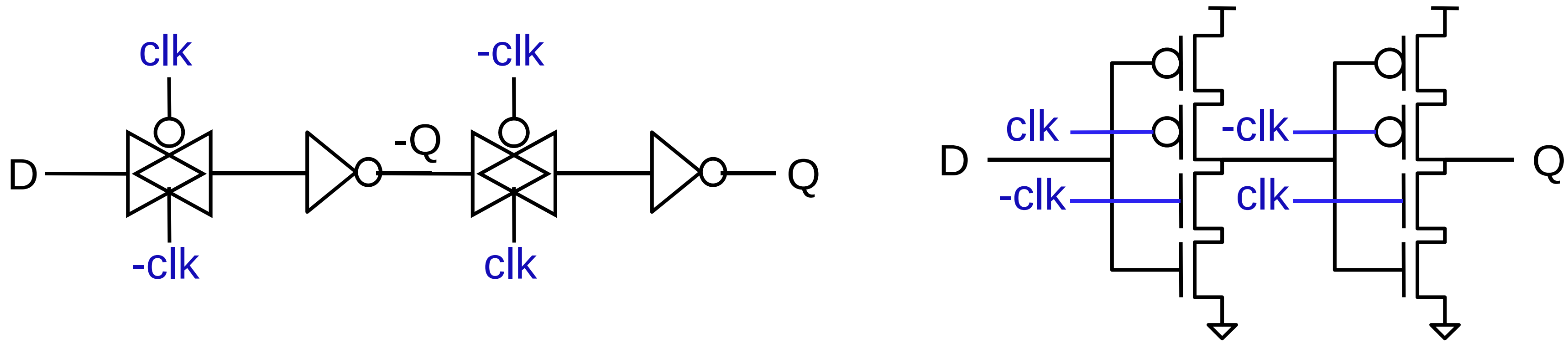


Dynamic Latches & Registers

- Dynamic single clock latches

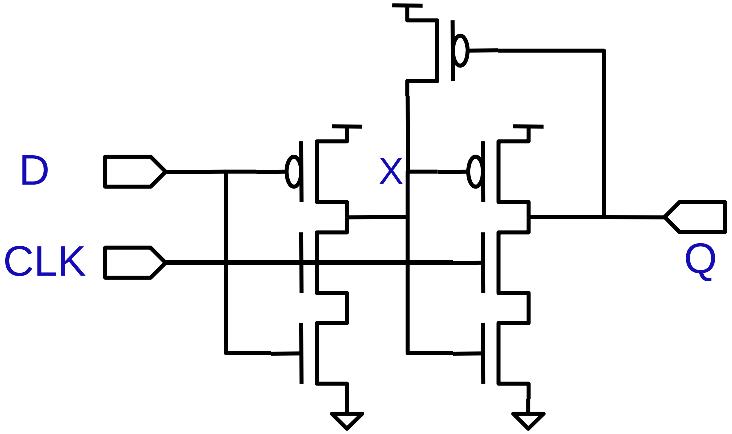


- Dynamic single clock registers



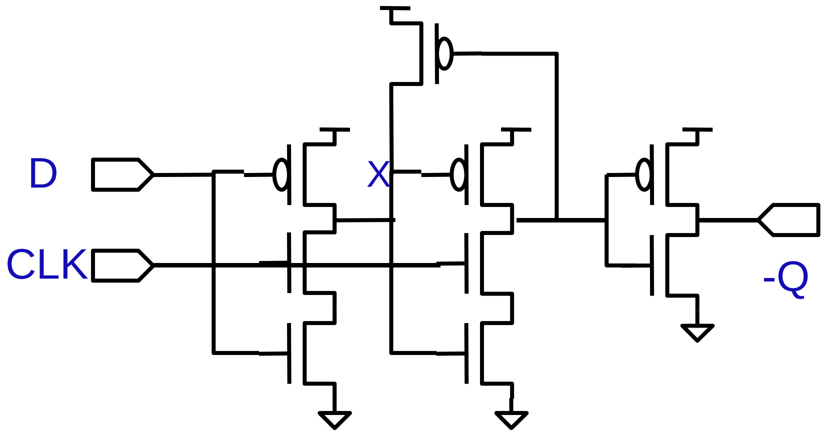
Dynamic Latches

- Clock active high latch



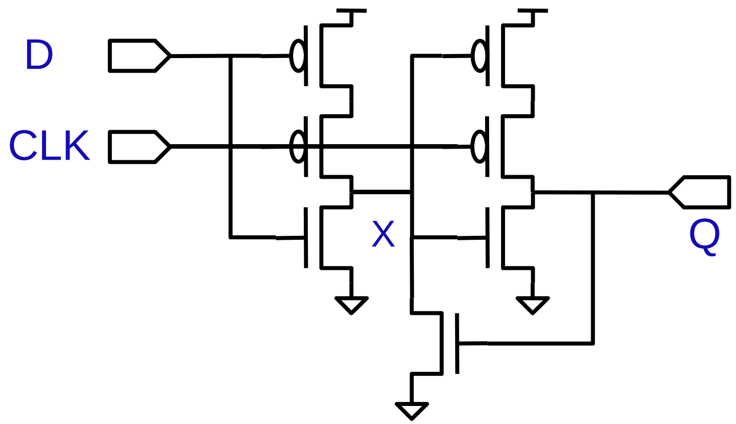
D_n	CLK	X_n	Q_n
0	H	1	0
1	H	0	1
1	L	X_{n-1}	Q_{n-1}
0	L	1	Q_{n-1}

- Clock active high latch with buffer



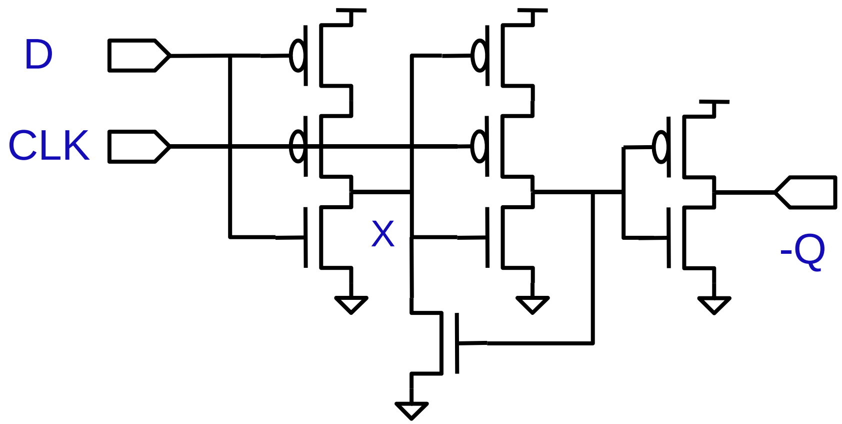
Dynamic Latches

- Clock active low latch



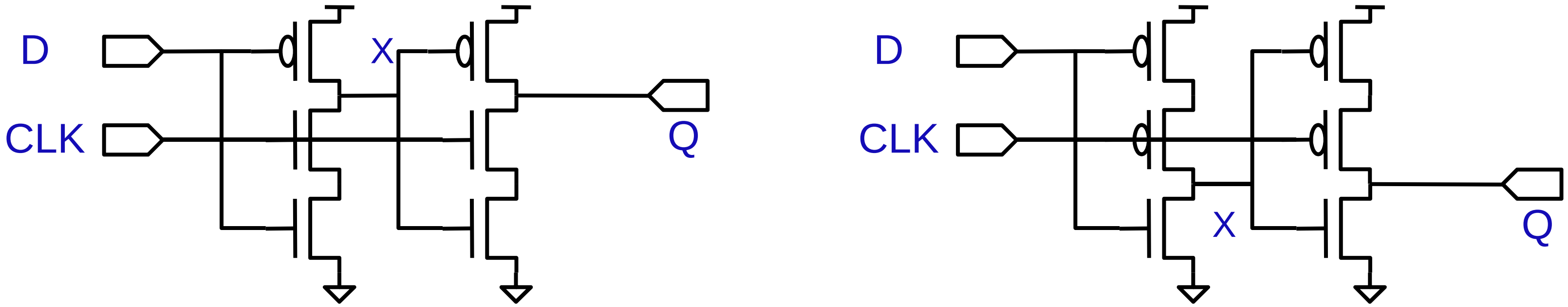
D_n	CLK	X_n	Q_n
0	L	1	0
1	L	0	1
1	H	0	Q_{n-1}
0	H	X_{n-1}	Q_{n-1}

- Clock active low latch with buffer



Dynamic Latches

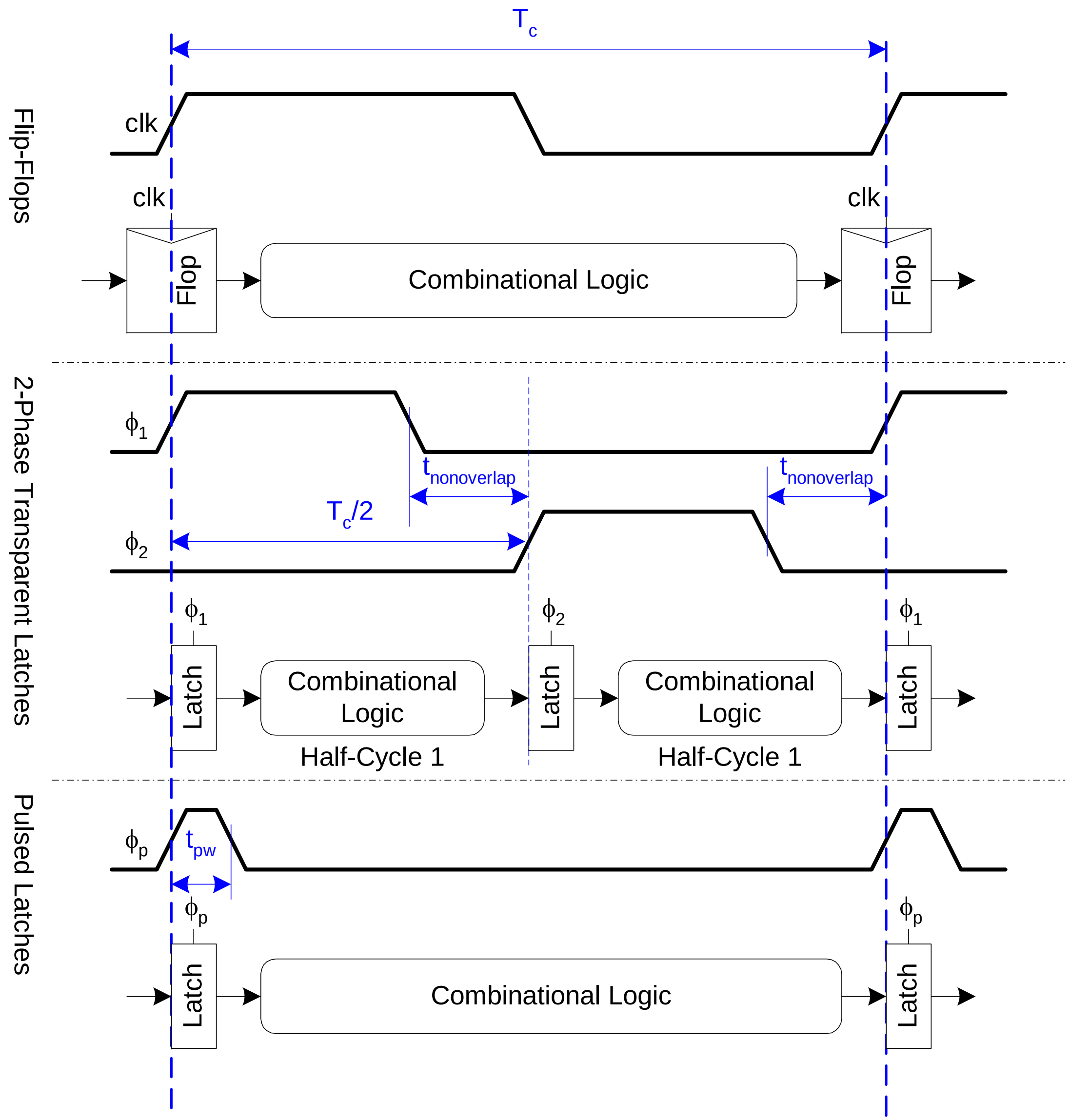
- Clock active high and low latches without feedback



- The problem of leakage current
  - Assume that the capacitance of node X is 0.002pF and the leakage current I is 1nA
    - Therefore, T=CV/I=0.002pFx5V/1nA=100us
    - That is, the latch needs to be refreshed each 100us. Otherwise, the output Q will become high

Sequencing Methods

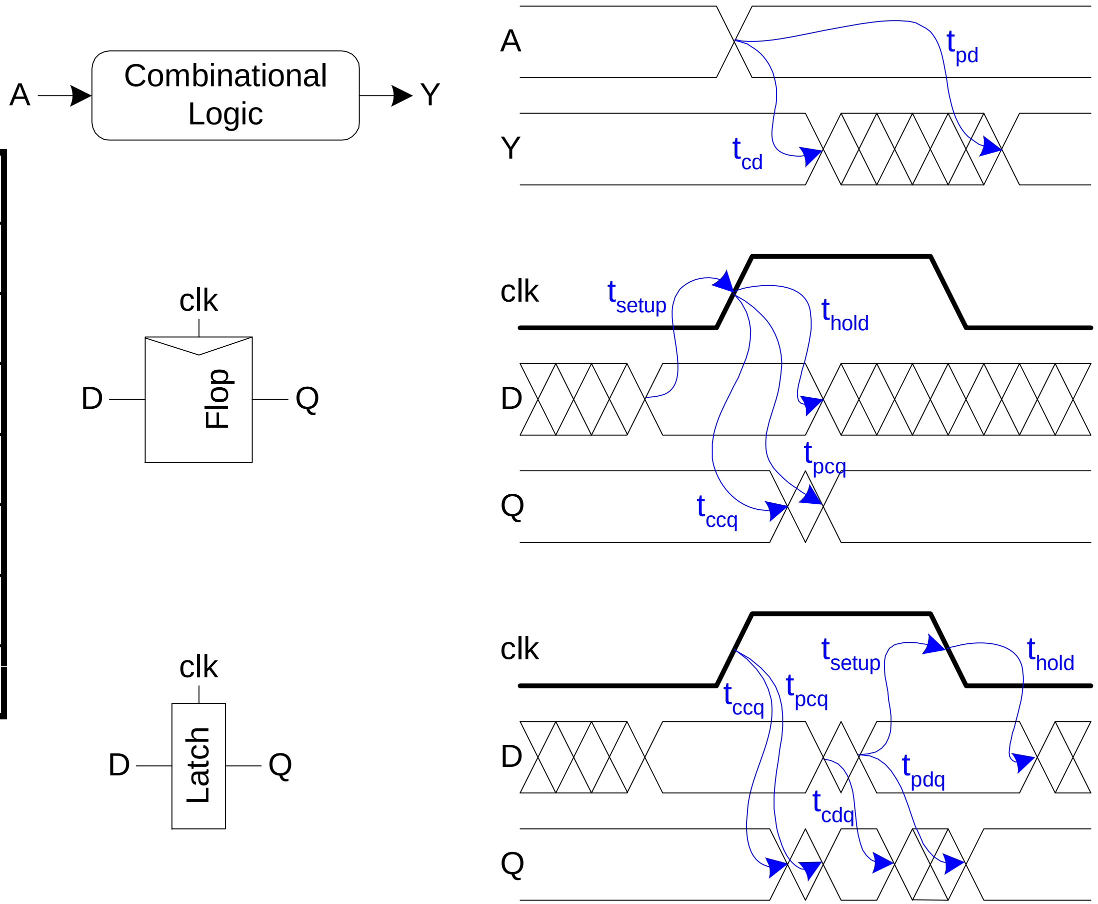
- Flip-flops
- 2-Phase Latches
- Pulsed Latches



Timing Diagrams

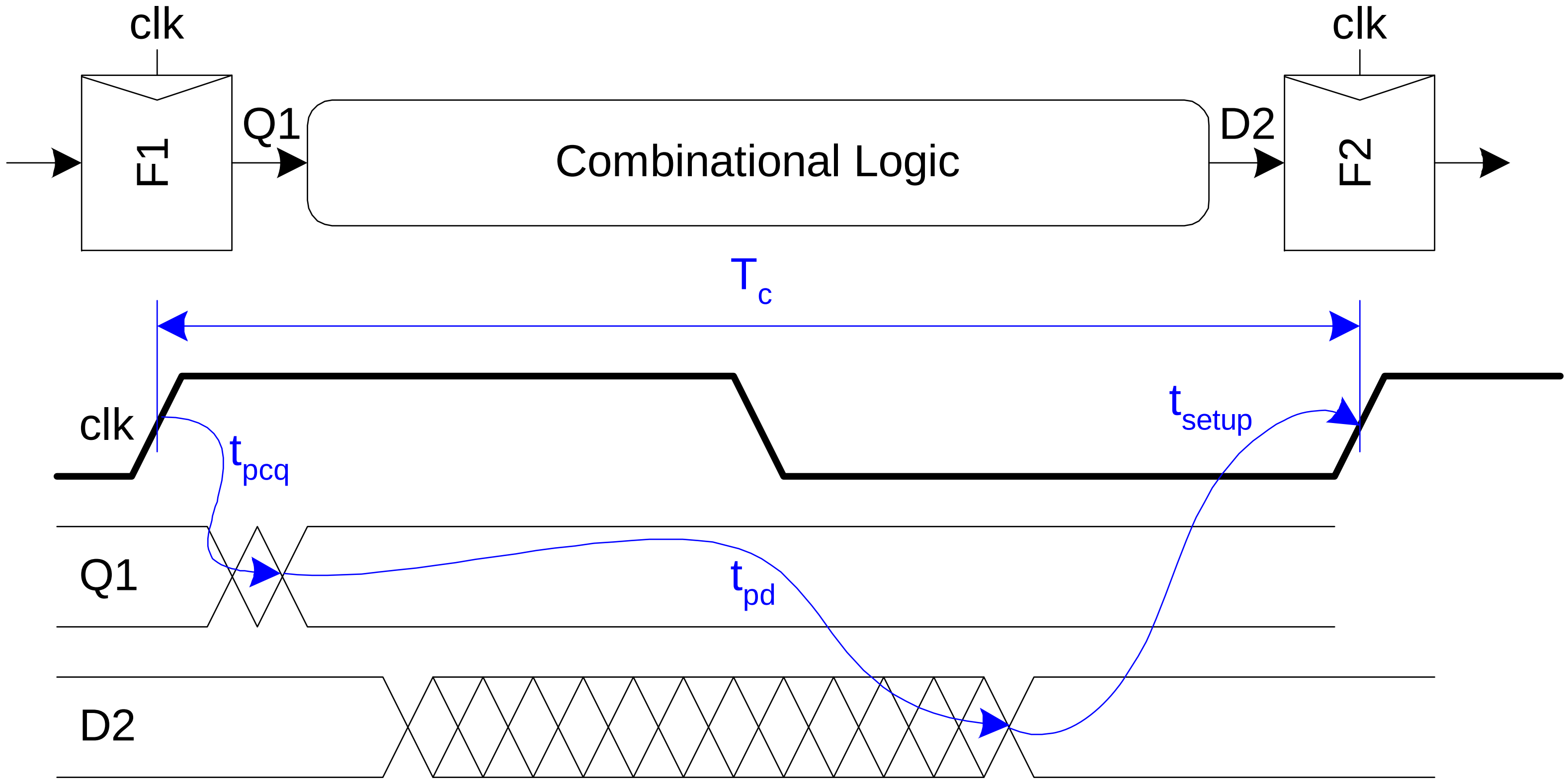
Contamination and Propagation Delays

t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay
t_{pcq}	Latch/Flop Clk-Q Prop Delay
t_{ccq}	Latch/Flop Clk-Q Cont. Delay
t_{pdq}	Latch D-Q Prop Delay
t_{pcq}	Latch D-Q Cont. Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time



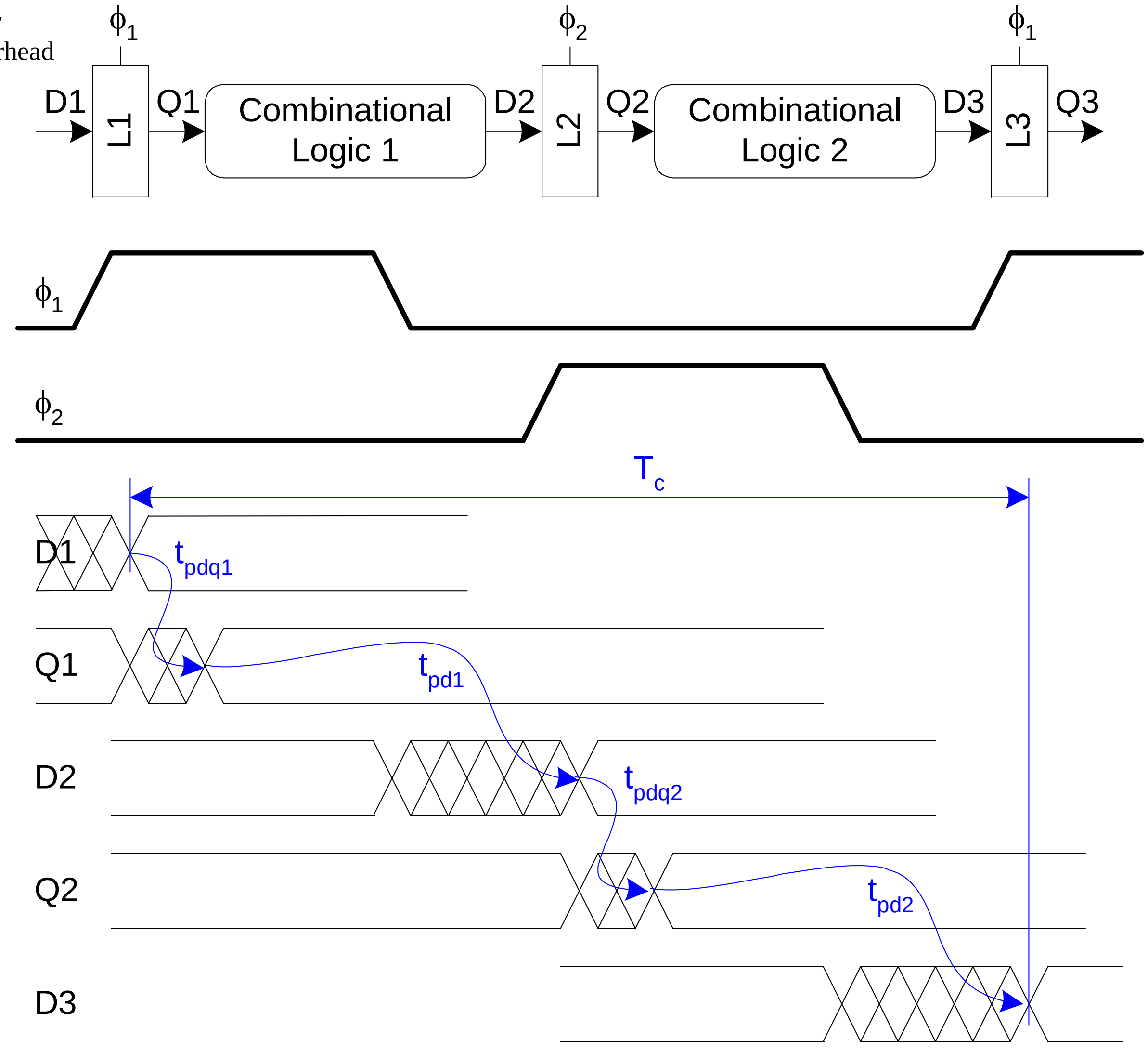
Max-Delay: Flip-Flops

$$t_{pd} \leq T_c - \underbrace{\left(t_{\text{setup}} + t_{pcq}\right)}_{\text{sequencing overhead}}$$



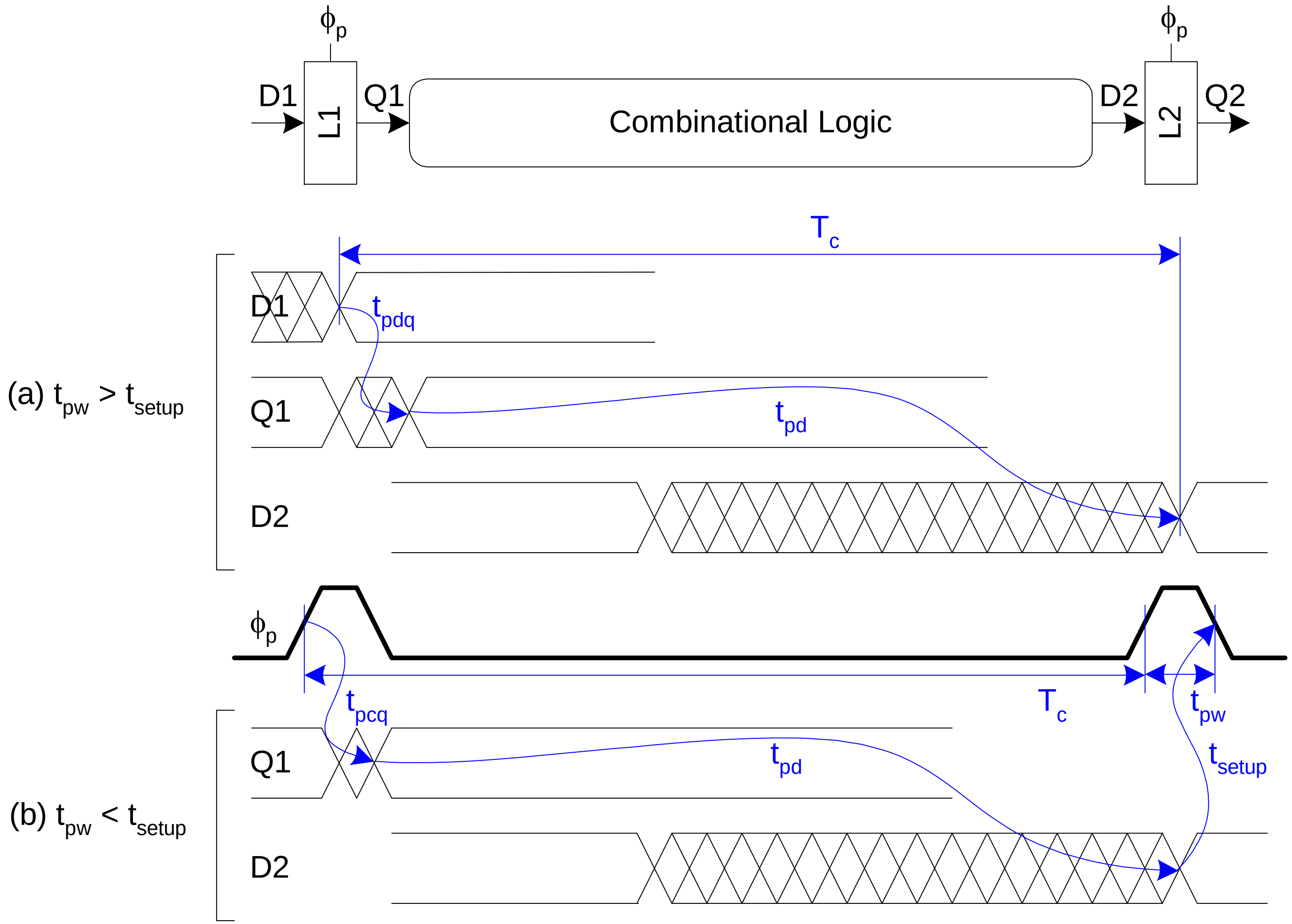
Max Delay: 2-Phase Latches

$$t_{pd} = t_{pd1} + t_{pd2} \le T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}}$$



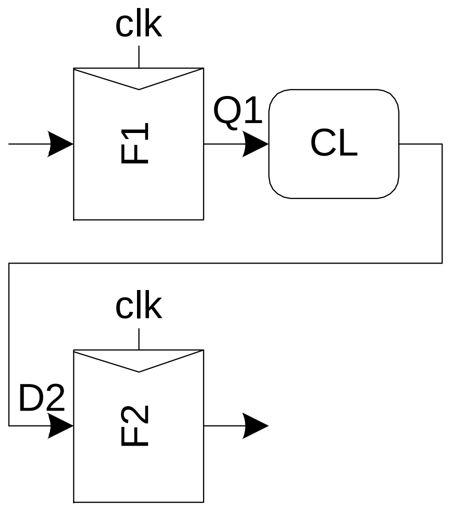
Max Delay: Pulsed Latches

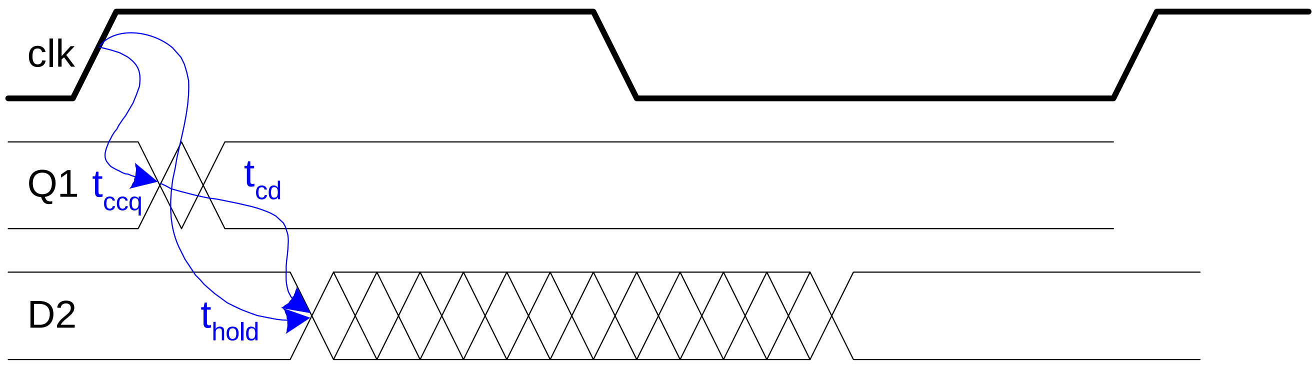
$$t_{pd} \le T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{setup} - t_{pw}\right)}_{\text{sequencing overhead}}$$



Min-Delay: Flip-Flops

$$t_{cd} \geq t_{\text{hold}} - t_{ccq}$$





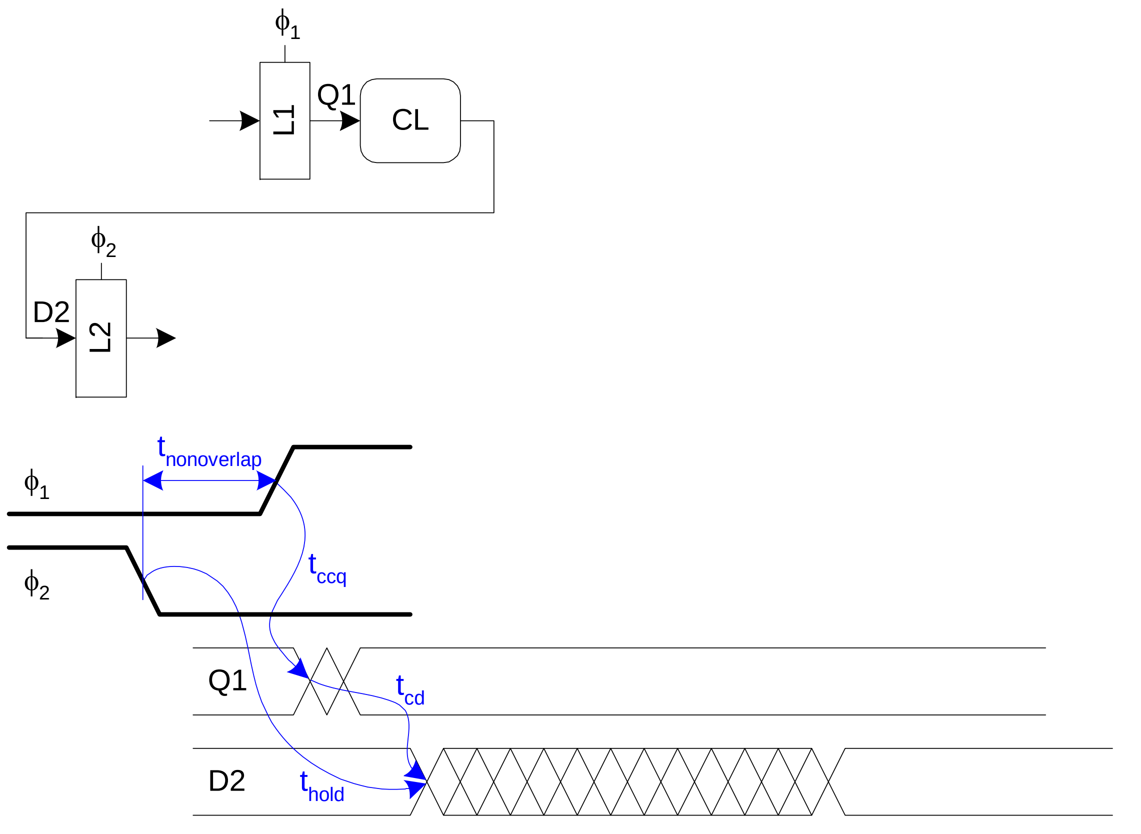
Min-Delay: 2-Phase Latches

$$t_{cd1}, t_{cd2} \geq t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}}$$

Hold time reduced by nonoverlap

Paradox: hold applies twice each cycle, vs. only once for flops.

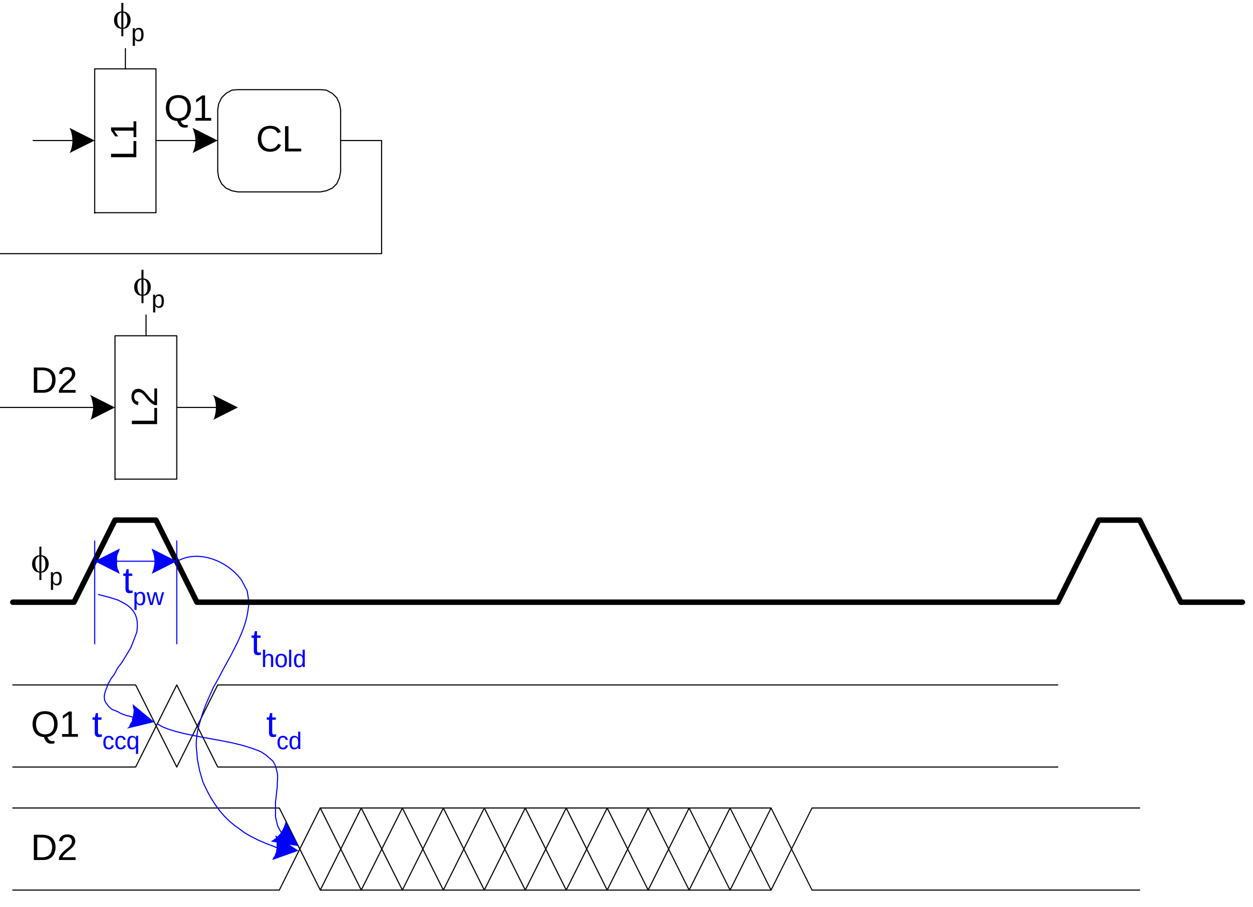
But a flop is made of two latches!



Min-Delay: Pulsed Latches

$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{pw}$$

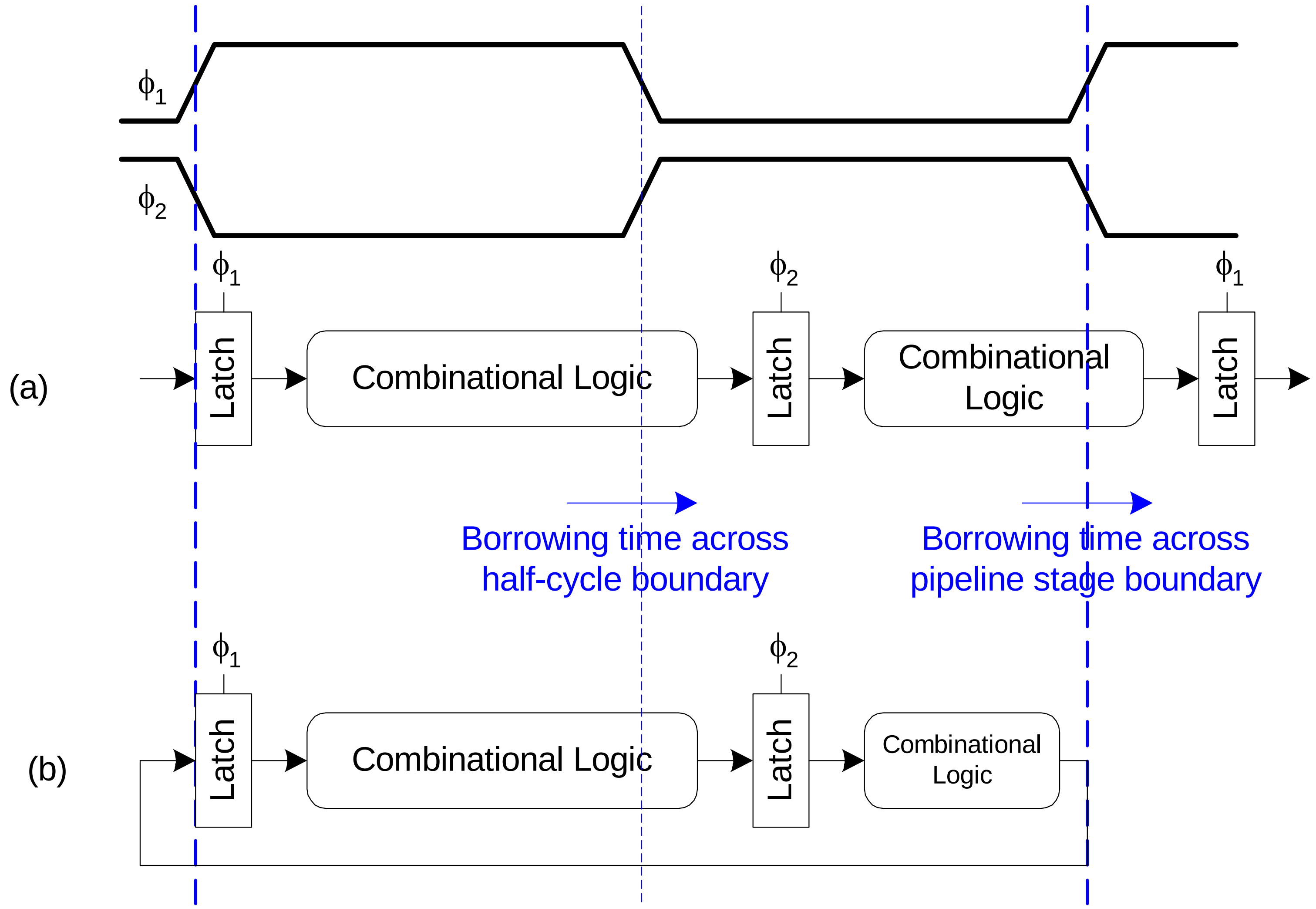
Hold time increased by pulse width



Time Borrowing

- In a flop-based system:
  - Data launches on one rising edge
  - Must setup before next rising edge
  - If it arrives late, system fails
  - If it arrives early, time is wasted
  - Flops have hard edges
- In a latch-based system
  - Data can pass through latch while transparent
  - Long cycle of logic can borrow time into next
  - As long as each loop completes in one cycle

Time Borrowing Example



Loops may borrow time internally but must complete within the cycle

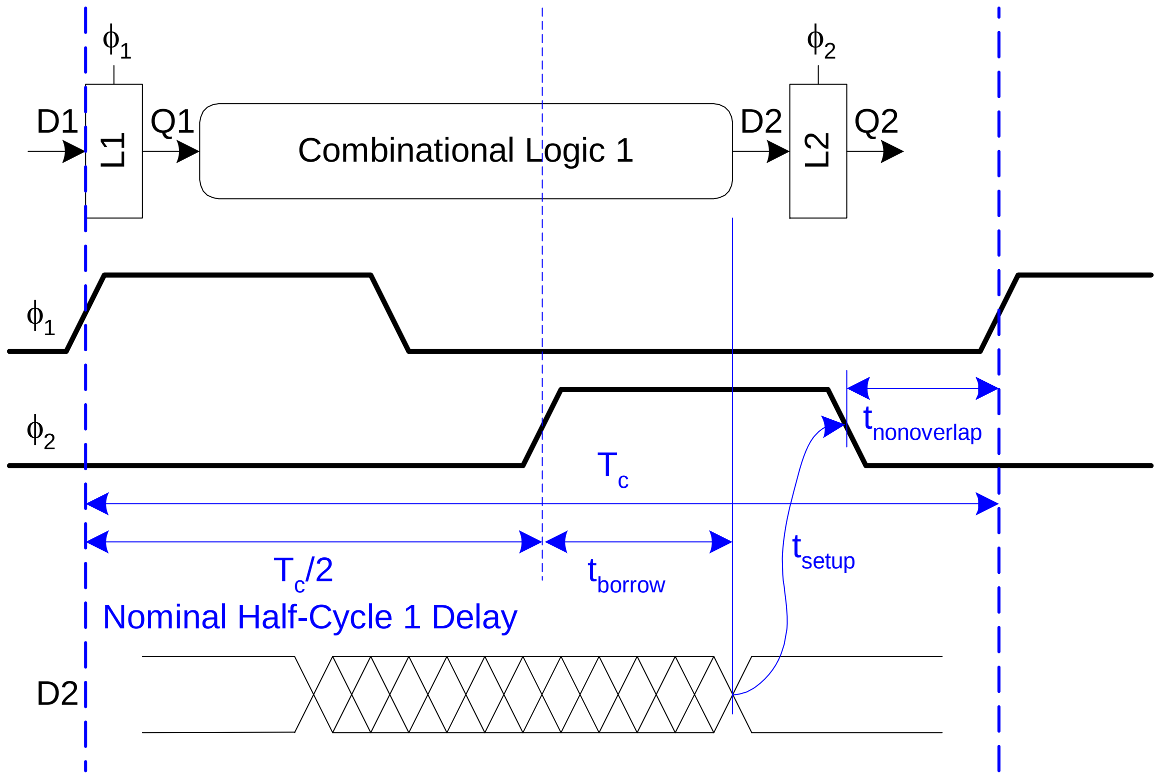
How Much Borrowing?

2-Phase Latches

$$t_{\text{borrow}} \le \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}}\right)$$

Pulsed Latches

$$t_{\text{borrow}} \le t_{pw} - t_{\text{setup}}$$



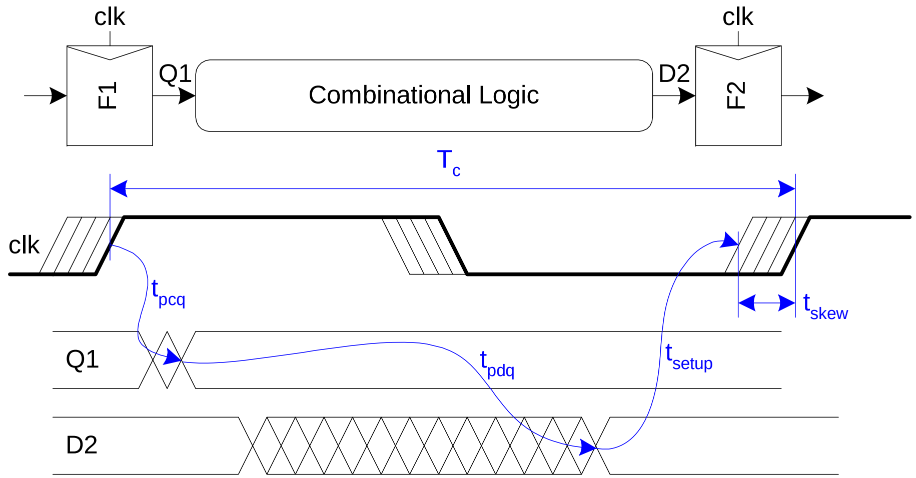
Clock Skew

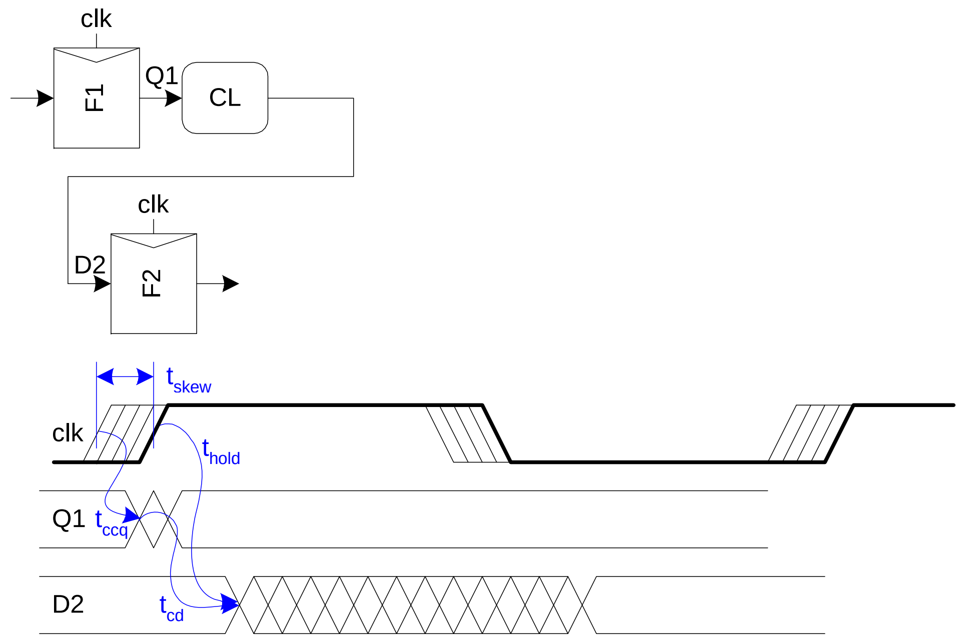
- We have assumed zero clock skew
- Clocks really have uncertainty in arrival time
  - Decreases maximum propagation delay
  - Increases minimum contamination delay
  - Decreases time borrowing

Skew: Flip-Flops

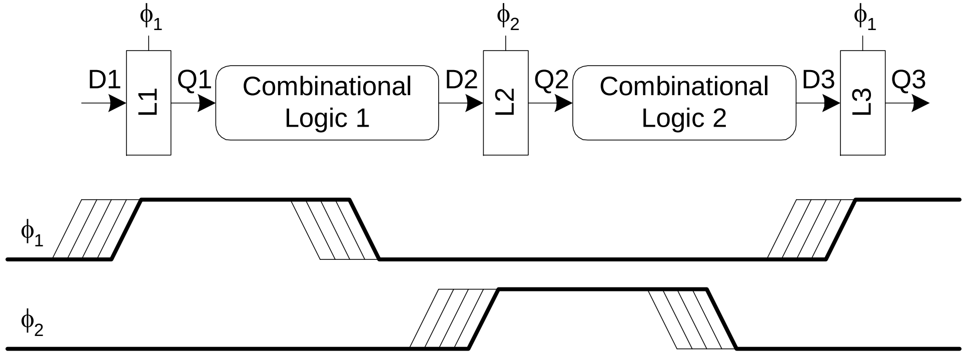
$$t_{pd} \le T_c - \underbrace{\left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$

$$t_{cd} \ge t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$





Skew: Latches



2-Phase Latches

$$t_{pd} \le T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}}$$

$$t_{cd1}, t_{cd2} \ge t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}} + t_{\text{skew}}$$

$$t_{\text{borrow}} \le \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}} + t_{\text{skew}}\right)$$

Pulsed Latches

$$t_{pd} \le T_c - \underbrace{\max\left(t_{pdq}, t_{pcq} + t_{\text{setup}} - t_{pw} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$

$$t_{cd} \ge t_{\text{hold}} + t_{pw} - t_{ccq} + t_{\text{skew}}$$

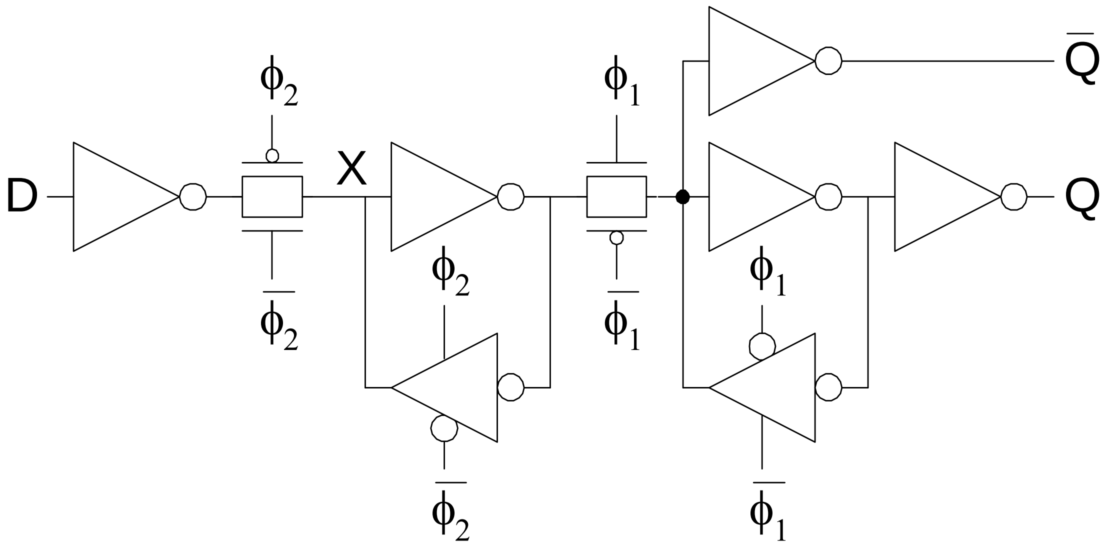
$$t_{\text{borrow}} \le t_{pw} - \left(t_{\text{setup}} + t_{\text{skew}}\right)$$

Two-Phase Clocking

- If setup times are violated, reduce clock speed
- If hold times are violated, chip fails at any speed
- In this class, working chips are most important
  - No tools to analyze clock skew
- An easy way to guarantee hold times is to use 2-phase latches with big nonoverlap times
- Call these clocks ϕ_1, ϕ_2 (ph1, ph2)

Safe Flip-Flop

- In class, use flip-flop with nonoverlapping clocks
  - Very slow – nonoverlap adds to setup time
  - But no hold times
- In industry, use a better timing analyzer
  - Add buffers to slow signals if hold time is at risk



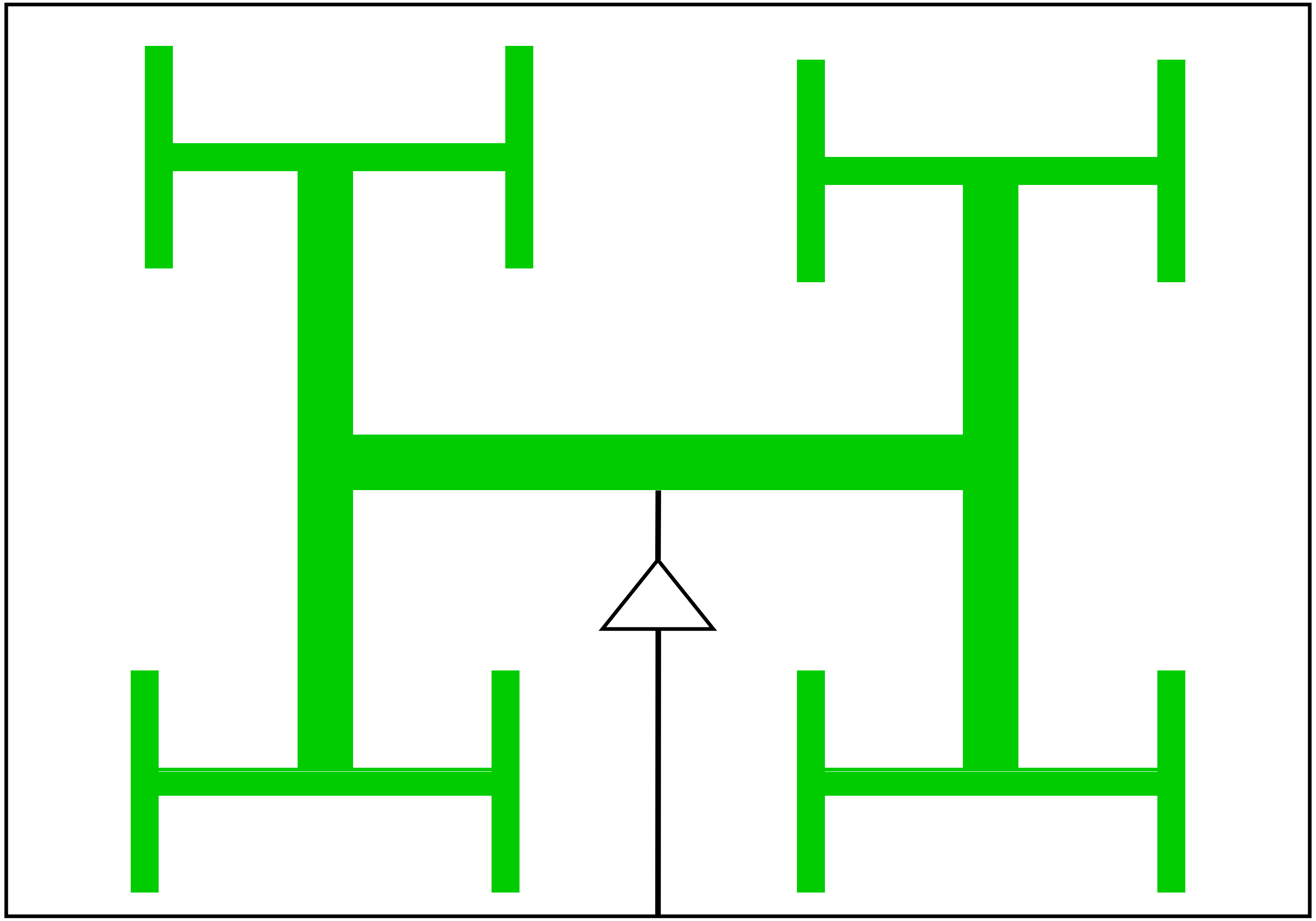
Clock Distribution

- In a large CMOS chip, clock distribution is a serious problem
  - For example,
    - $V_{dd}=5V$
    - $C_{reg}=2000pF$ (20K register bits @ 0.1pF)
    - $T_{clk}=10ns$
    - $T_{rise/fall}=1ns$
    - $I_{peak}=C(dv/dt)=(2000p)\times(5/1n)=10A$
    - $P_d=C(V_{dd})^2f=2000p\times25\times100=5W$
- Methods for reducing the values of I_{peak} and P_d
  - Reduce C
  - Interleaving the rise/fall time

Clock Distribution

- Clocking is a floorplanning problem because clock delay varies with position on the chip
- Ways to improve clock distribution
  - Physical design
    - Make clock delays more even
    - At least more predictable
  - Circuit design
    - Minimizing delays using several stages of drivers
- Two most common types of physical clocking networks
  - H-tree clock distribution
  - Balanced-tree clock distribution

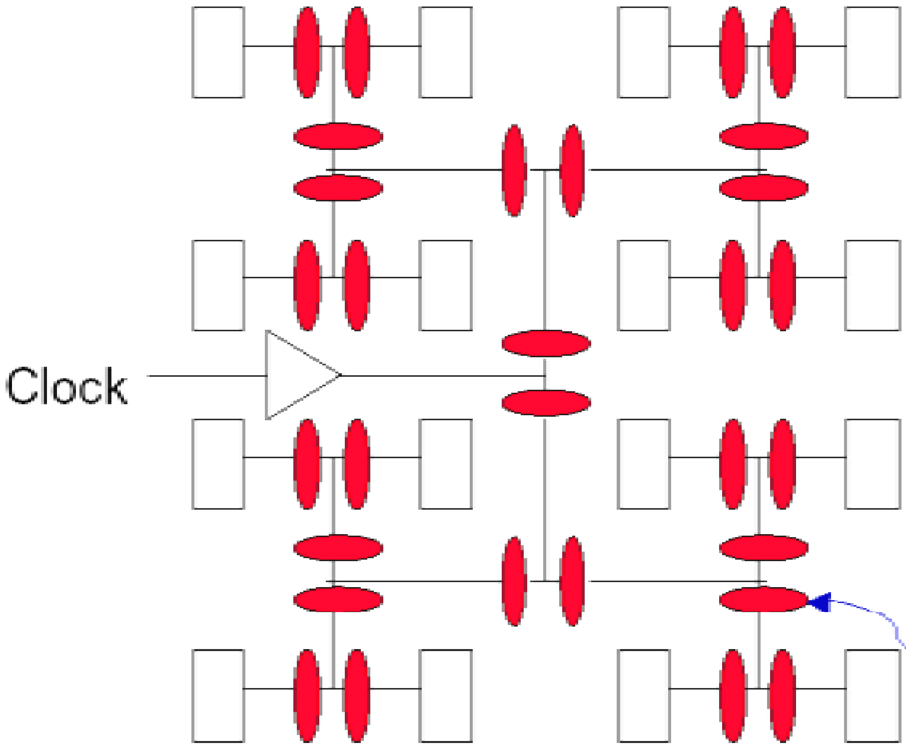
H-Tree Clock Distribution



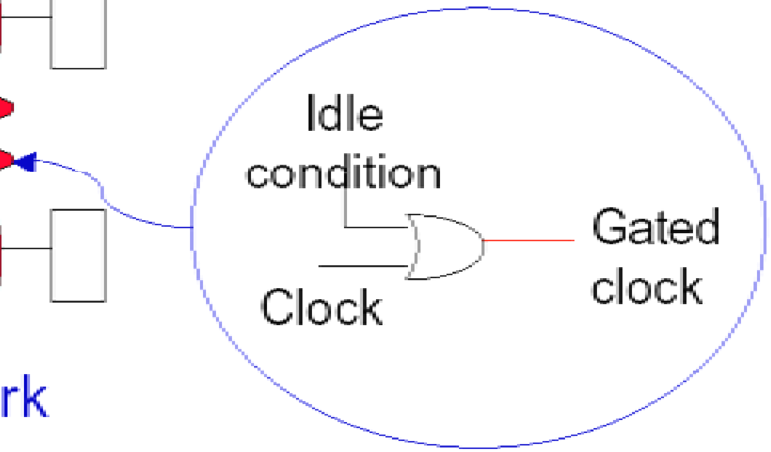
H-Tree Clock Distribution

Can insert clock gating at multiple levels in clock tree

Can shut off entire subtree if all gating conditions are satisfied

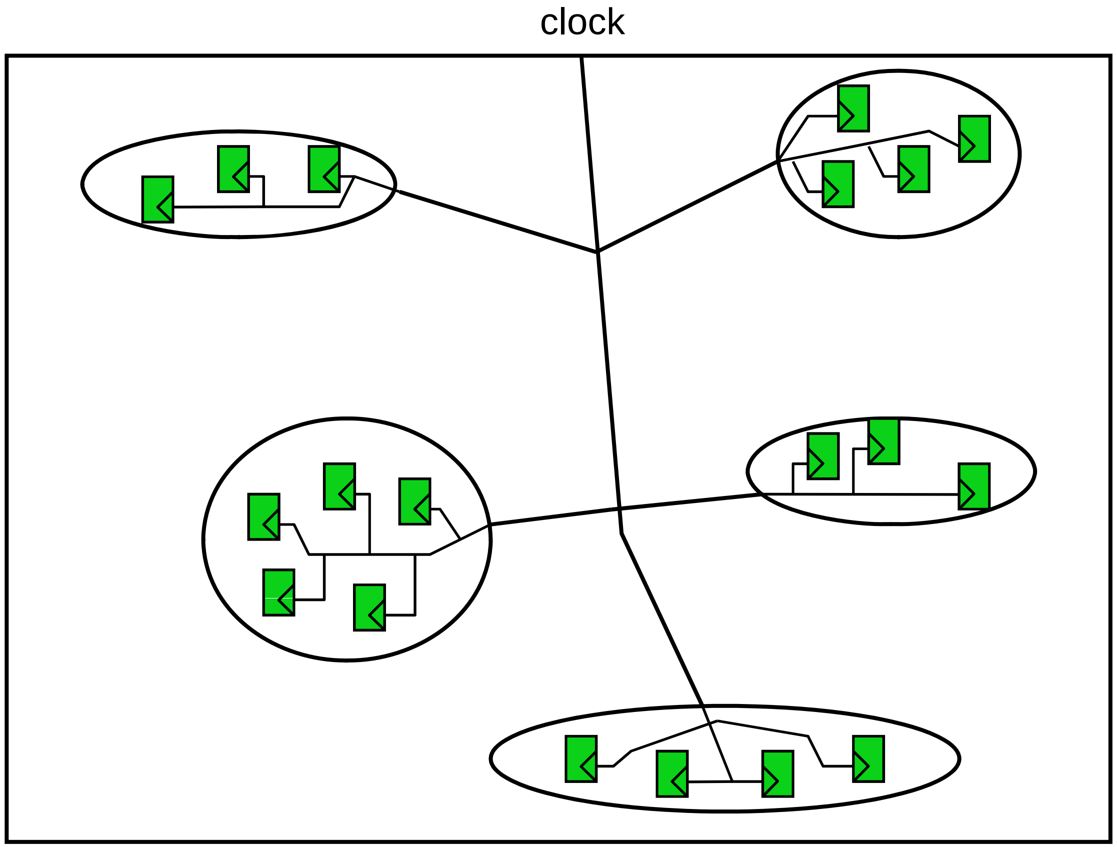


H-Tree Clock Network



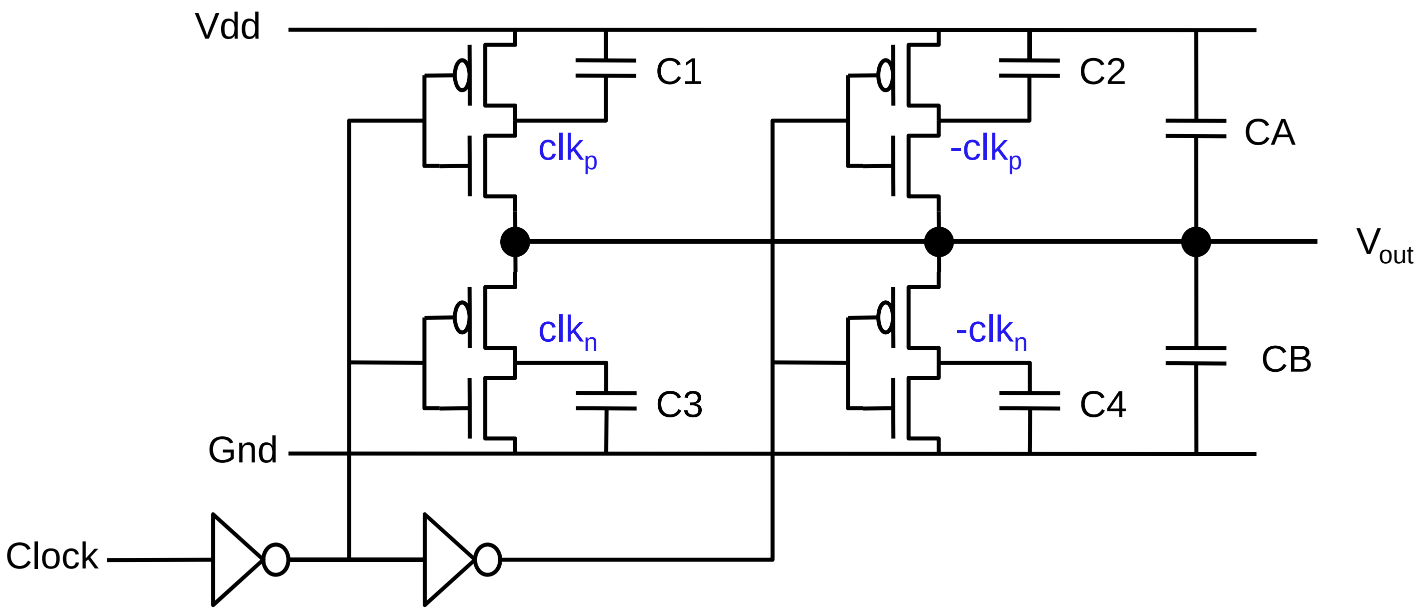
Source: Prof. Irwin

Balanced-Tree Clock Distribution

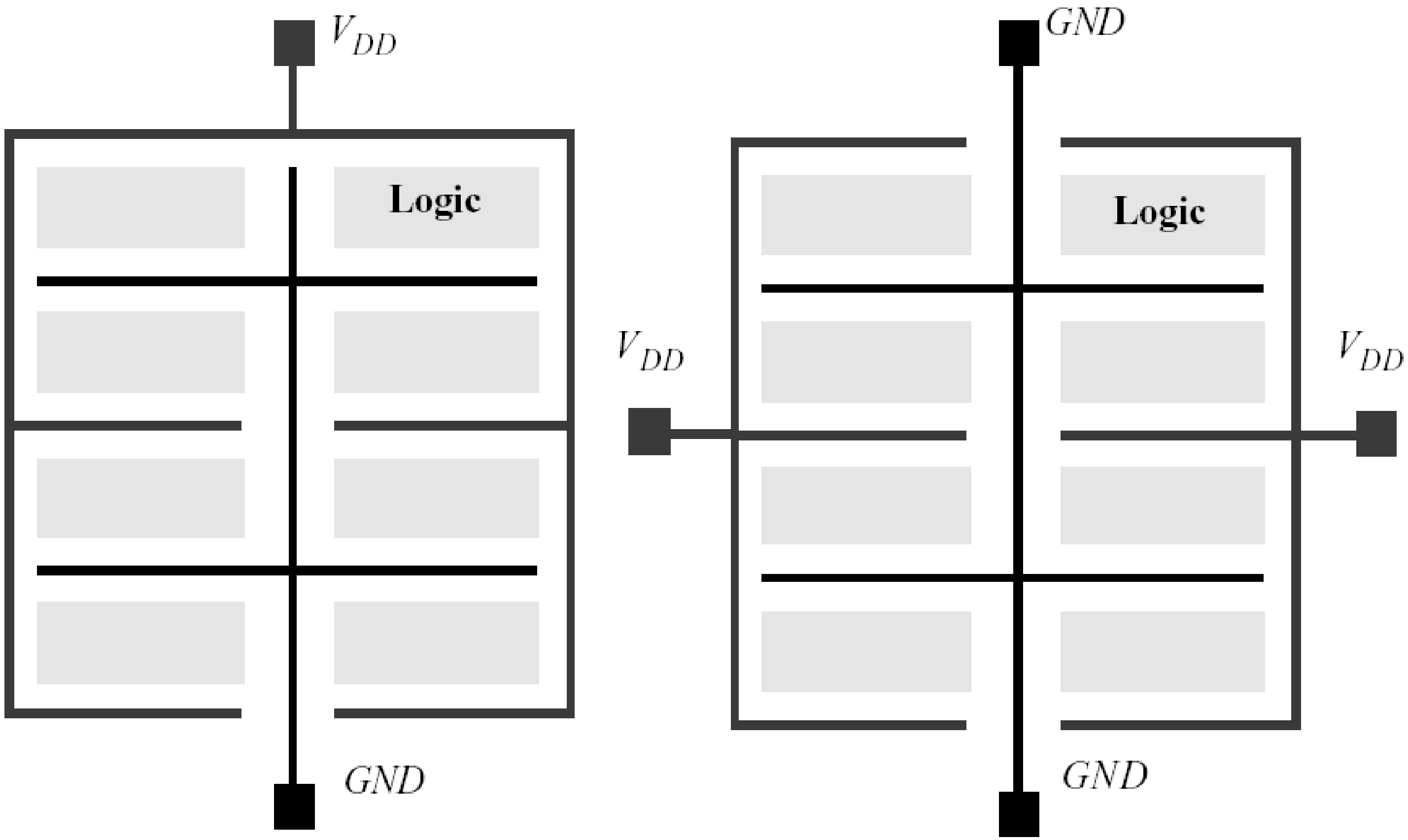


Reduce Clocking Power

- Techniques used to reduce the high dynamic power dissipation
  - Use a low capacitance clock routing line such as metal3. This layer of metal can be, for example, dedicated to clock distribution only
  - Using low-swing drivers at the top level of the tree or in intermediate levels



Power & Ground Distribution



(a) Finger-shaped network (b) Network with multiple supply pins

Source: Prof. Irwin