EE6013 VLSI Design—Homework 2

1. **RC Model of MOS Transistor** (3 points)
   Construct the RC switch model for the NMOS transistor layout in Figure 1. Assume a power supply voltage of 3V and that the dimensions are in units of microns, and parameters of the NMOS are ($L = 0.5\mu m$, $V_{tn} = 0.6V$, $k_n = 150\mu A/V^2$, $C_{ox} = 2.70fF/\mu m^2$, $C_{ja} = 0.86fF/\mu m^2$, $\lambda = 0.5\mu m$ and $C_{jp} = 0.24fF/\mu m$.

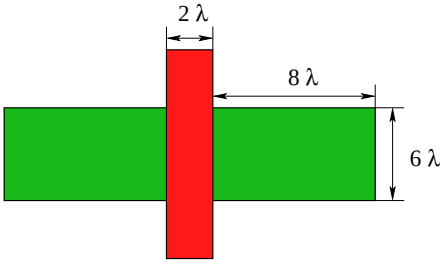

Figure 1: The layout view of an NMOS.

2. **CMOS Design** (3 points)
   Design a CMOS circuit to implement the truth table shown in Table 1. This circuit has 4 data inputs (a_0–a_3), 4 control inputs (c_0–c_3), and 4 data outputs (z_0–z_3).

Table 1: Truth table of a CMOS circuit.

c_3	c_2	c_1	c_0	z_3	z_2	z_1	z_0
0	1	1	1	a_3	a_2	a_1	a_0
1	0	1	1	a_2	a_1	a_0	a_3
1	1	0	1	a_1	a_0	a_3	a_2
1	1	1	0	a_0	a_3	a_2	a_1

3. **Crosstalk Simulation** (4 points)
   Figure 2 shows two designs of parallel wires, where the $\times 1$ inverter means that the sizes of NMOS and PMOS are $4\mu m/0.18\mu m$, and $2\mu m/0.18\mu m$. Simulate these two cases with Hspice. Show the waveforms of S_a and S_v.

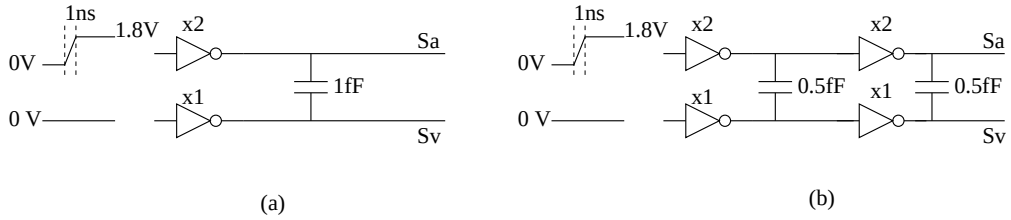

Figure 2: Two different designs of parallel wires.

4. **Article Reading** (4 points)
   Read the article entitled ”The High-k solution”, which is published in *IEEE Spectrum*, vol. 44, no. 10, pp. 23-29, Oct. 2007. Then, write a summary about this article.