Homework 3 3-1

## EE6013 VLSI Design—Homework 3

- 1. Use layout editor to draw a symbolic layout for a CMOS circuit that implements  $F = \overline{A + BC}$ . (5 points)
- 2. Use layout editor to draw a standard-cell style layout for a CMOS circuit that implements  $F = \overline{A + BD + C}$ . (5 points)
- 3. Article Reading (3 points)

Read the article entitled "Transistors go vertical", which is published in *IEEE Spectrum*, vol. 44, no. 11, pp. 13-14, Nov. 2007. Then, write a summary about this article.

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