EE8054
Semiconductor Memory Testing

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Syllabus

Contents

- Chapter 1: Introduction
- Chapter 2: Basics of Memories & VLSI Testing
- Chapter 3: Functional Fault Models and Test Algorithms
- Chapter 4: Memory Built-In Self-Test
- Chapter 5: Memory Built-In Self-Repair
- Chapter 6: Memory Diagnostics
- Chapter 7: Memory On-Line Testing
- Chapter 8: Testing Content Addressable Memories
- Chapter 9: Testing Non-volatile Memories

Syllabus

- Reference Books
  - 1. **Cheng-Wen Wu**,"*Specific Semiconductor Memory Testing*", Lecture Notes of SOC Consortium, MOE.
  - 2. **Jin-Fu Li**, "*Yield-Enhancement Techniques for Embedded Memories*", Lecture Notes of SOC Consortium, MOE.
  - 3. **Wang, Wu, and Wen**, "*VLSI Test Principles and Architectures*", Elsevier, 2006.
  - 4. **van de Goor**, "*Testing Semiconductor Memories*: Theory and Practice", John Wiley & Sons, Chichester, England, 1991.
- Grading
  - Homework (30%); Midterm (40%); Project (30%)
- **Key dates**
  - **Midterm: 10:00-12:00, Tues, April 29, E1-120**
  - **Project Proposal: May 13**
  - **Project Presentation: June 15 and June16**
  - **Project Report: By 17:00, June 20.**