EE8054 Semiconductor Memory Testing—Homework 2

1. **Fault Modeling**
   Figure 1 shows a dynamic ternary CAM cell. Please model comparison faults for the TCAM cell and verify your fault models using Hspice.

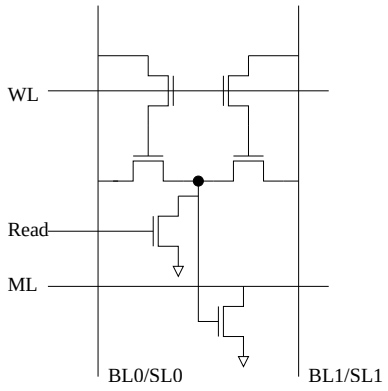

Figure 1: A dynamic TCAM cell.

2. **Test Pattern Generation**
   Figure 2 depicts an 8-bit prefix computation logic. Derive test patterns which can cover all stuck-at faults of the circuit.

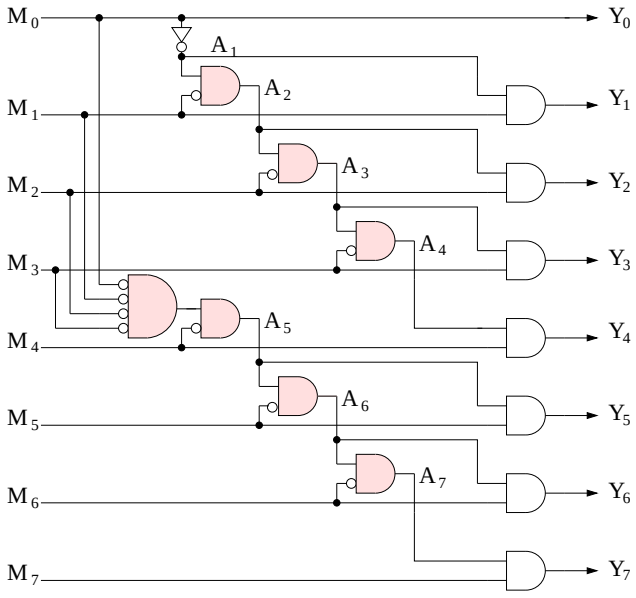

Figure 2: An 8-bit prefix computation logic.