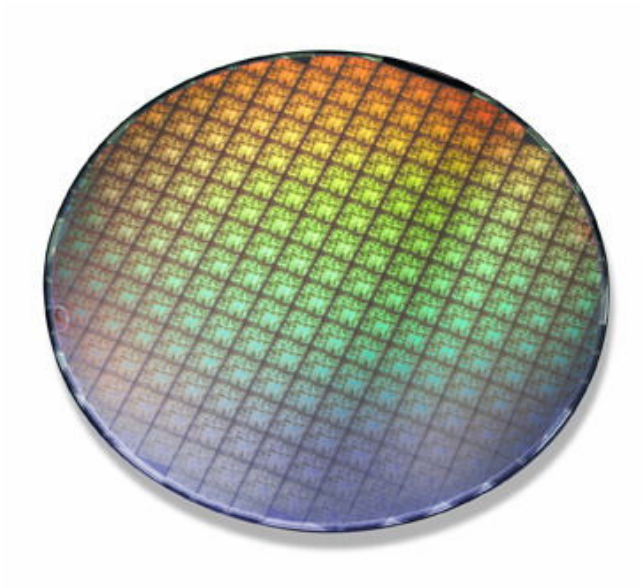
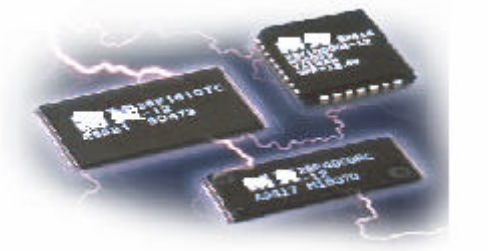
Memory Testing Introduction





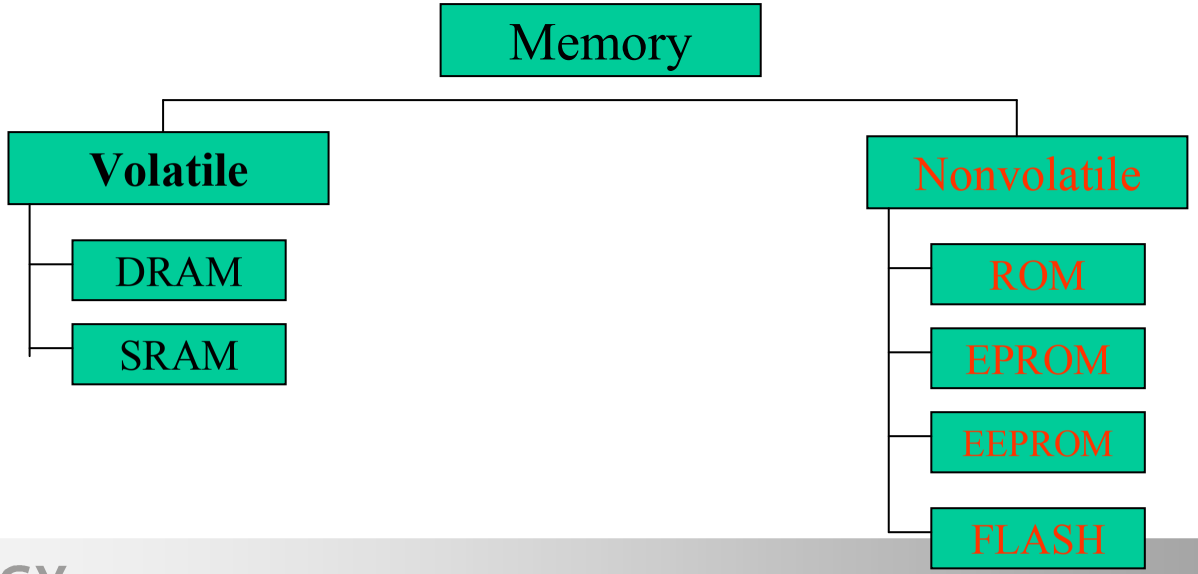
Contents

- Memory Devices Introduction
- Memory Testing Methodology
- Memory ATE & Integration
- Memory Testing Challenges
- Q&A

Memory device type

- **Volatile**- the memory array loses its contents when power is removed - SRAM,DRAM

- **Non-Volatile** - It doesn't lose data after power is turned off - ROM,EPROM,EEPROM,Flash



Memory Summary

	Volatile		NV	
	DRAM	(p)SRAM	NOR	NAND
Mainstream Density	**512M-1G**	**32-64M**	**128-512M**	**2-8G**
Cell	**T+C**	**4-6T**	**Floating Gate**	**Floating Gate**
Addr Interface	**Row, Column**	**Logic Addr**	**Logic Addr, A/D Multiplex**	**IOx bus**
IO Bits	x8, **x16**	**x16(U,L)**	**x16**	x8,**x16**
Control Bits	**CSn, RASn,CASn, WEn**	**CEn,WEn,OEn**	**CEn,WEn,OEn**	**CEn,WEn,REn,CLE, ALE**
Operation	**R,W**	**R,W**	**R,W,E**	**R,W,E**
Access Mode	**Burst**	**As, Burst**	**As, Burst**	**As**
Access Time	**xxx ps**	**xx ns**	**xx ns**	**xx us**
Partition	**Bank,Row,Col**	**Row, Col**	**Sect, Row, Col,(Partition)**	**Block, Page, Column**
Embedded Controller	**no**	**no**	**yes**	**yes**
Major Vendors	**S,H,M,Q,E**	**DH, IDM**	**S,I,ST,**	**S,H,T,IM,R**
Main Application	**PC**	**Celluar**		**iPod**

Memory Features

EPROM

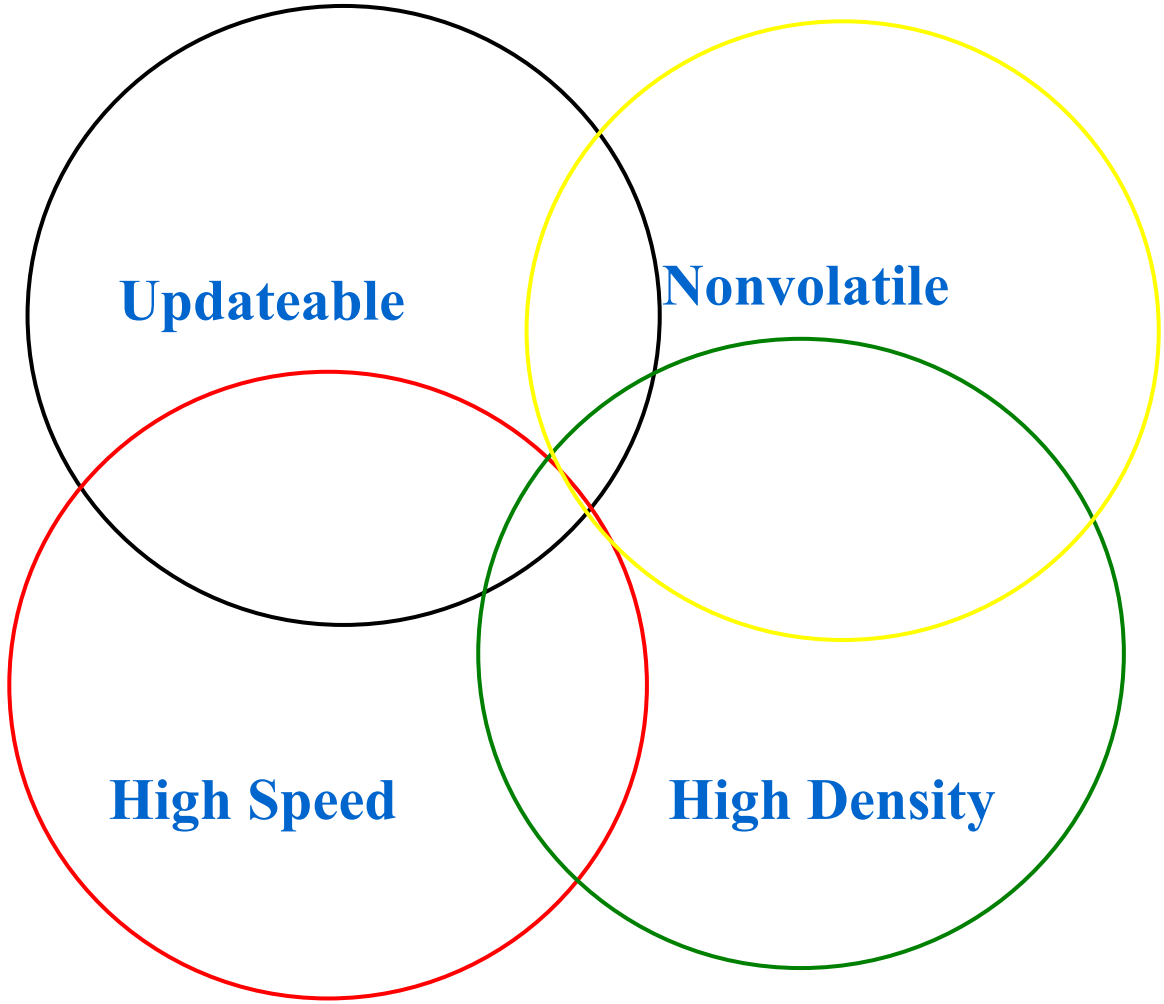
EEPROM

ROM

FLASH

DRAM

SRAM



Source : Intel

Memory Testing Methodology

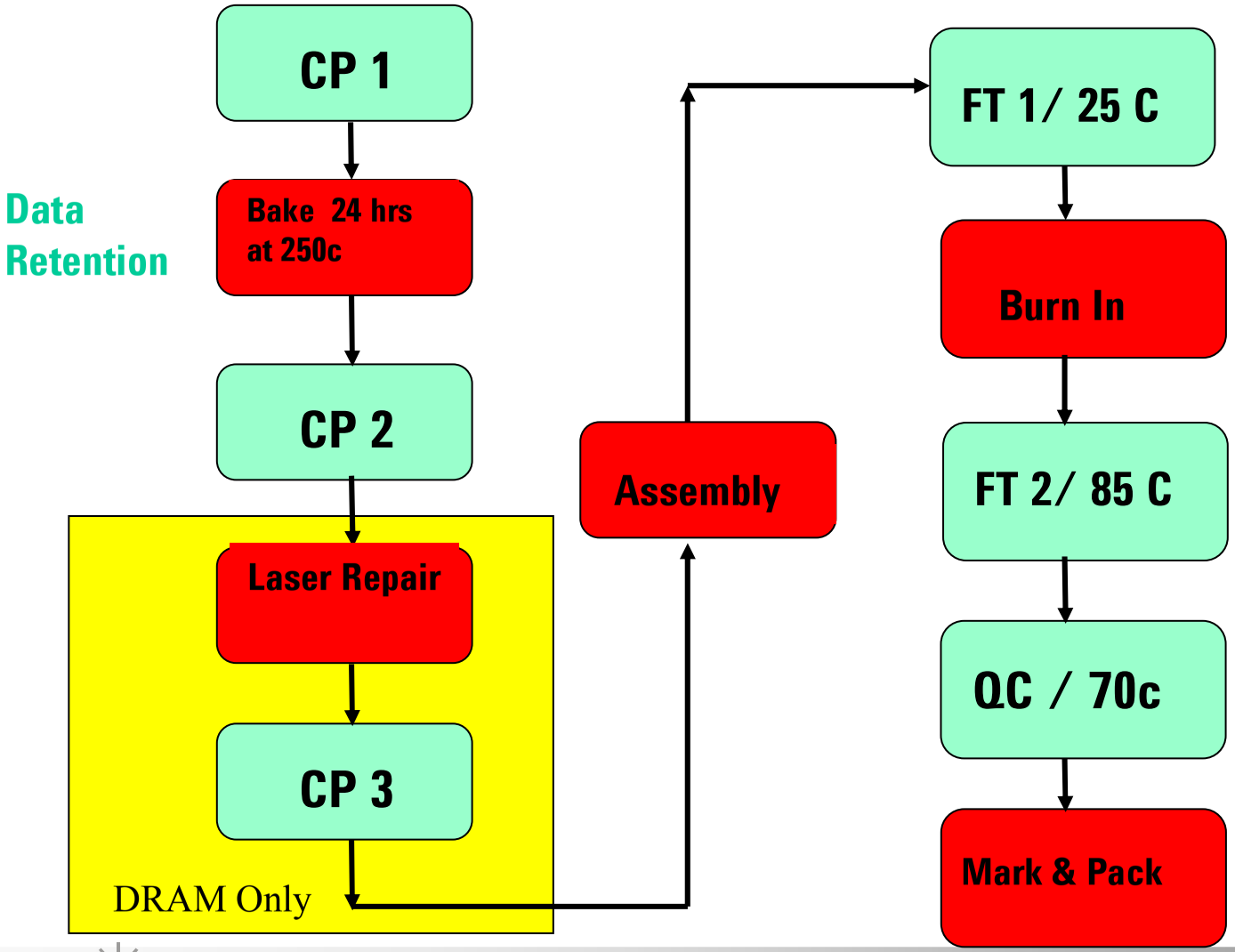
Characterization vs. Production Test

- **Characterization Test**
  - To identify the design and process window.
  - To finalized the datasheet specification.
  - Failure analysis and process debugging
  - Use many tool to get device characterization data, such as bitmap, shmoo, Specs search, thermal stress.
  - Test time is not a issue
- **Production Test**
  - Acceptance test or go/ no-go test
  - Wafer sort, final test, burn in test, speed test, reliability test.
  - Test time = Cost .

Basic Memory Test Items

- Continuity test – open/short
- DC parameter test
  - Input leakage test
  - Output leakage test
  - Output voltage test
  - Output short circuit test
  - Static/Dynamic Idd test
  - ODT(DDRII)
- AC Functional test
  - Timing test (Taa, Toe, Tce, Trc, etc)
  - Memory pattern test (March, Diagonal, Checkerboard, Galloping…)
  - Special test mode(stress, V_{th}, Icell, marginal test, data retention...)
- Redundancy & Repair test (optional)

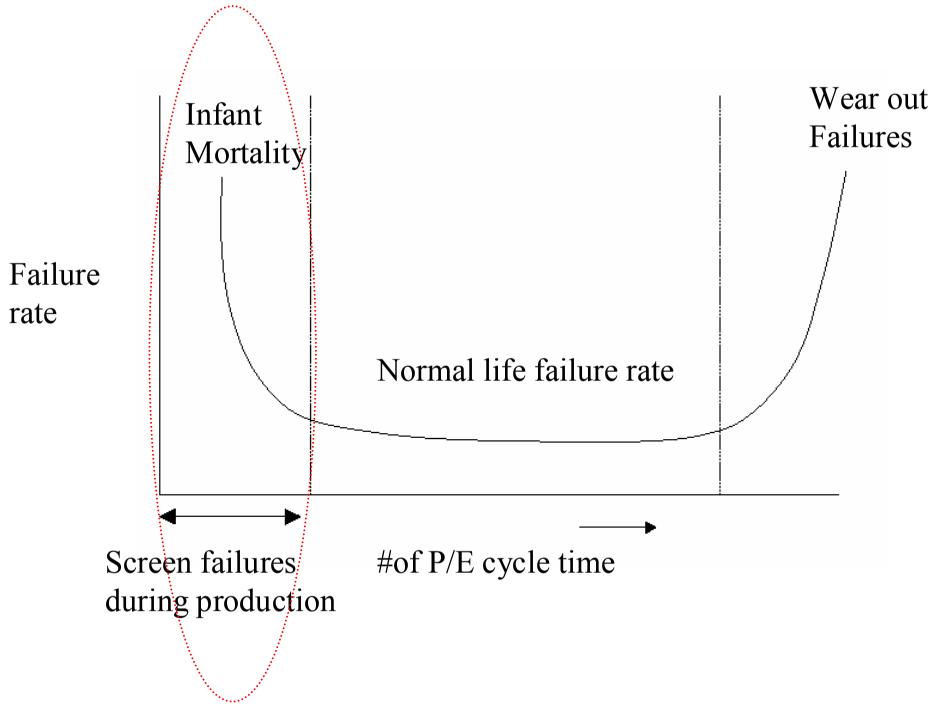
Memory Backend Flow



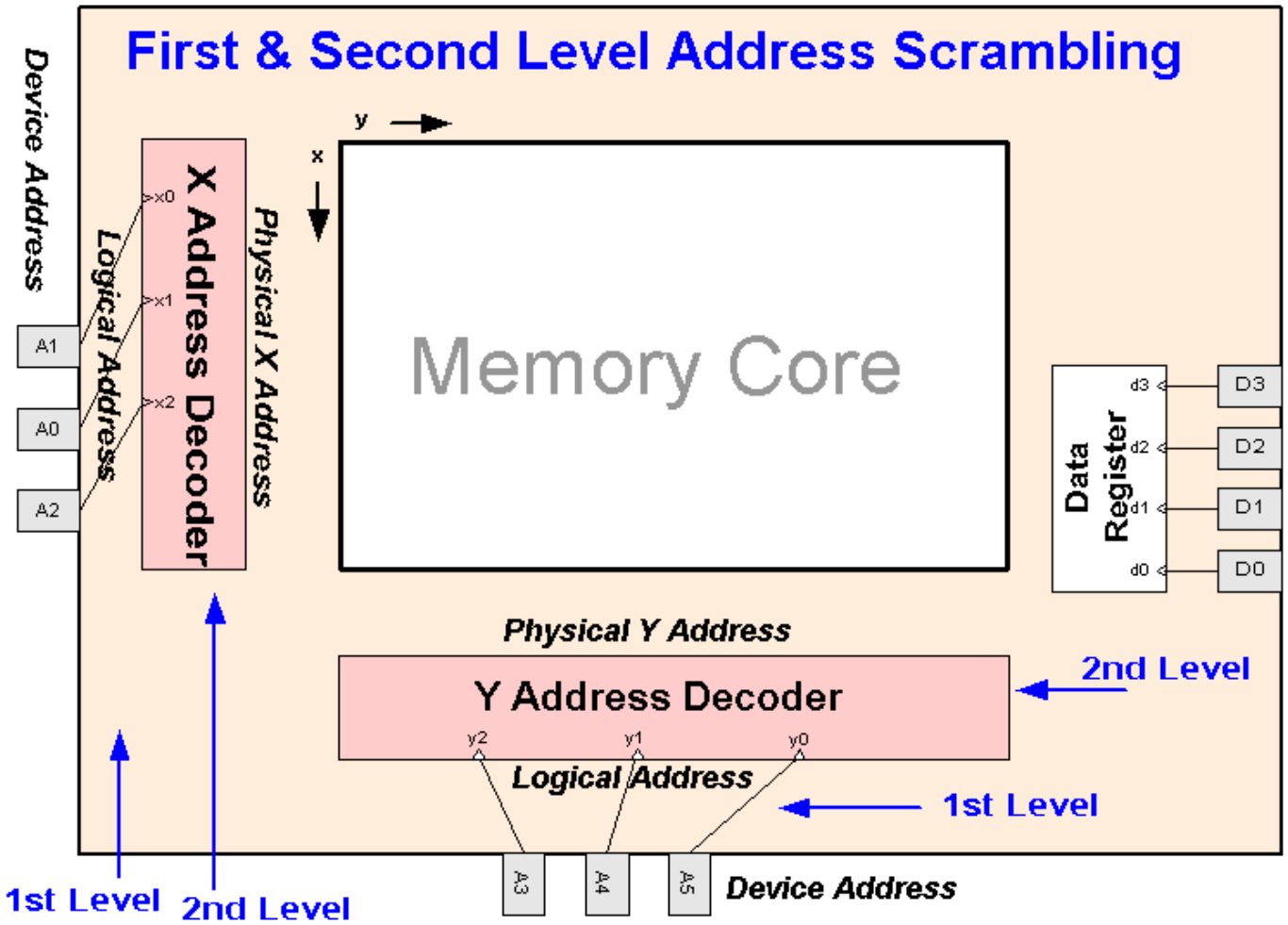
Purpose of Burn-In

High voltage, High temperature(125℃)

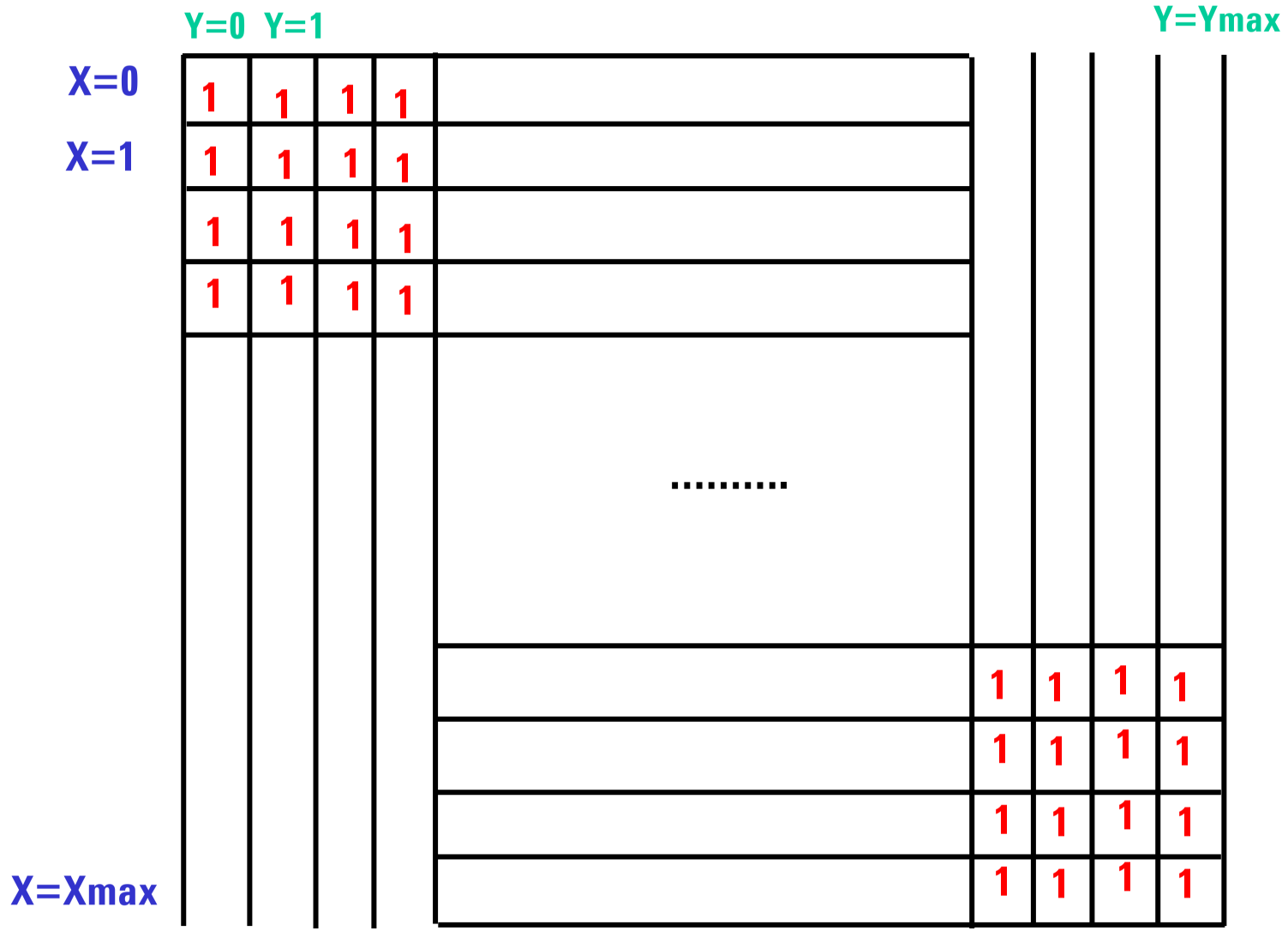
– to screen out infant mortalities



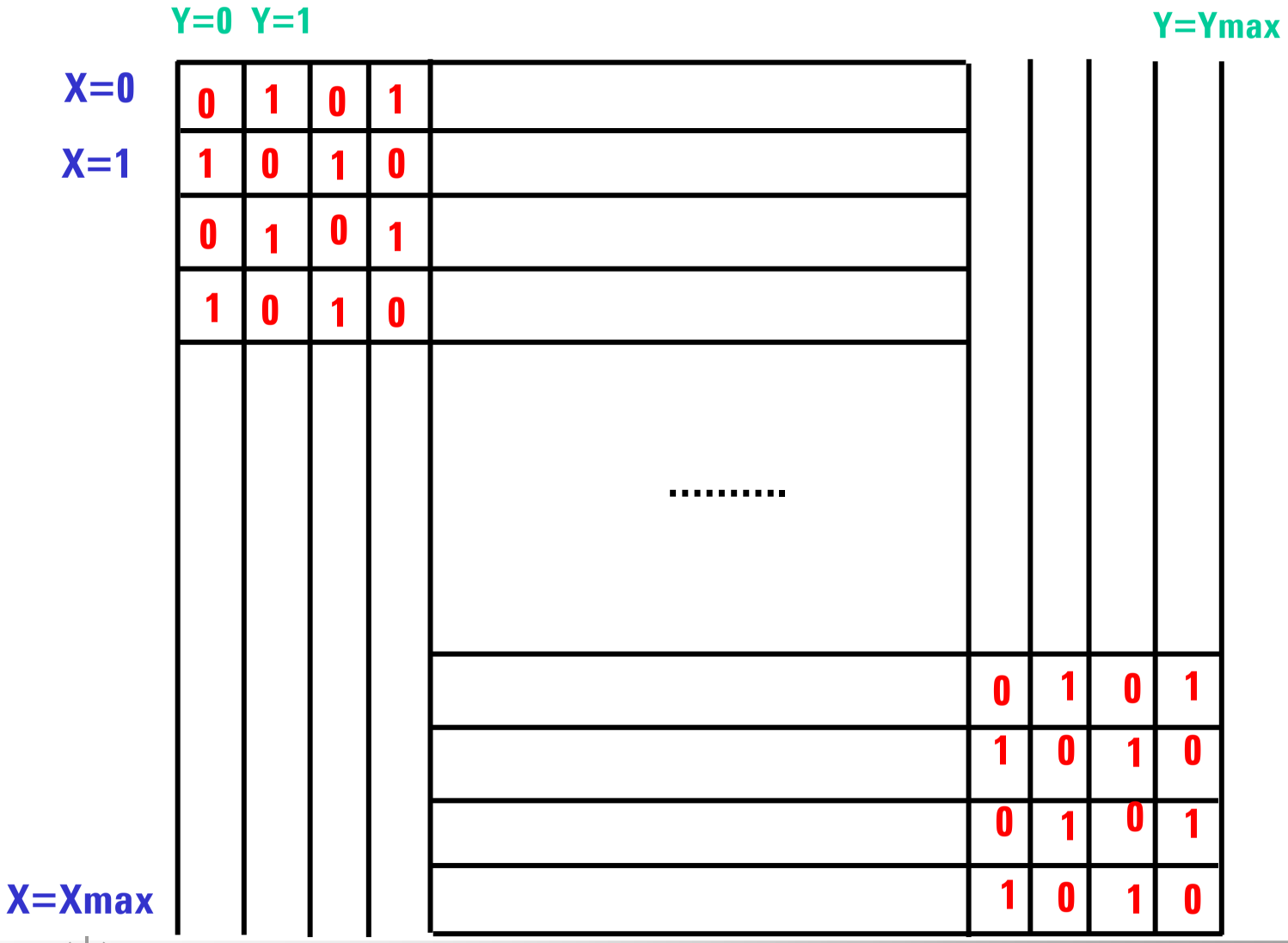
Memory Simplified Block Diagram



Access (R/W) Memory core 1/2



Access (R/W) Memory core 2/2



Memory core v.s. Multiple Table 1/2

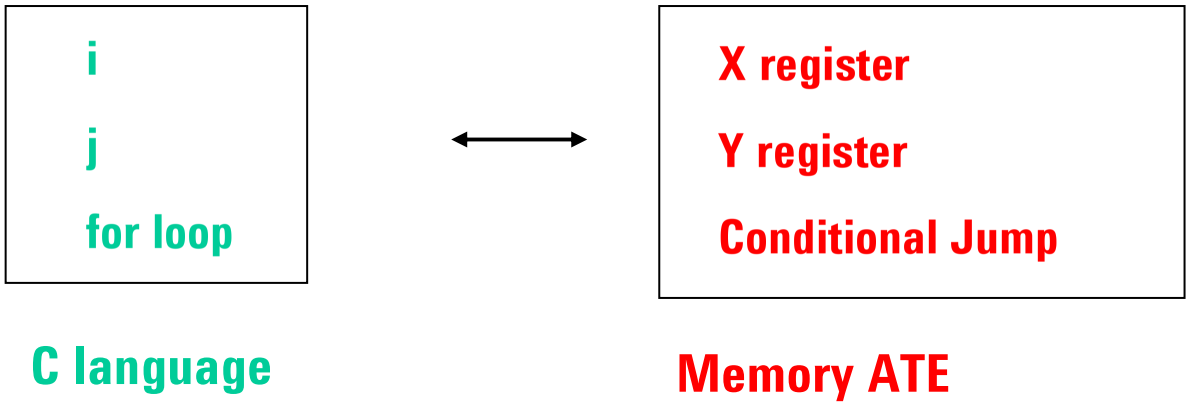
1x1=1	2x1=2	3x1=1	4x1=4	8x1=8	9x1=9
1x2=2	2x2=4	3x2=2	4x2=8	8x2=16	9x2=18
1x3=3	2x3=6	3x3=3	4x3=12	8x3=24	9x3=27
1x4=4	2x4=8	3x4=12	4x4=16	8x4=32	9x4=36
1x5=5	2x5=10	3x5=15	4x5=20	8x5=40	9x5=45
1x6=6	2x6=12	3x6=18	4x6=24	8x6=48	9x6=54
1x7=7	2x7=14	3x7=21	4x7=28	8x7=56	9x7=63
1x8=8	2x8=16	3x8=24	4x8=32	8x8=64	9x8=72
1x9=9	2x9=18	3x9=27	4x9=36	8x9=72	9x9=81

.....

Memory core v.s. Multiple Table 2/2

```
for (i=1 ; i<10; i++)
  for(j=1; j<10; j++)
    printf("%d x %d = %d\n", i, j, ixj);
```

We can use for loop and different variables and set boundary condition in C language, but how to implement similar function in memory tester pattern?



Memory ATE v.s. Logic ATE 1/2

```
cycle1, y= 0; x=0;
cycle2, ymax=0x3ff; xmax=0xffff;
cycle3, c=(ymax+1)*(xmax+1)-1
cycle4, d=expect_data, Data nc;
loop:
 cycle5, y++,x++(ymax), Address nr, Data cn, jump( !c.tc) loop, c--;
cycle6, Data nc;
```

Less than 10 Vectors length

Memory ATE v.s. Logic ATE 2/2

	address	data	control
cycle1,	0..0000000000000000	hlhlhlhl	xxxx;
cycle2,	0..0000000000000001	hlhlhlhl	xxxx;
cycle3,	0..0000000000000010	hlhlhlhl	xxxx;
cycle4,	0..0000000000000011	hlhlhlhl	xxxx;
:			
cycle0x3ffffff,	1..1111111111111110	hlhlhlhl	xxxx;
cycle0x4000000,	1..1111111111111111	hlhlhlhl	xxxx;

64M Vectors length

Memory ATE & Integration

Requirement for memory ATE

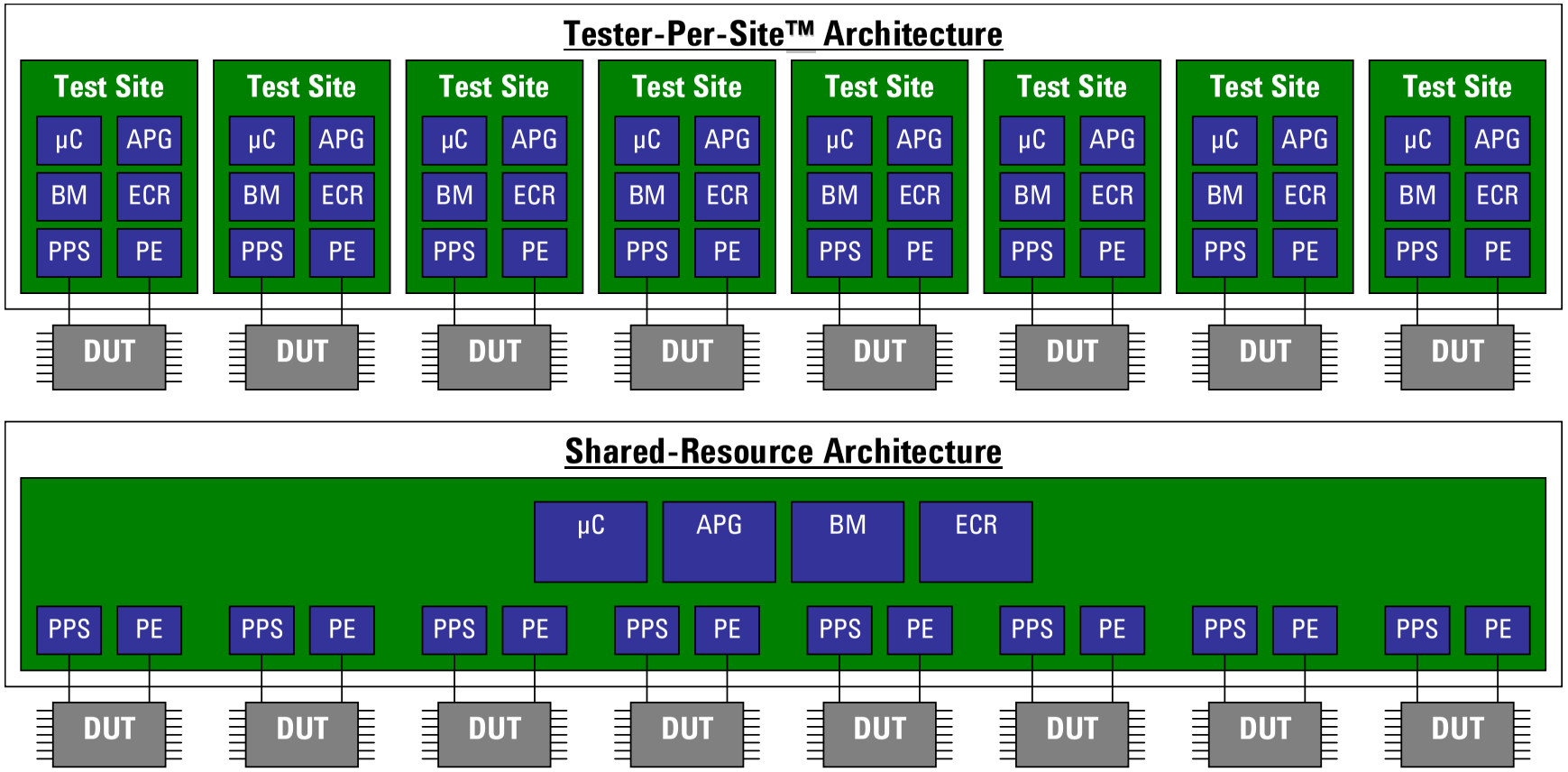
RAM Tester : DRAM,SRAM
pattern generator capability : APG, BM, ECR,...
data width:32/64 or more,interleave,burst,refresh function,...
high speed
powerful redundancy analysis repair

- **NVM Tester** : Flash, Mask ROM, EEPROM,...
- pattern generator capability : APG, BM, ECR...
- high voltage – Vcc, Vpp
- high density buffer memory for mask ROM
- powerful redundancy analysis repair
- Tester-Per-Site™

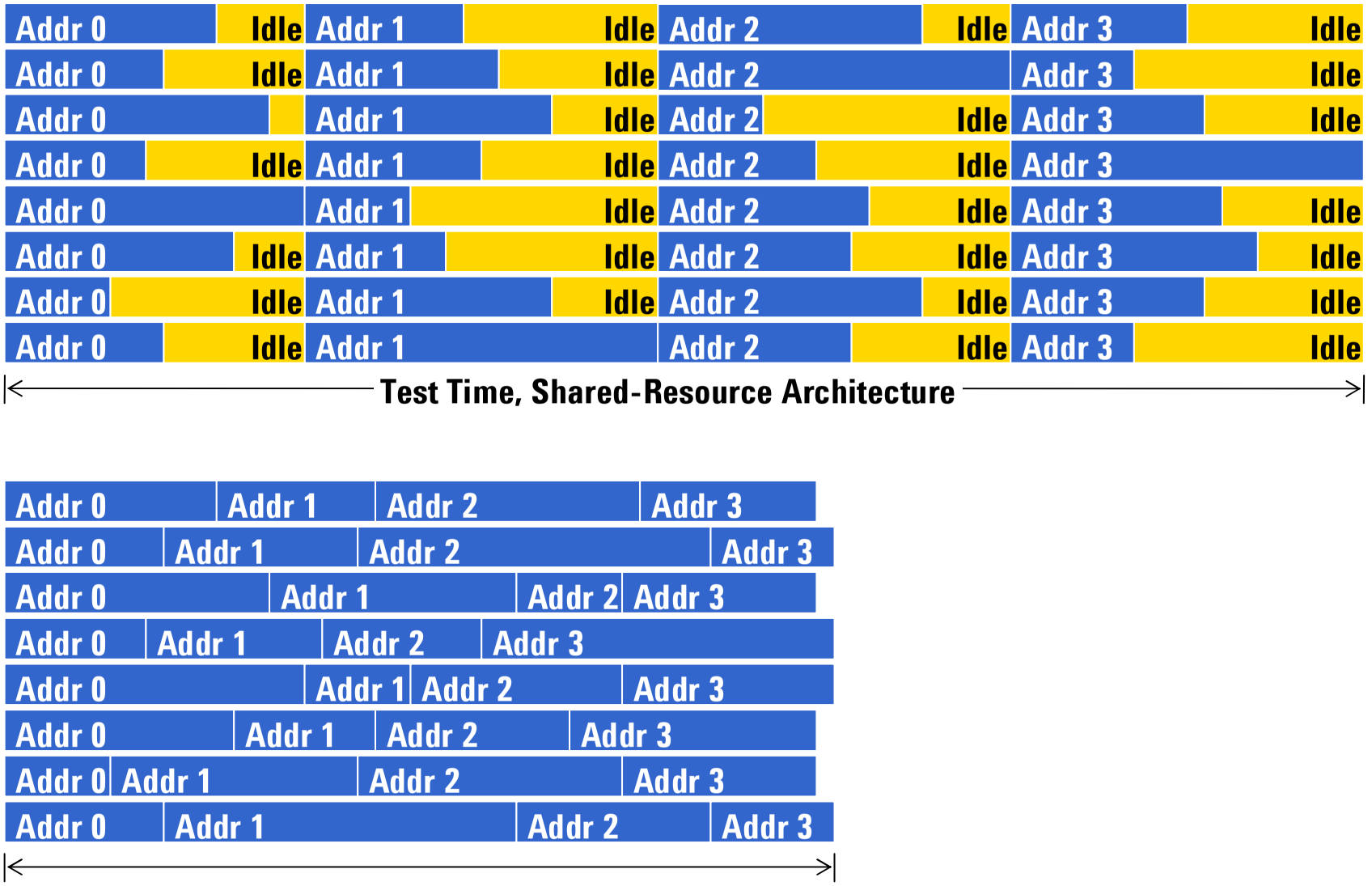
High Speed Tester : XDR, GDDR, DDRIII

- High speed(>2G bps)
- EPA <100 ps
- Small jitter, Wide data Eye

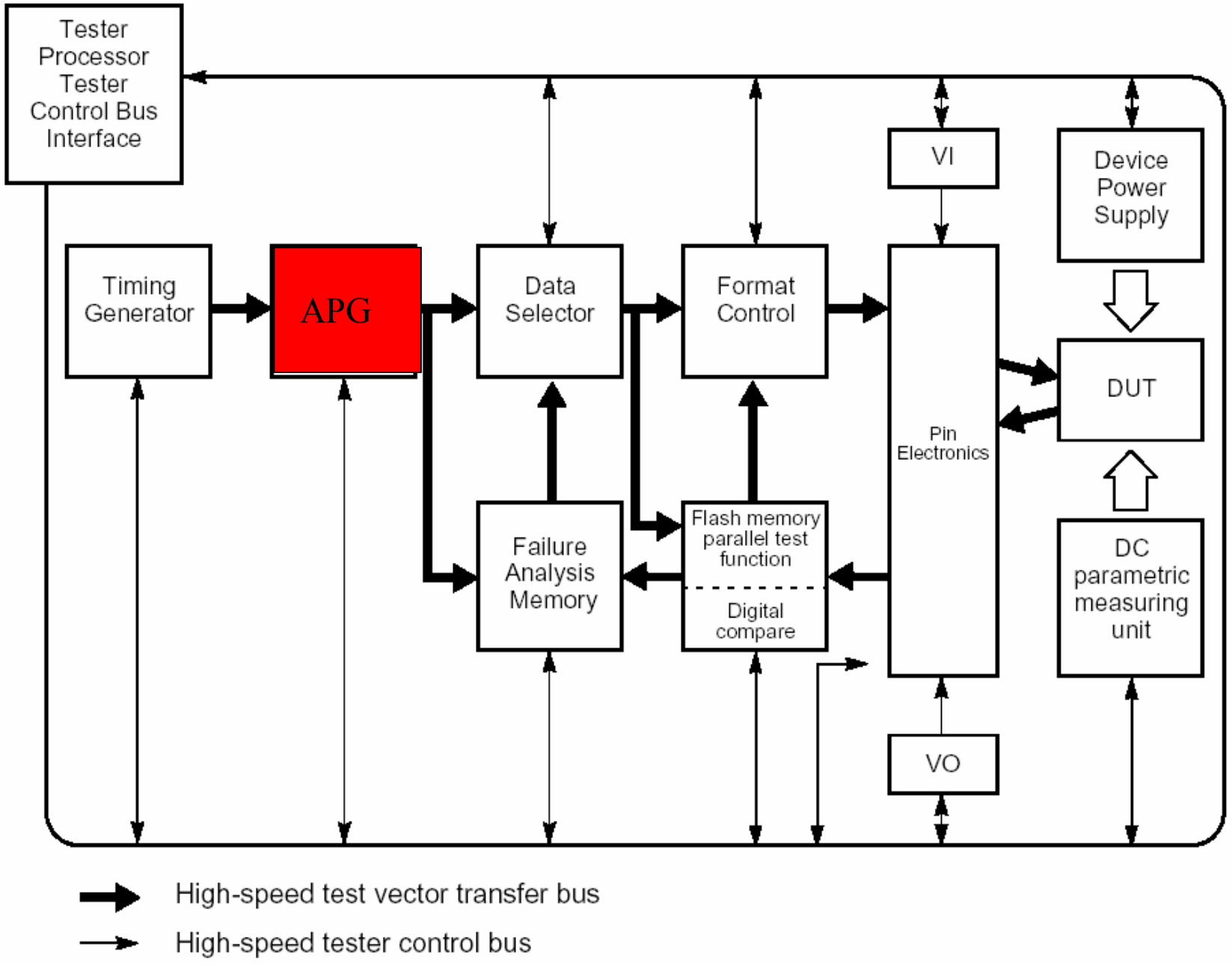
Conventional Test Architectures



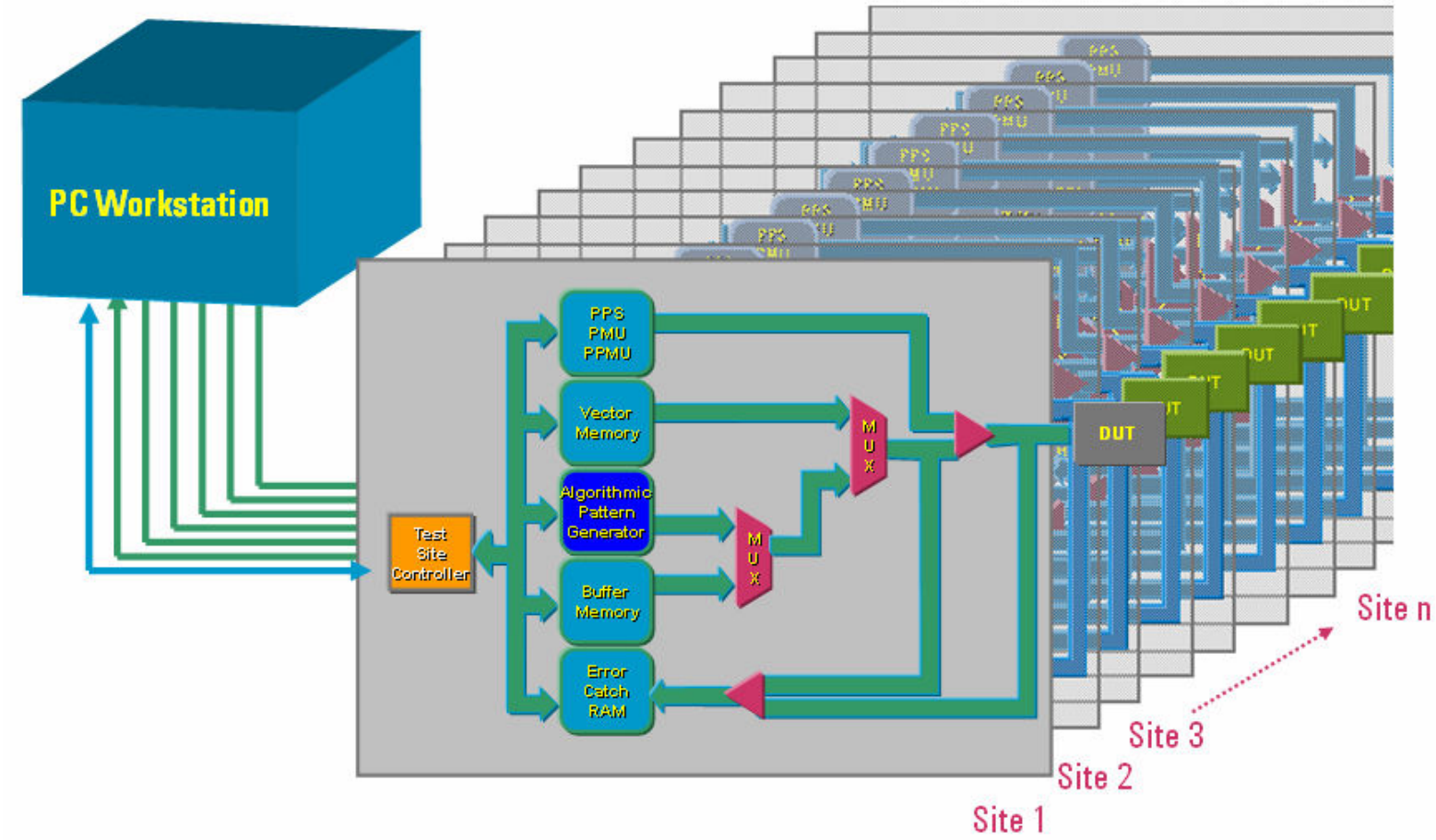
Throughput Comparison



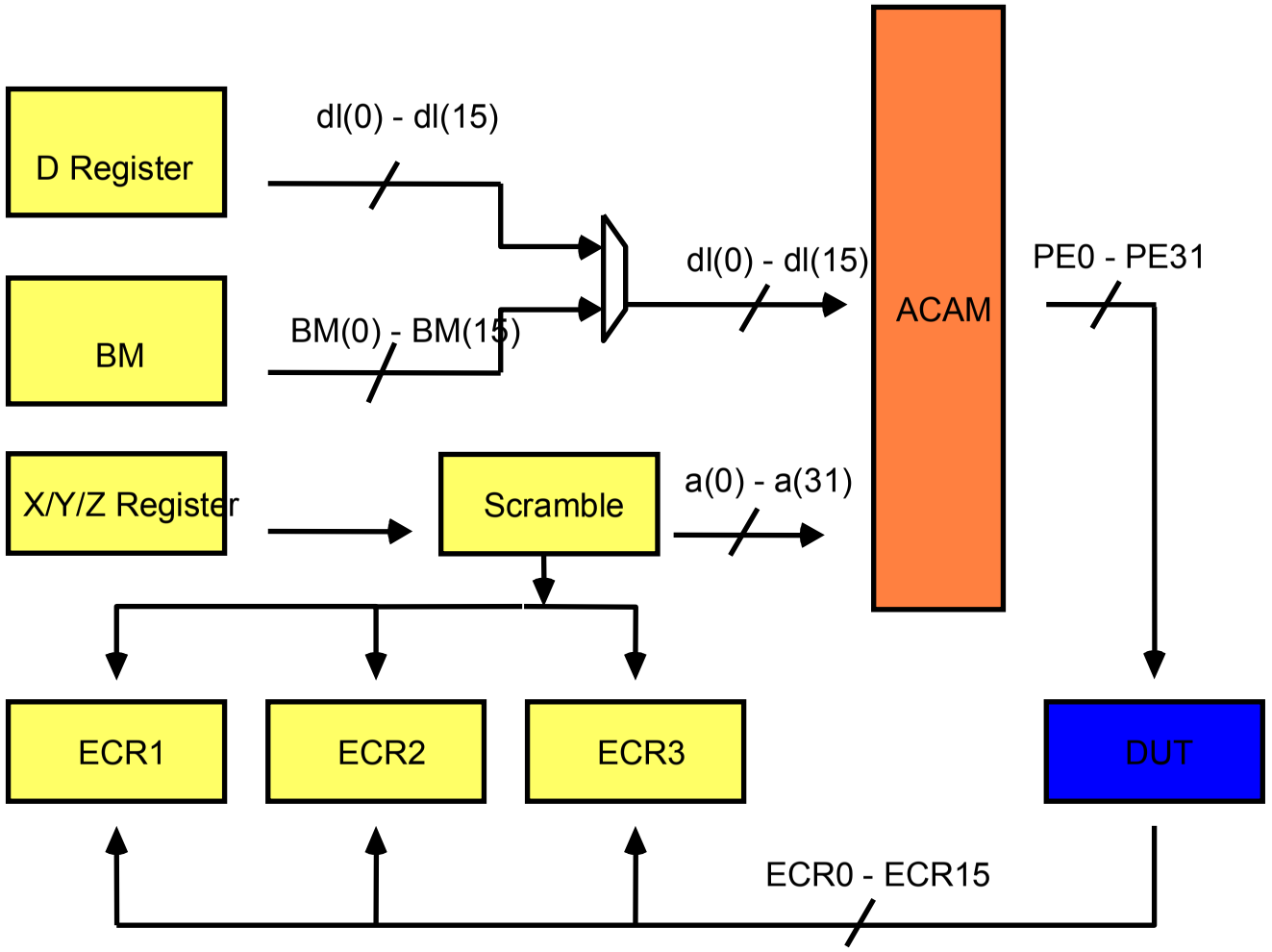
ATE Main Frame Block Diagram



Tester-Per-Site™ Parallel Test Architecture



Memory ATE(APG Resource)

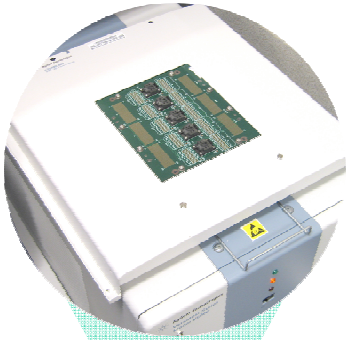


Engineering to High-Volume Manufacturing

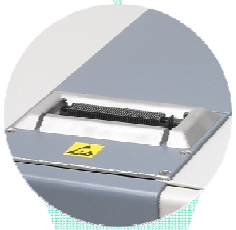
Engineering tester
- Powerful / Flexible
- Good debugging tools
- Convenient
- Easy migrating to production

High-volume manufacturing tester
- Higher through-put
- Lower cost-of-test
- Easy maintain

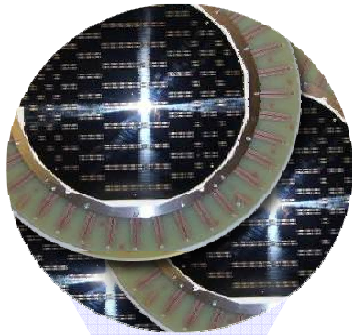
Interface/Interconnect technology



Eng. Matrix – 768 pins
MCP, NOR, NAND development



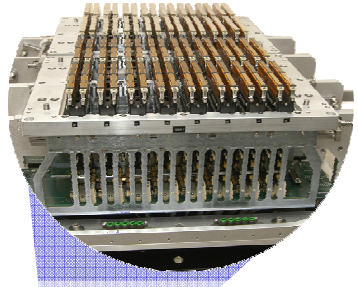
Engineering
4 sites – 128 pins



300mm Wafer Probing
2 TD skip row, 1 TD full wafer

Wafer Sort
144 sites – 4608 pins

DSI
128 NOR, 320 NAND

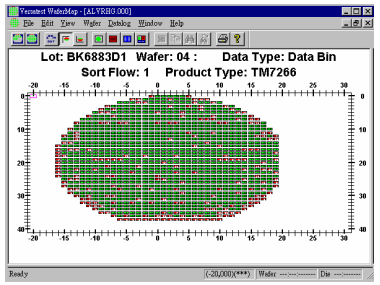


Matrix – 24,576 pins
384 MCP, 384 NOR, >512 NAND

Final Test
128 sites – 4096 pins

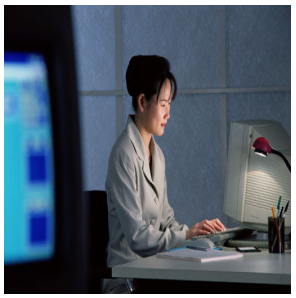
Test Cell Environment

- Tester
- Test head
- Prober(CP) / Handler(FT)
- Load board
- Probe card
- Test program
- Server/CIM system

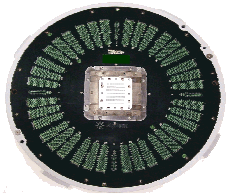


Test result(Wafer Map)

Server/Network



Engineer/Operator

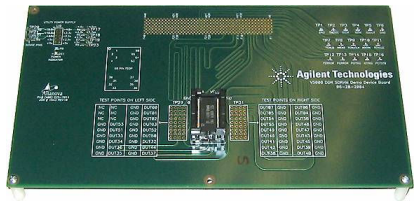


Probe Card

Tester

Prober(CP)

Handler(FT)



Load Board

Economical Test Solution for Memory

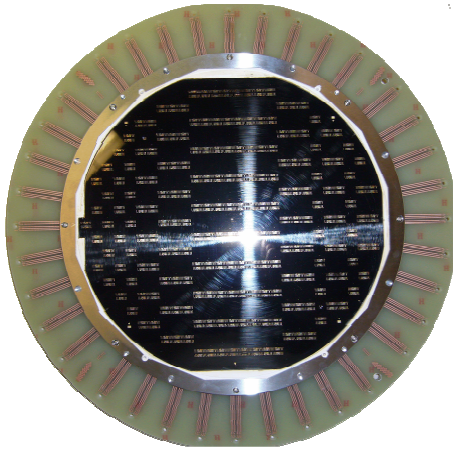
Final Test Configuration

Wafer Sort Configuration

WS 1TD Probe Card solution

144 Test Sites ensure the fastest test times
@ up to 288 devices in parallel

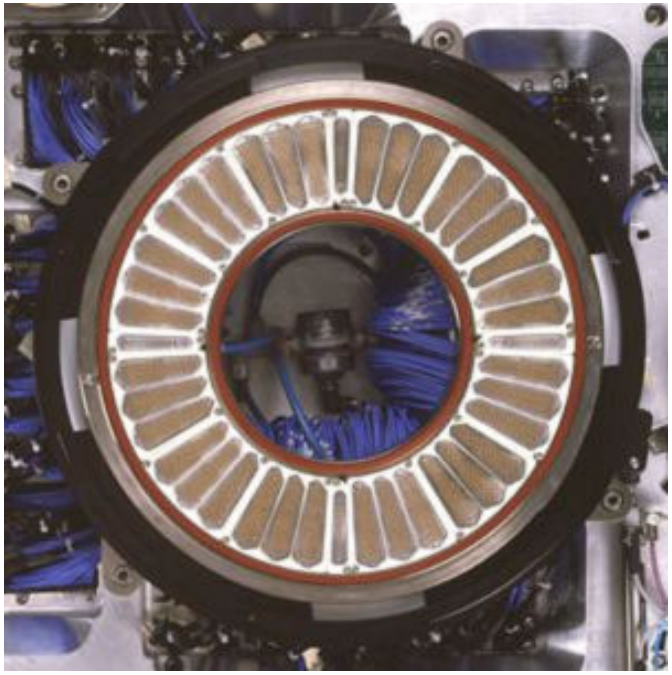
WS interface for full
300mm probing



WS 300mm probecard
1 Touchdown @ 100% efficiency

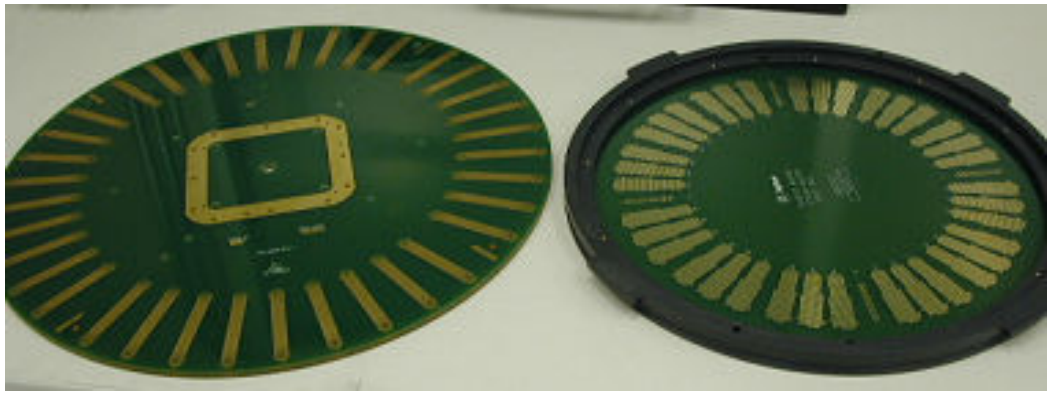
WS Interface

2304 I/O Channels
Vacuum Compression
(Pogos)



4608 I/O Channels
Mechanical Compression
(XZIF)

WS Interface – Probe Card



V5400 vs. V4400

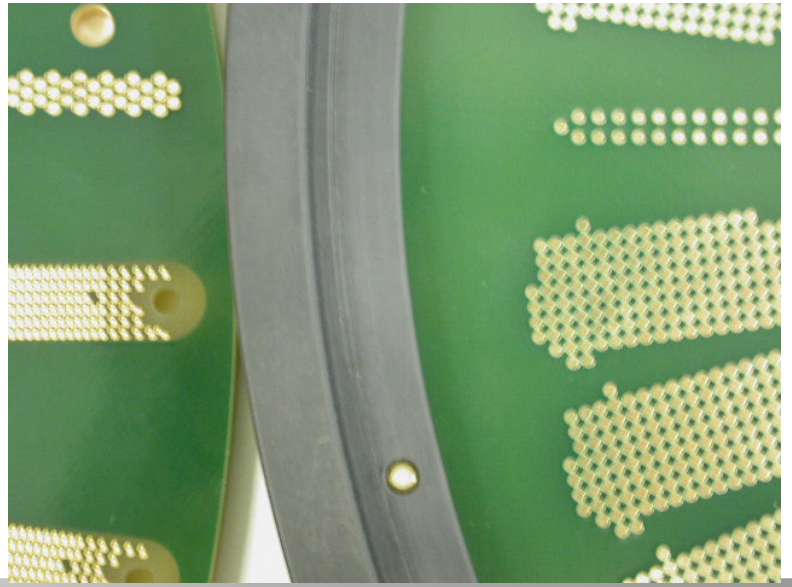
- ***V4400 probe card is 355mm***
- ***V5400 probe card is 440mm***

- ***24% more probe card area***
- ***Double the I/O density***
- ***75% more keep out area***

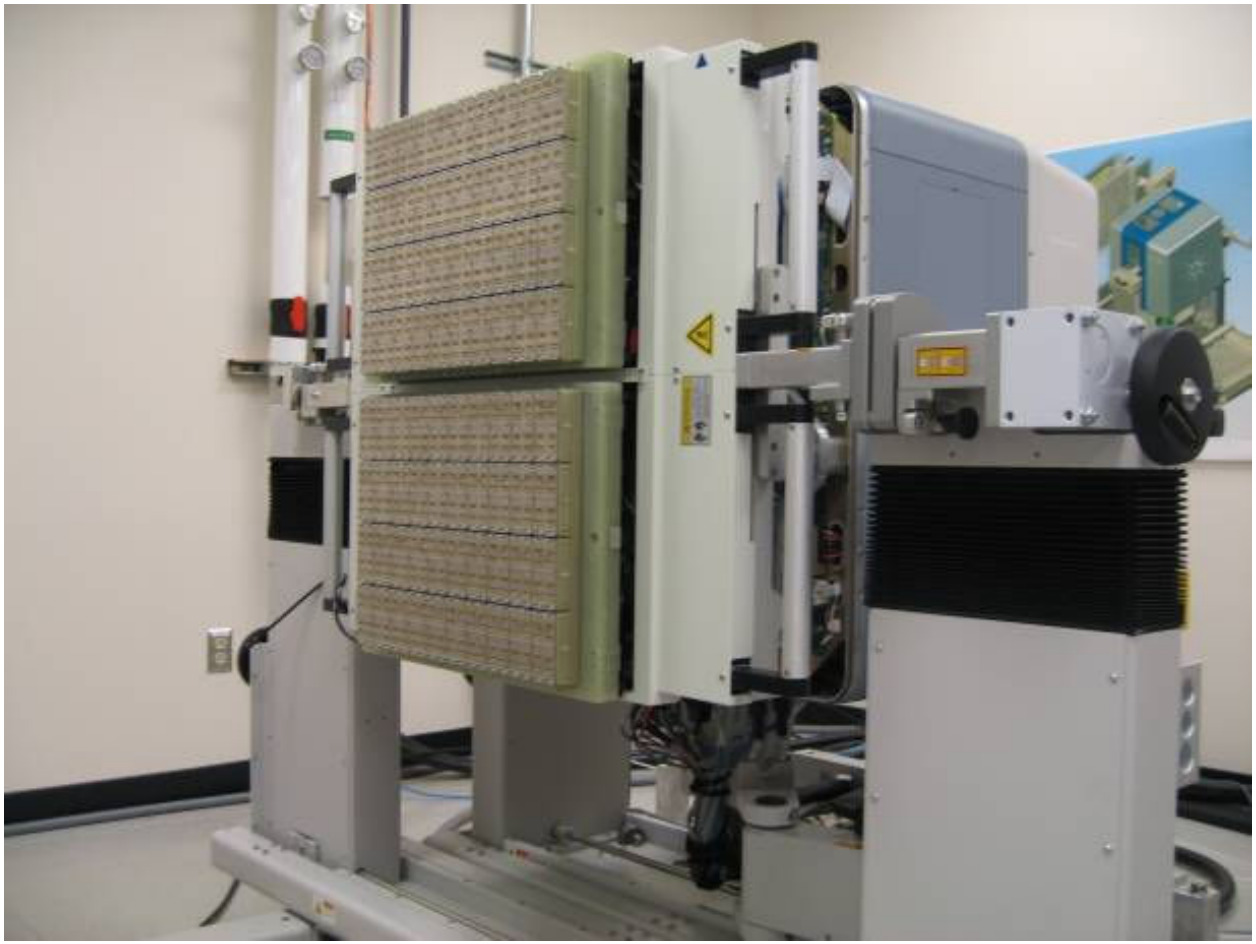
V5400 vs. V4400

- ***V4400 pad density is 70mm***
- ***V5400 pad density is 40mm***

- ***V5400 keep out area is 10" or 250mm***



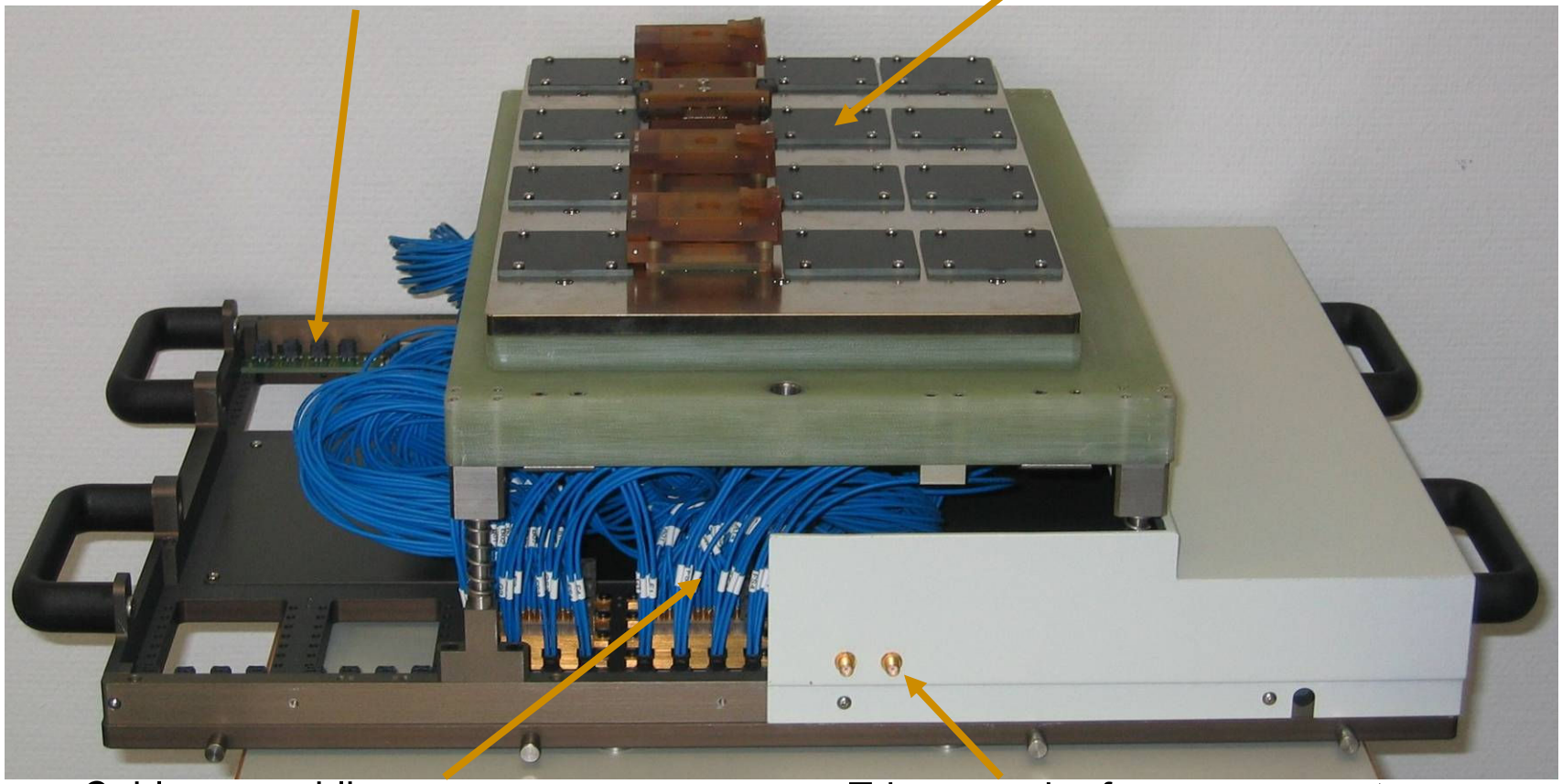
FT Interface: HiFix



HiFix Components

DPS wiring board for 8 DPS channels
8 boards in total

Up to 16 HSM sites



Cable assemblies
(signal and DPS lines)

Trigger and reference connectors
for calibration robot

Memory Test Challenges

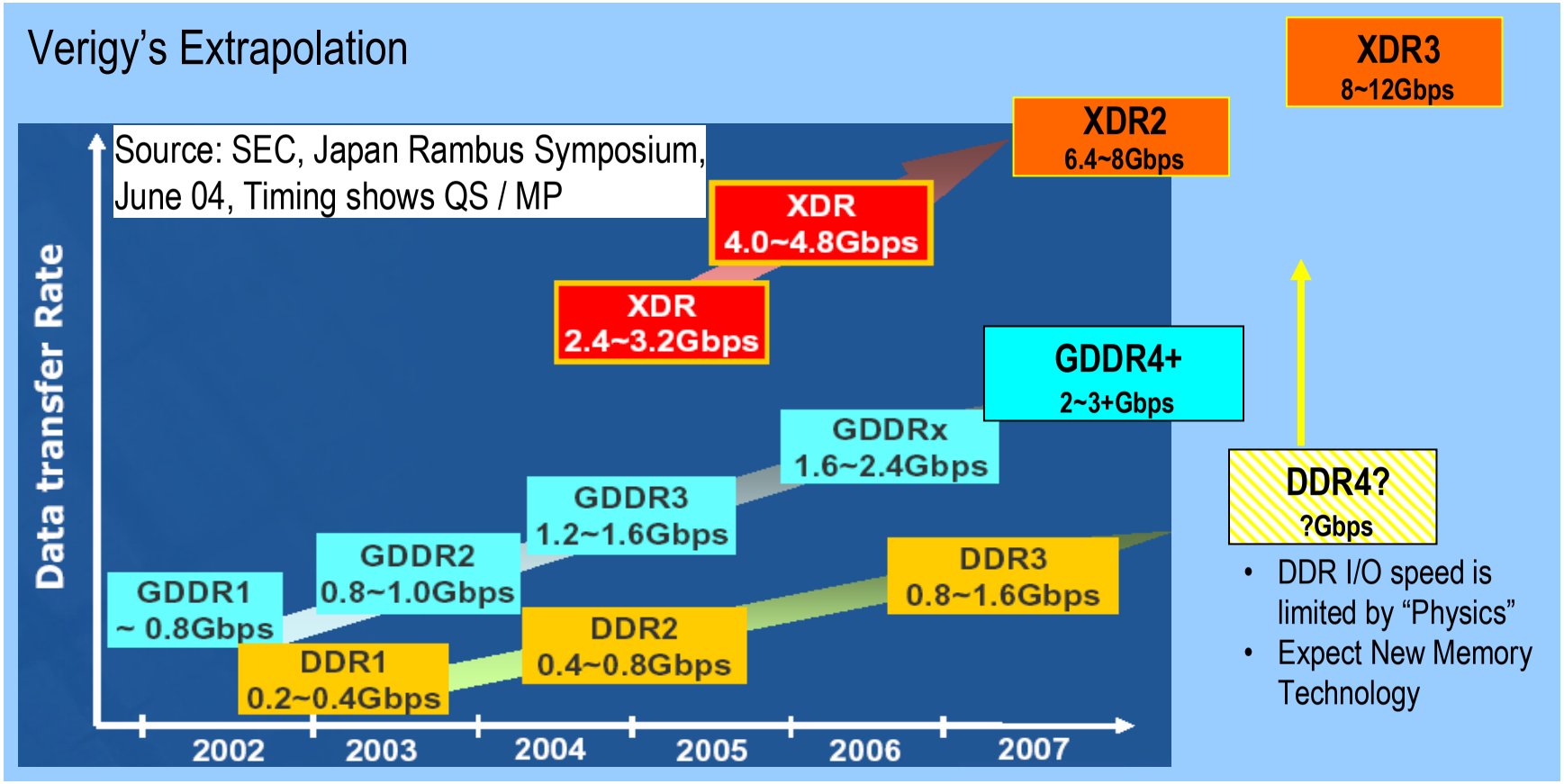
- **High Speed**

- Mix of parts is increasing
  - Flash, DRAM, SRAM
- Increase Parallelism

- Debug tools

- **High throughput**
- **Flexible configuration**
- **Reduced system cost**

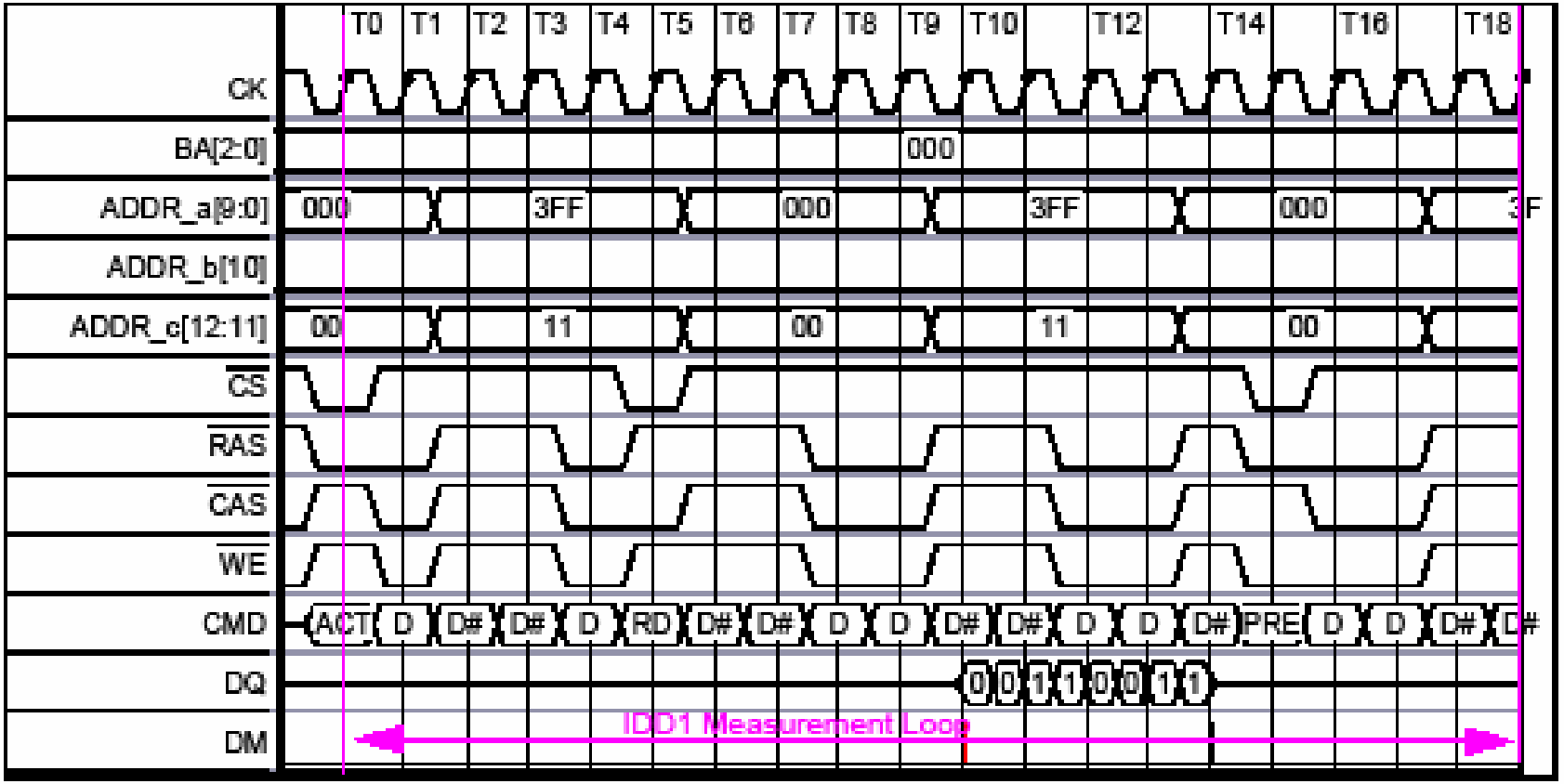
High-Speed Memory Device Roadmap



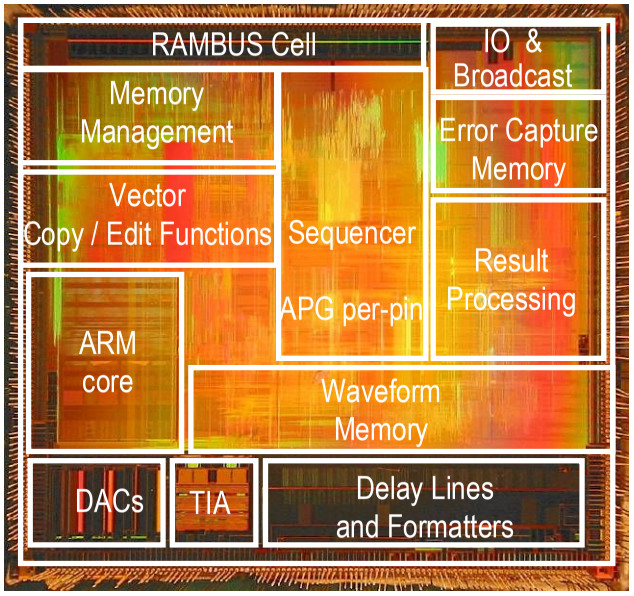
→ Bandwidth demand drive speed of High-Speed DRAMs

→ nm Process technology is used to address speed & density (cost)

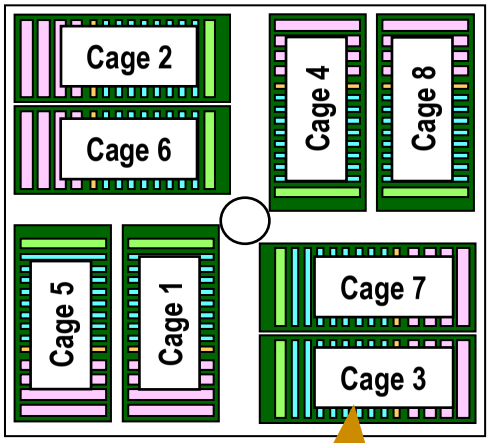
DDRIII Memory



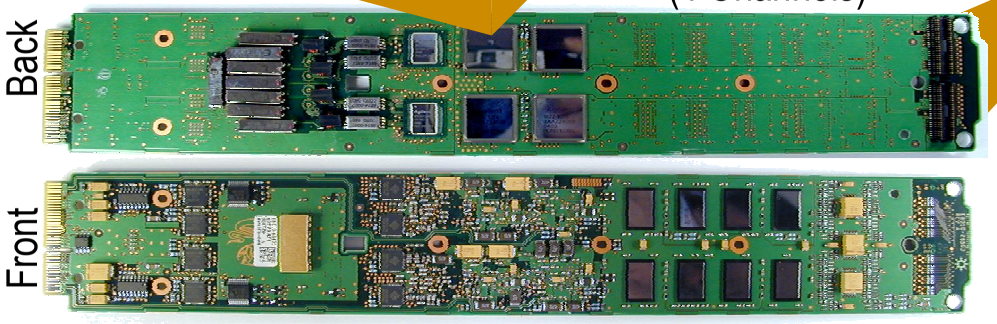
High Speed Solution: Per-Pin Processor

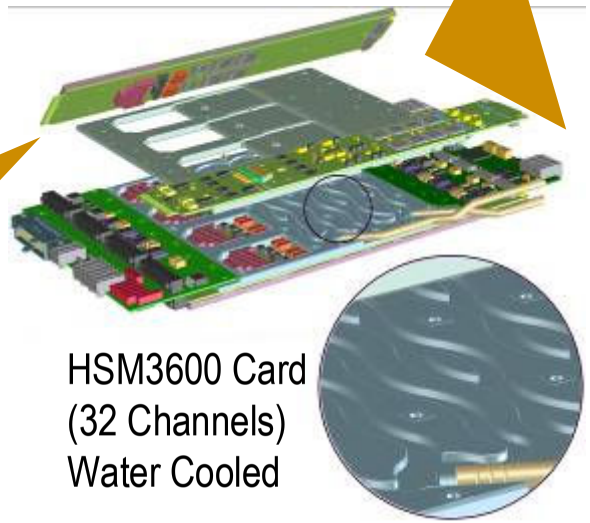


Memory ATE on a Single Chip
(Test-Processor Per-Pin)



HSM3600 Sub-Module
(4 Channels)

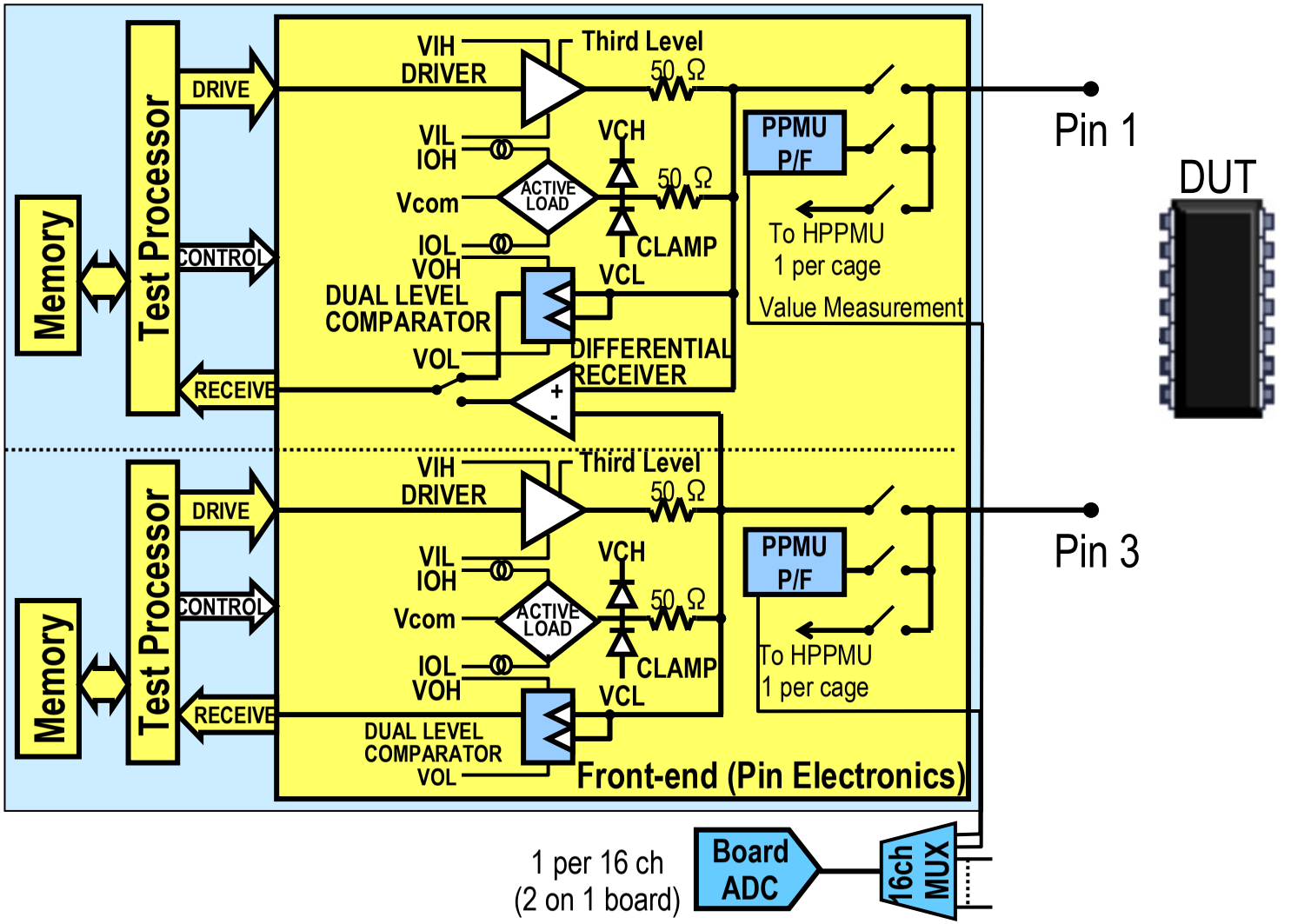




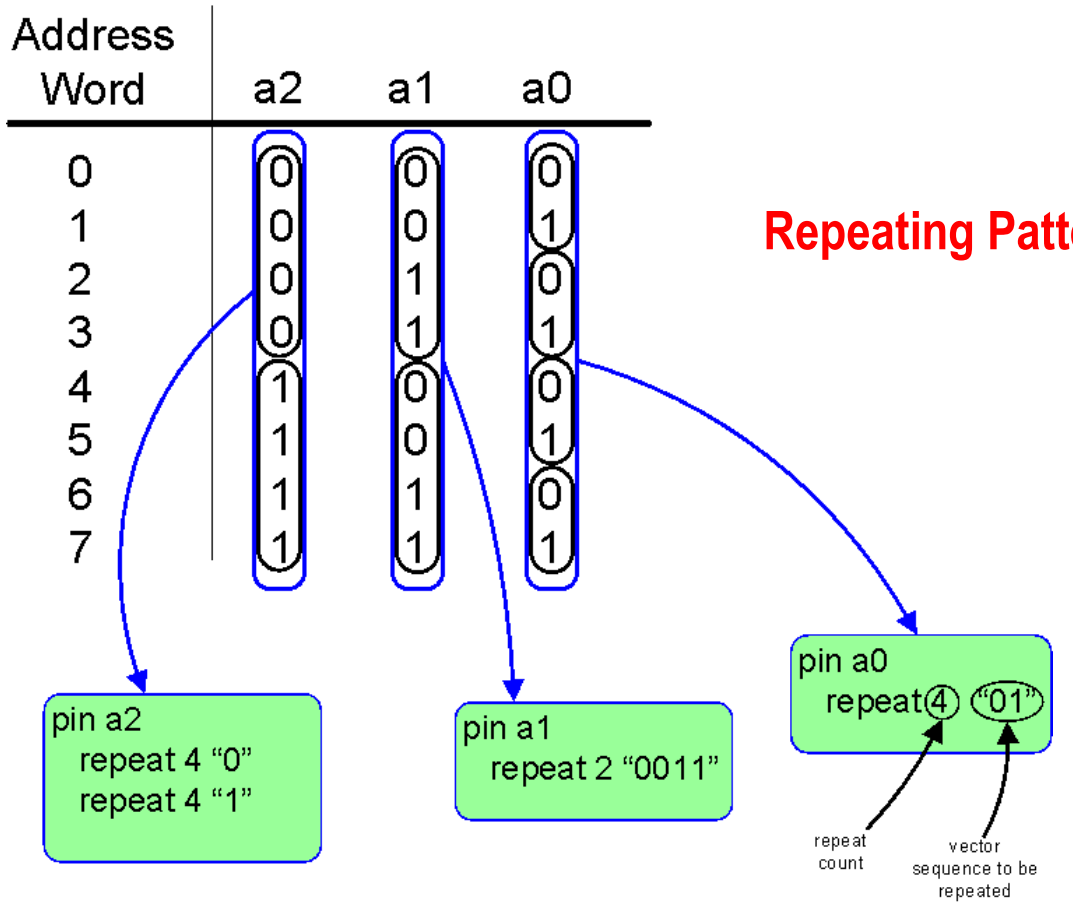
HSM3600 Card
(32 Channels)
Water Cooled

→ TRUE "Memory ATE Per-Pin" enabled by the Test-Processor Technology

High Speed Solution: HW Free APG



High Speed Solution: Per-Pin Complier



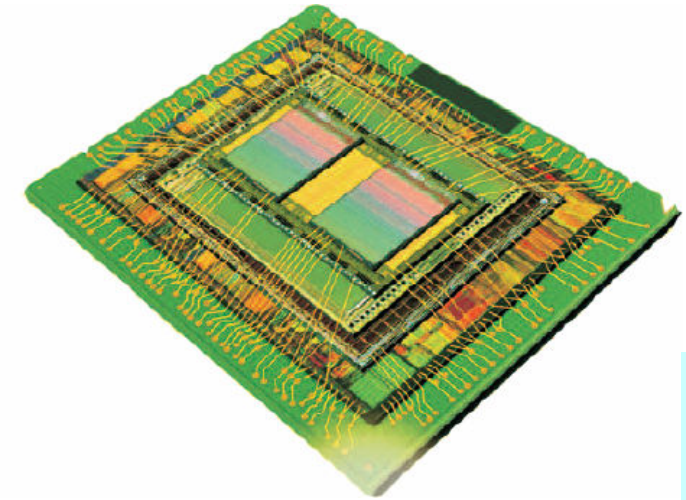
Repeating Patterns on a Pin

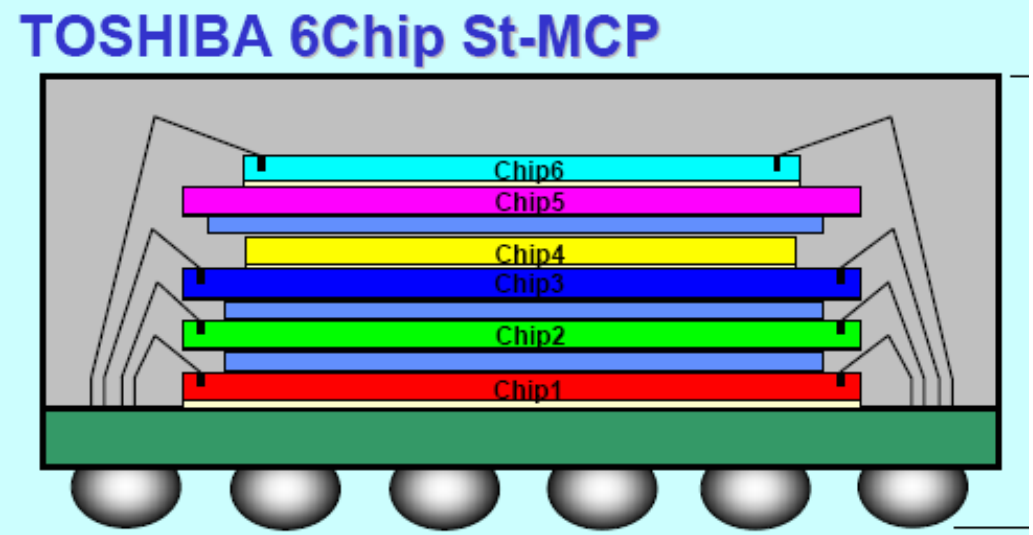
Memory Test Challenges

- High Speed
- **Mix of parts is increasing**
  - **Flash, DRAM, SRAM**
- Increase Parallelism
- Debug tools

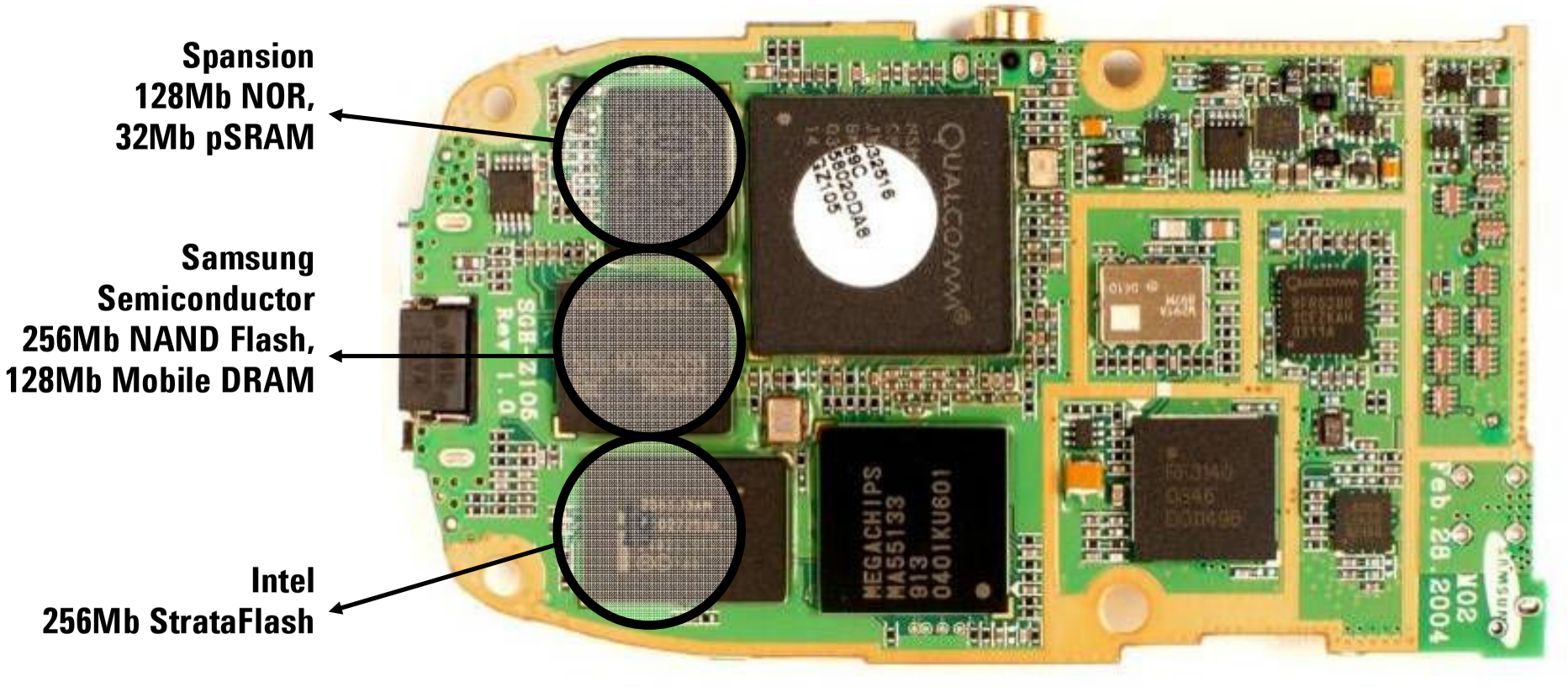
- **High throughput**
- **Flexible configuration**
- **Reduced system cost**

Multi Chip Package (MCP)





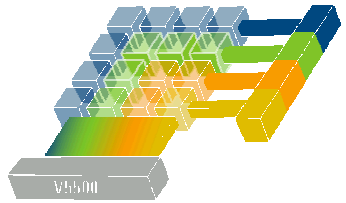
100% of modern cell phones use MCPs



A streaming video phone with 0.3MP Camera

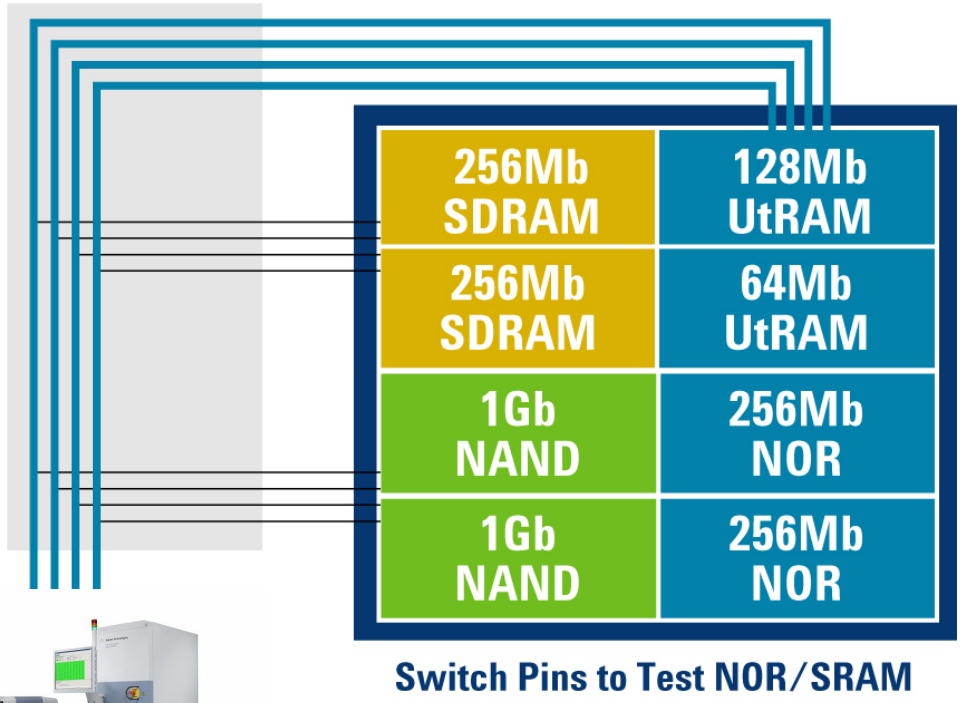
Source: iSuppli Corp.

Dynamic Interface: Matrix



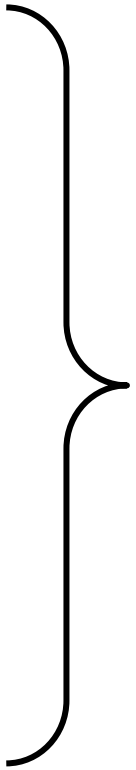
1) Dynamic Interface design to access different Memory parts

2) Dynamic APG minimizes test time and allows for concurrent testing



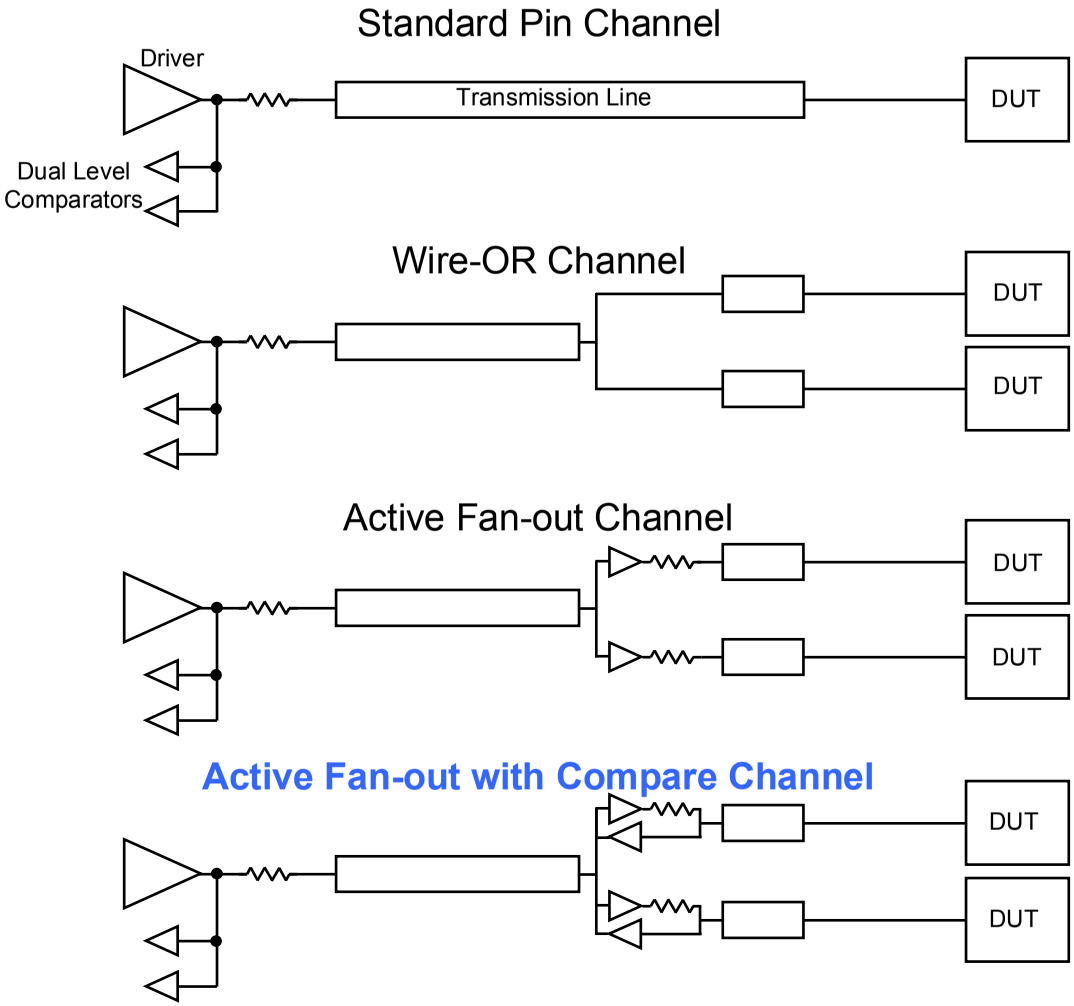
Memory Test Challenges

- High Speed
- Mix of parts is increasing
  - Flash, DRAM, SRAM
- **Increase Parallelism**
- Debug tools



- **High throughput**
- **Flexible configuration**
- **Reduced system cost**

Increase Parallelism: PE Share



- Good Signal Quality (Yield)
- Low Parallelism (Throughput)
- High Cost

- High Parallelism (Throughput)
- Lowest Cost
- Degraded Signal Quality (Yield)
- Device Interaction (Yield)
- Serial Reads (Throughput)

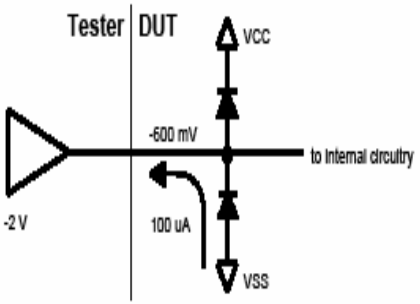
- Better Signal Quality (Yield)
- High Parallelism (Throughput)
- Better Cost
- Serial Reads (Throughput)

- Better Signal Quality (Yield)
- High Parallelism (Throughput)
- Better Cost
- Parallel Reads (Throughput)

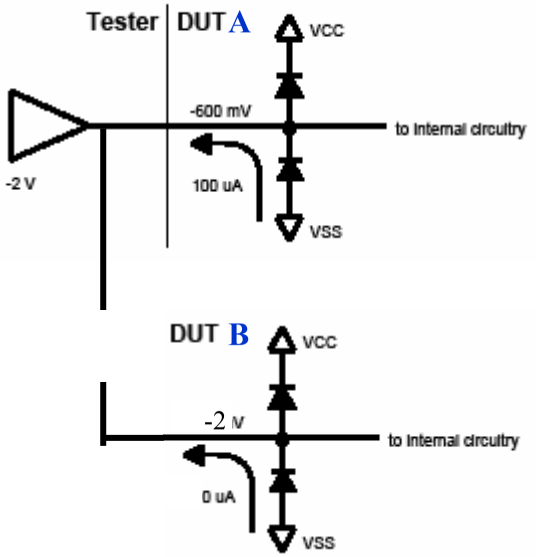
Side effect at PE Share 1/2

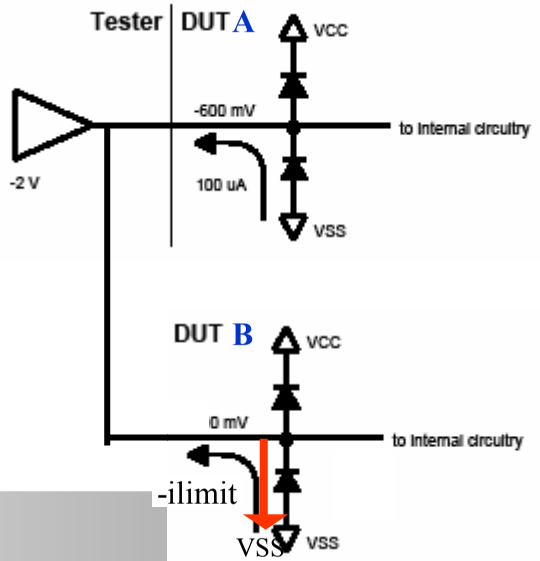
2. OpensShorts()

In this exercise, we will work with a parametric test function. OpensShorts has been pre-coded. Don't forget to uncomment this function in DoTestProgram(). To test open pins, we want to force –2 V and clamp the current at 100 uA (FIMV) and fail all pins where the measured PMU current is greater (less negative) than –80 uA. The theory is, if the PMU attempts to drive a –2 V on a DUT pin, it forward –biases an internal protection diode, which turns on and conducts current at the negative PMU current limit of –100 uA. In this case, the PMU current clamp holds the PMU equilibrium output voltage at –600 mV, not –2 V. If the pin is open, PMU current is 0 uA, and voltage is –2 V.

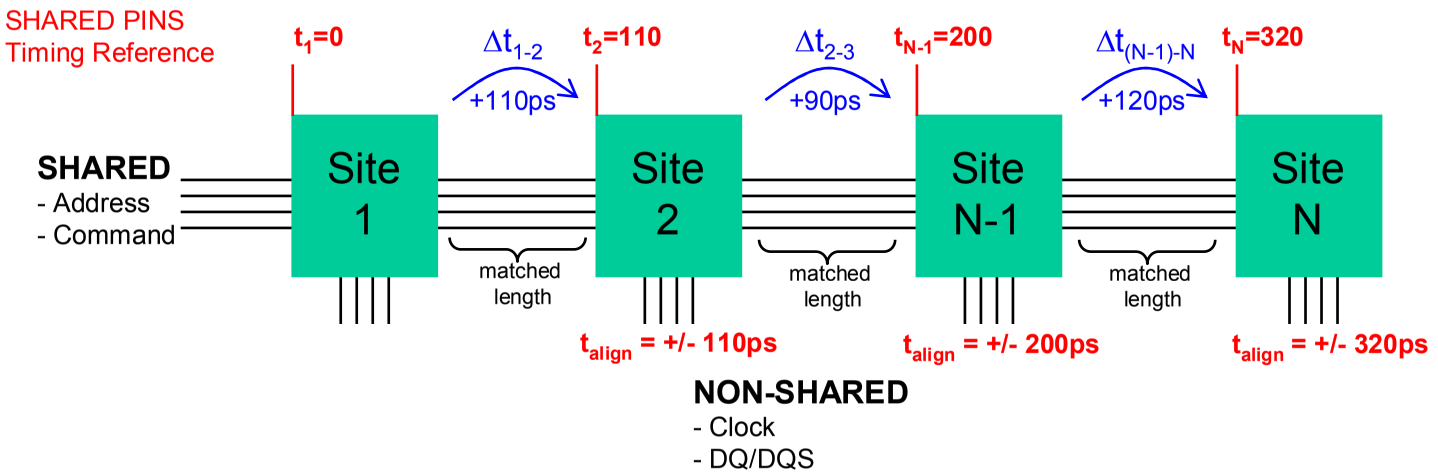


To test short pins, we want to force –2 V and clamp the current at 100 uA (FIMV) and fail all pins where the measured PMU voltage is greater (less negative) than –300 mV. The theory is, if the pin is shorted to another pin, we should measure 0 V on the pin because it is shorted to pins that are driven to 0 V (The device has been pre-conditioned to drive 0 V on all pins in the pre-coded part of the function OpensShorts()).





Side effect at PE Share 2/2



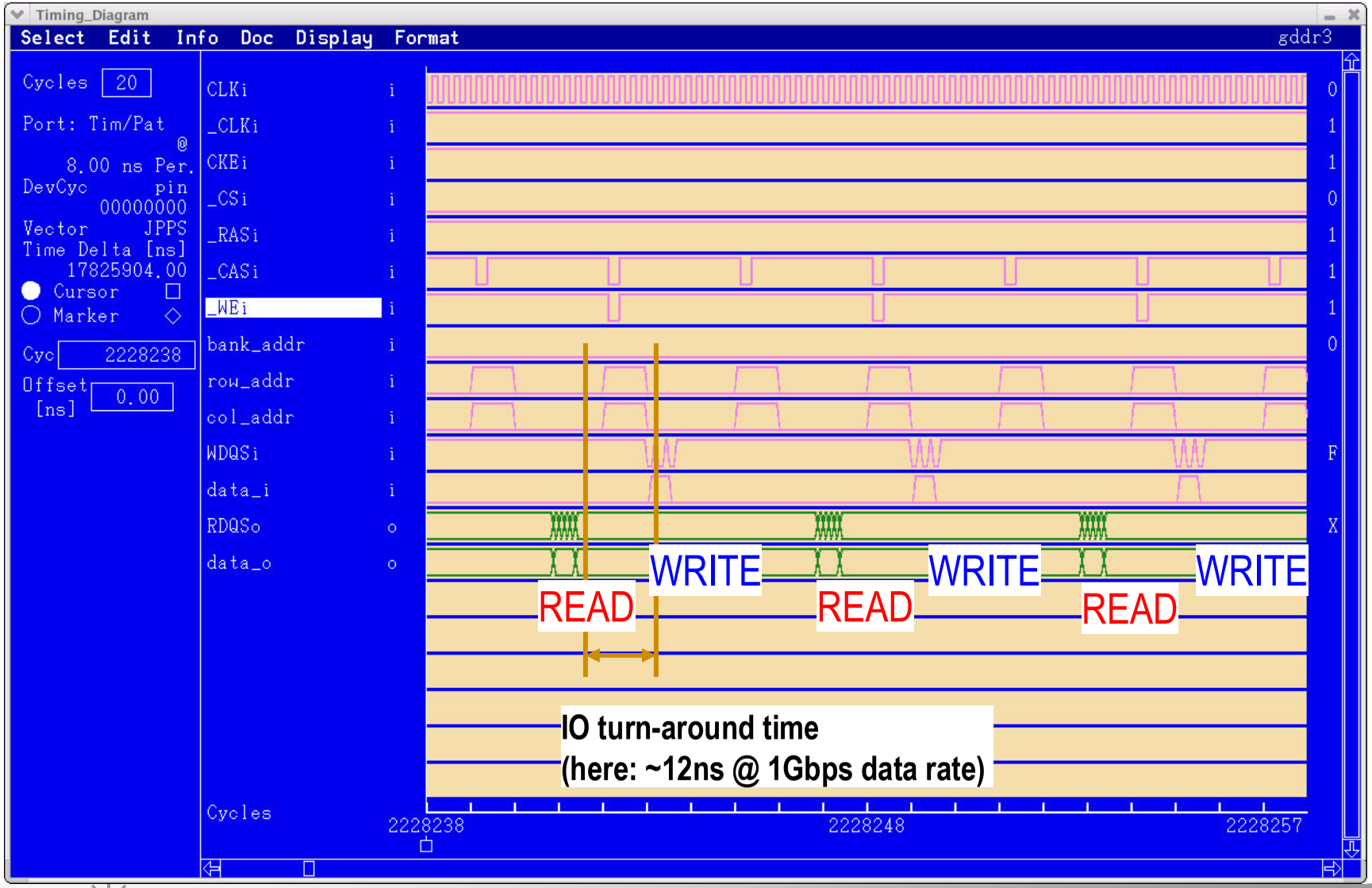
- For a driver sharing application (by-N sharing) the timing reference is the socket of site 1
  - for the shared pins the fixture delay values compensate the delay to site 1 only
    → for site 1 there is no change compared to a non-shared application

Memory Test Challenges

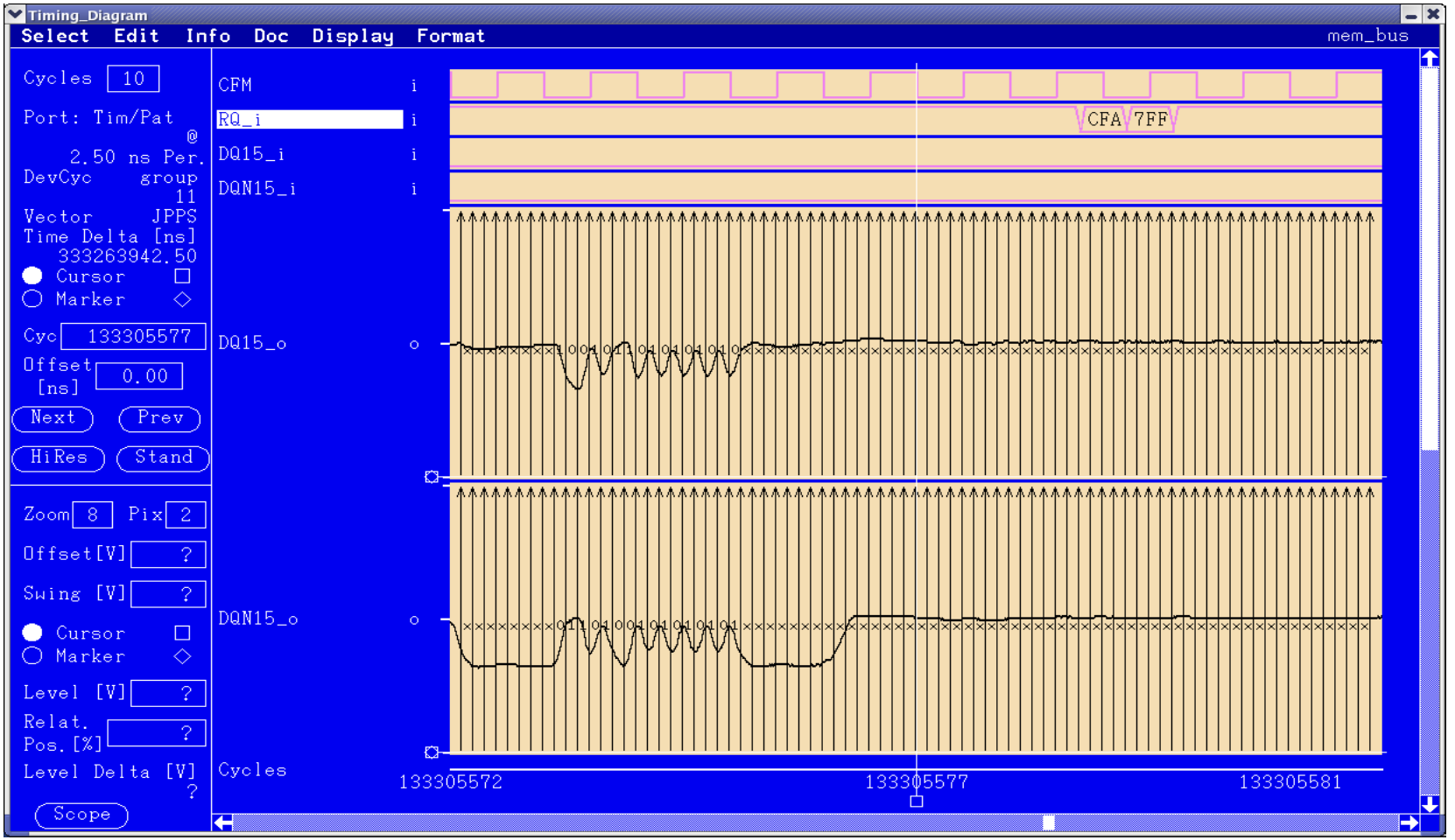
- High Speed
- Mix of parts is increasing
  - Flash, DRAM, SRAM
- Increase Parallelism
- **Debug tools**

- **High throughput**
- **Flexible configuration**
- **Reduced system cost**

Timing Diagram

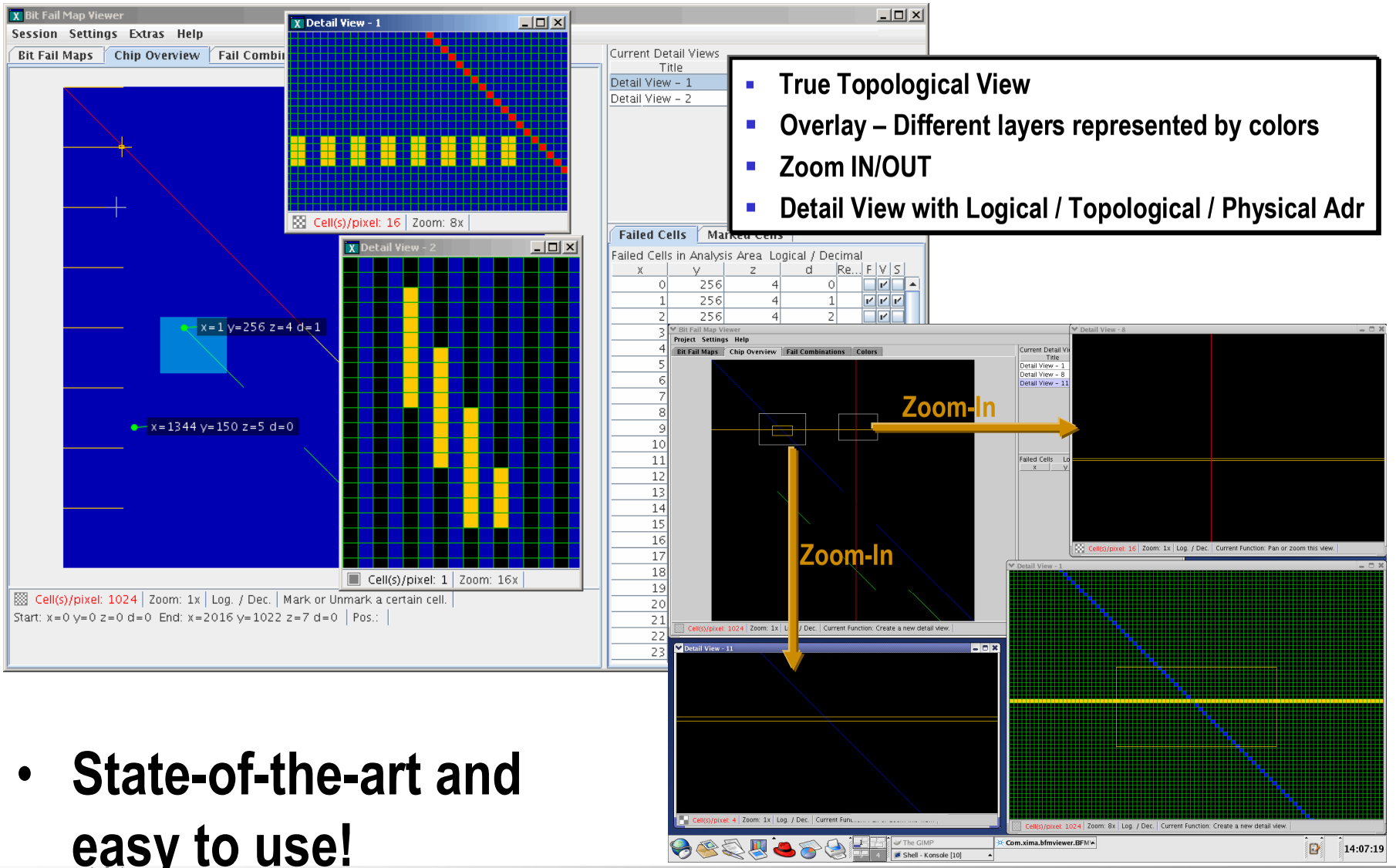


Scope view



‘Oscilloscope’ integrated into test system

BitMap Viewer

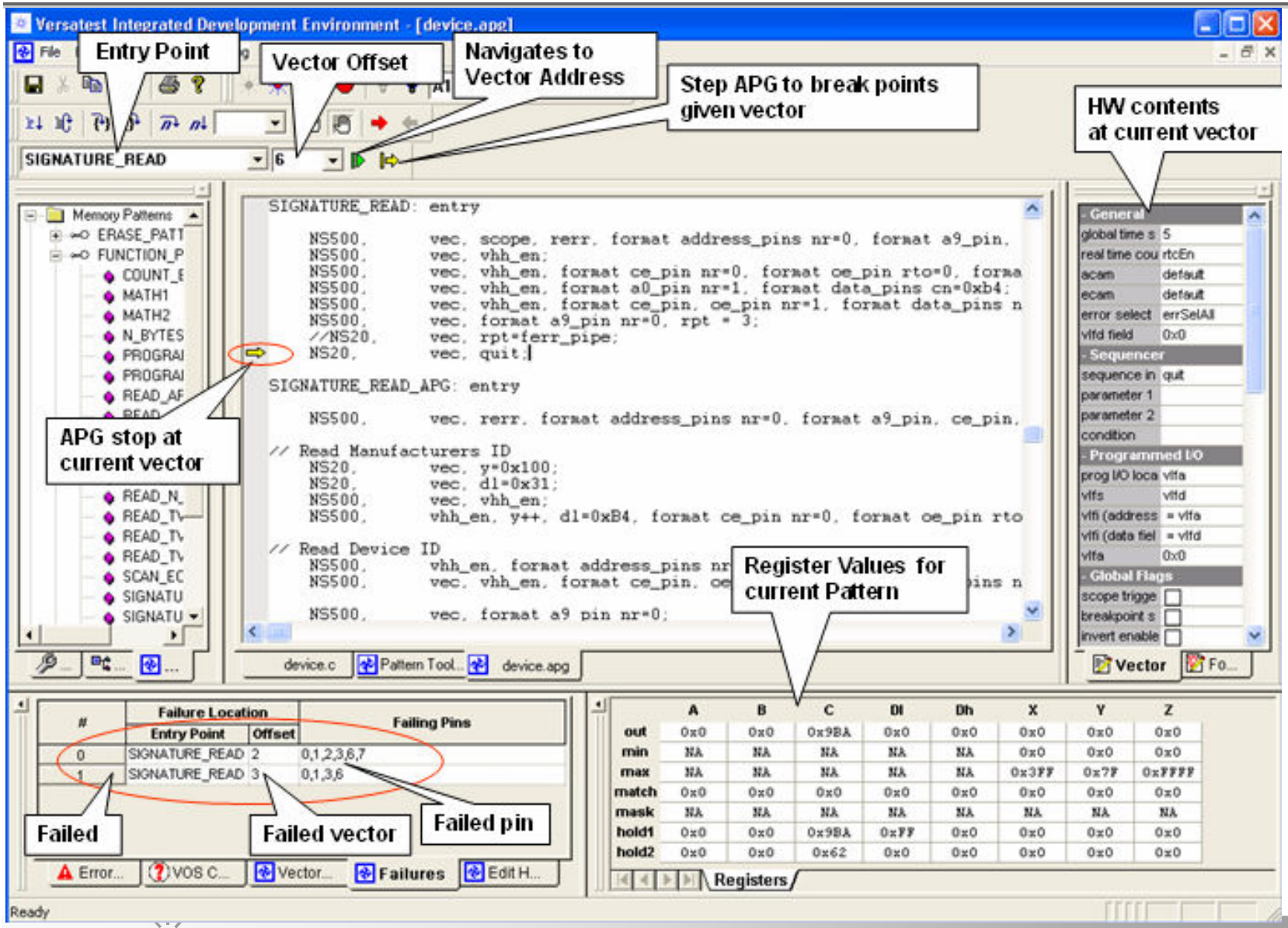


- True Topological View
- Overlay – Different layers represented by colors
- Zoom IN/OUT
- Detail View with Logical / Topological / Physical Adr

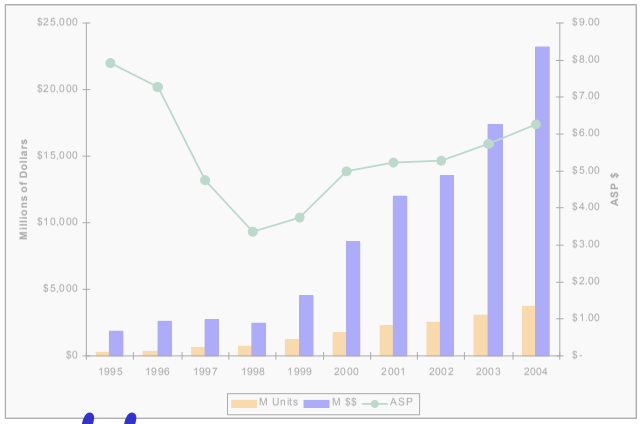
- State-of-the-art and easy to use!

VERIGY

PATTERN Tool



Q & A


$25,000
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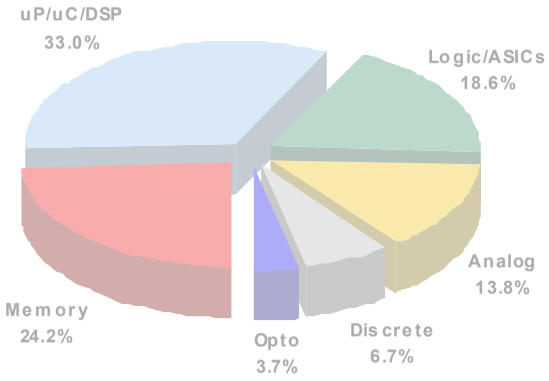
ASP

- *Thank you !!*


uP/uC/DSP
33.0%
Logic/ASICs
18.6%
Analog
13.8%
Discrete
6.7%
Opto
3.7%
Memory
24.2%