EE8086
System-On-Chip Testing

Jin-Fu Li
Advanced Reliable Systems (ARES) Laboratory
Department of Electrical Engineering
National Central University
Jhongli, Taiwan

Syllabus

Contents

- Introduction
- Basics of VLSI Testing
- Digital Test Architecture
- System/Network-on-Chip Test Architectures
- Semiconductor Memory Testing
- Low-Power Testing
- System-in-Package Test Architectures
- Coping with Physical Failures, Soft Errors, and Reliability Issues

Syllabus

- Text Books
  - 1. L.-T. Wang, C. E. Stroud, and N. A. Tuba,"System on Chip Test Architectures", Elsevier, 2008.
  - 2. Handouts
- Reference Book
  - L.-T. Wang, C.-W. Wu, and X. Wen,"VLSI Test Principles and Architectures", Elsevier, 2006.
- Grading
  - Homework (30%); Midterm (40%); Project (30%)
- Prerequisite
  - Introduction to VLSI
- **Key dates**
  - **Midterm : 10:00-12:00, Mon. May 4, E1-105**
  - **Project Presentation: 6/15, 6/16, 6/21**
  - **Project Report: By 17:00, June 26.**

Lecture Schedule

Date	Note
Week 1 (2/23, 24)	
Week 2 (3/2, 3/3)	
Week 3 (3/9, 3/10)	
Week 4 (3/16, 3/18)	
Week 5 (3/23, 3/24)	
Week 6 (3/30, 3/31)	
Week 7 (4/6, 4/7)	
Week 8 (4/13, 4/14)	
Week 9 (4/20, 4/21)	
Week 10 (4/27, 4/28)	Project Proposal
Week 11 (5/4, 5/5)	Midterm
Week 12 (5/11, 5/12)	
Week 13 (5/18, 5/19)	
Week 14 (5/25, 5/26)	
Week 15 (6/1, 6/2)	
Week 16 (6/8, 6/9)	
Week 17/18 (6/15, 6/16, 6/21)	Project Presentation; Project Report is due by 17:00 6/26