Chapter 1 Introduction

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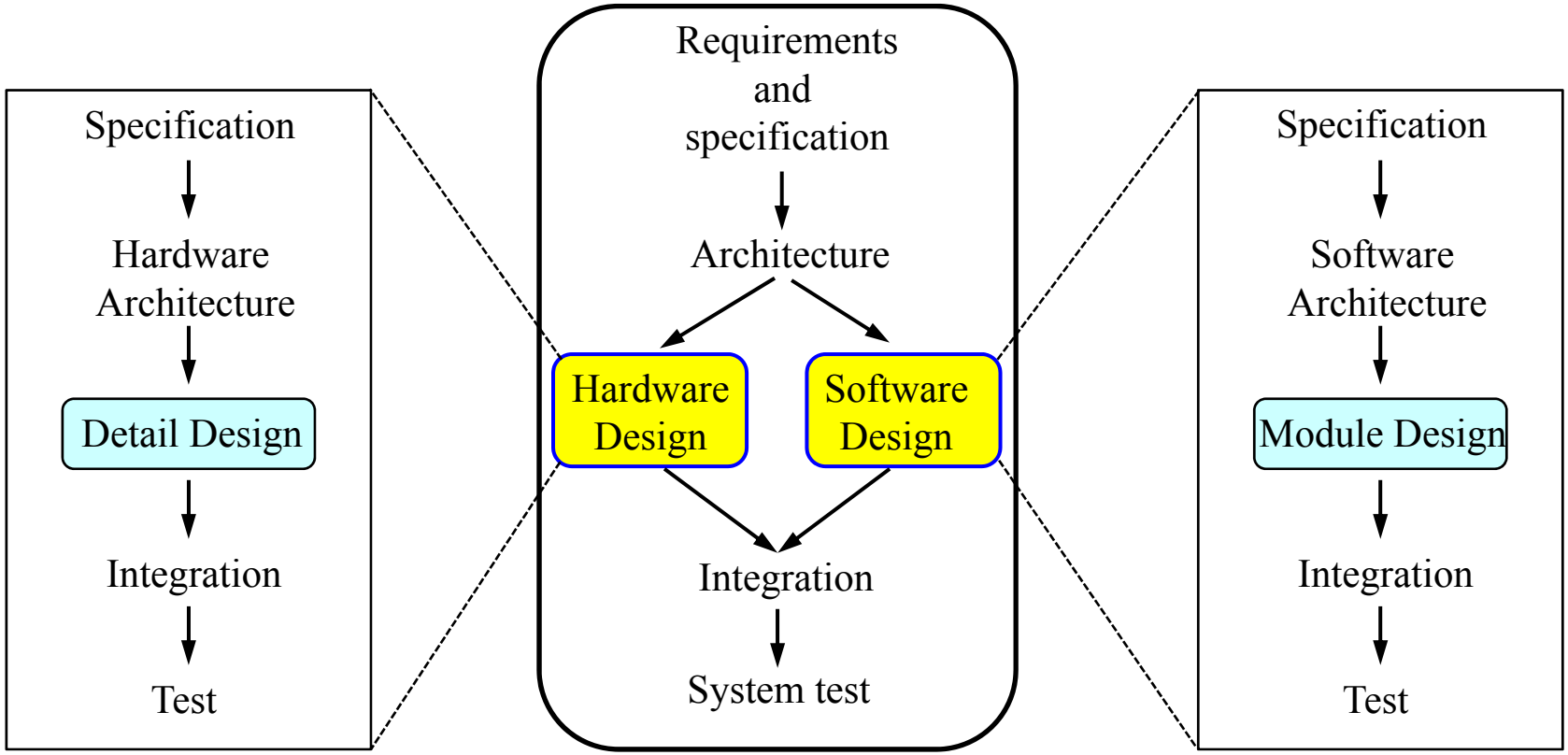
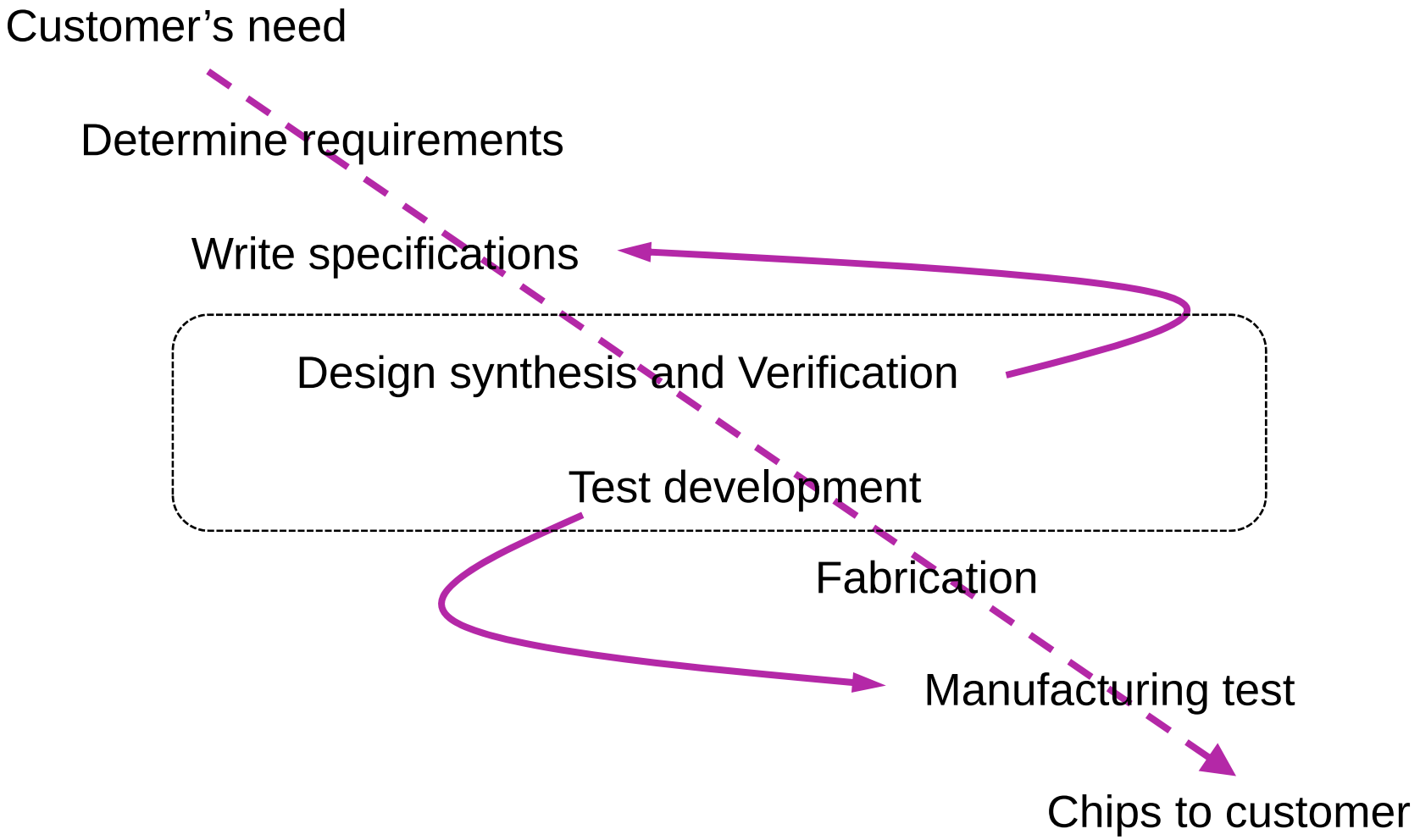
Outline

- VLSI Realization
- Role of Testing
- Trends of Architecture of VLSI Chips

Hierarchical Design Flow for an System Chip



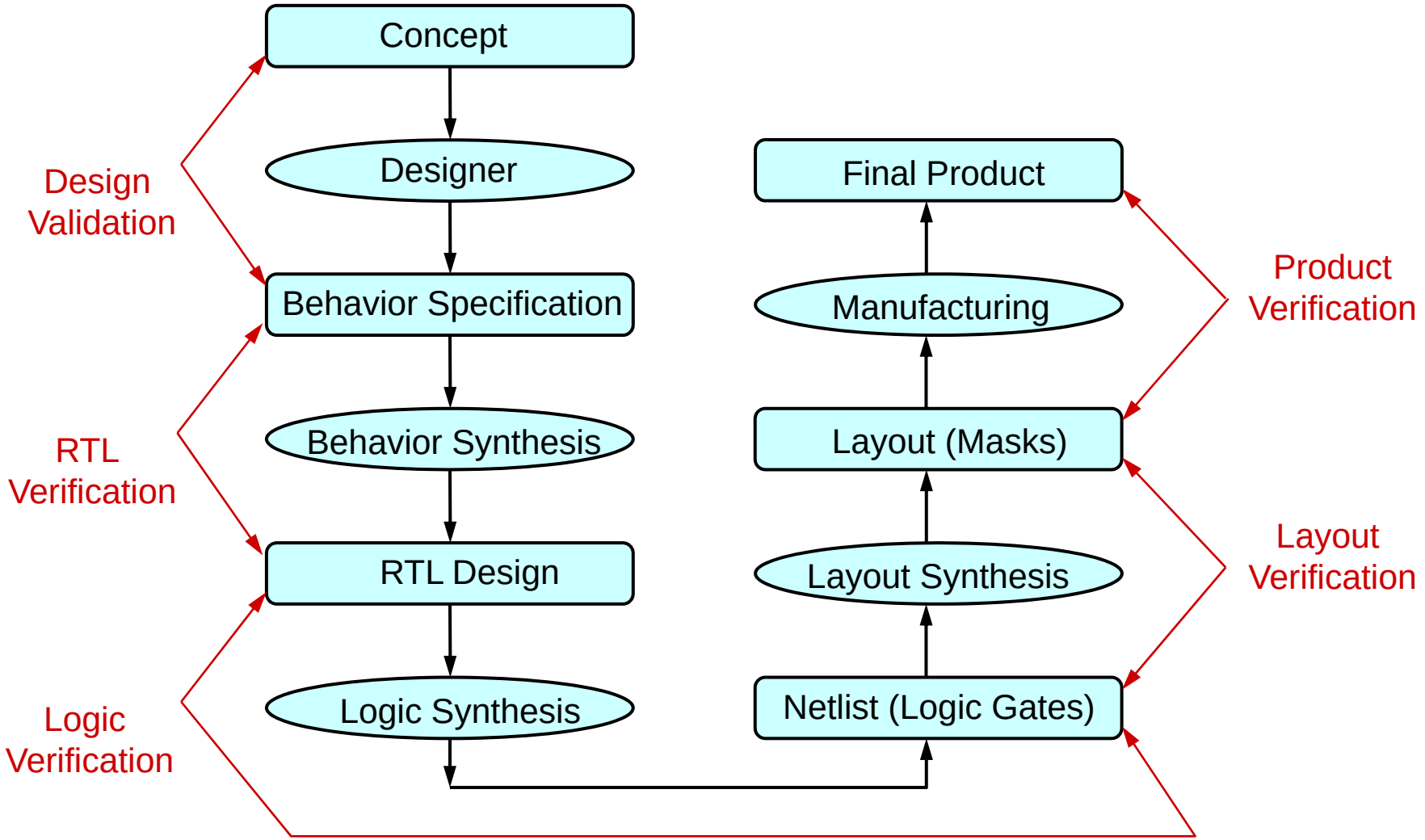
VLSI Realization Process



Definitions

- Design synthesis
  - Given an I/O function, develop a procedure to manufacture a device using known materials and processes
- Verification
  - Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function
- Test
  - A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect

VLSI Design Cycle



Verification

- The four representations of the design
  - Behavioral, RTL, gate level, and layout
- In mapping the design from one phase to another, it is likely that some errors are produced
  - Caused by the CAD tools or human mishandling of the tools
- Usually, *simulation* is used for verification, although more recently, *formal verification* has been gaining in importance
- Two types of simulations are used to verify the design
  - *Functional simulation* & *timing simulation*

Role of Testing

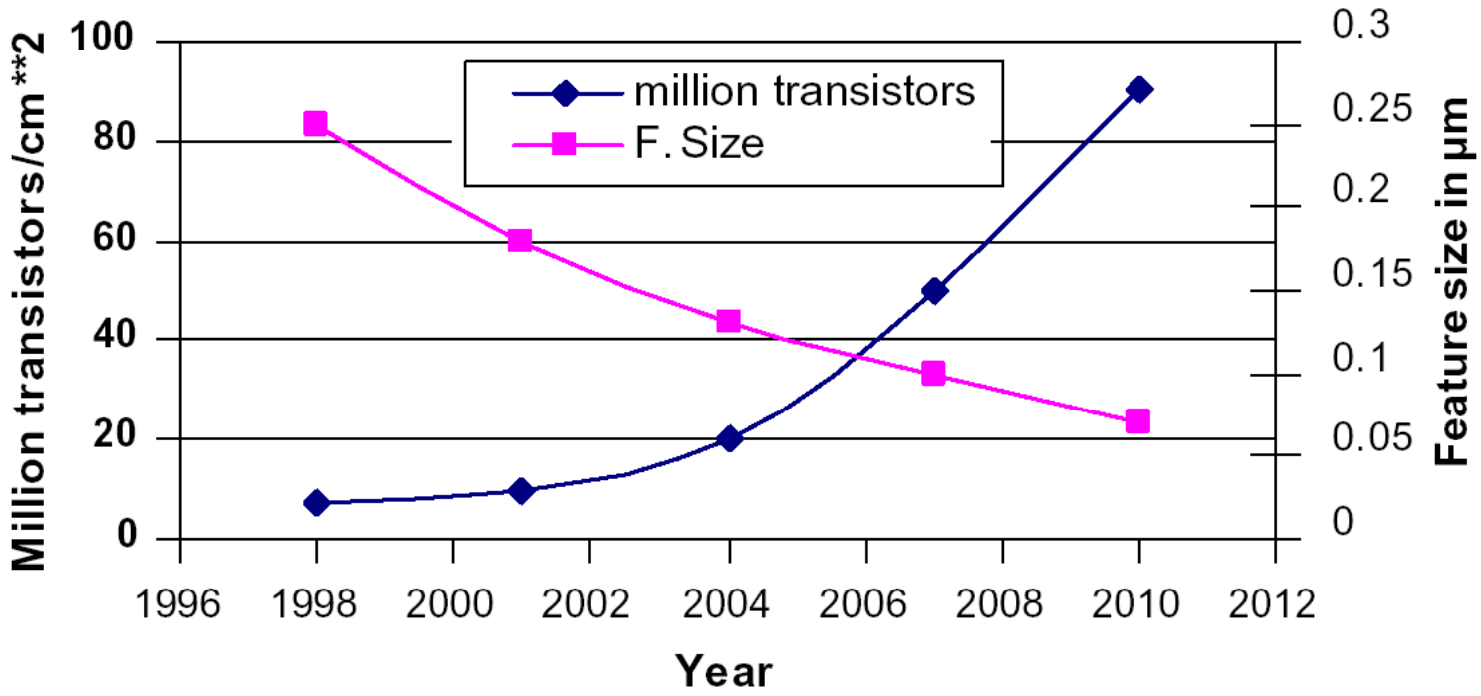
- If you design a product, fabricate, and test it, and it fails the test, then there must be a cause for the failure
  - Test was wrong
  - The fabrication process was faulty
  - The design was incorrect
  - The specification problem
- The role of *testing* is to detect whether something went wrong and the role of *diagnosis* is to determine exactly what went wrong
- Correctness and effectiveness of testing is most important for quality products

Benefits of Testing

- *Quality* and *economy* are two major benefits of testing
- The two attributes are greatly dependent and can not be defined without the other
- Quality means satisfying the user's needs at a minimum cost
- The purpose of testing is to weed out all bad products before they reach the user
  - The number of bad products heavily affect the price of good products
- A profound understanding of the principles of manufacturing and test is essential for an engineer to design a quality product

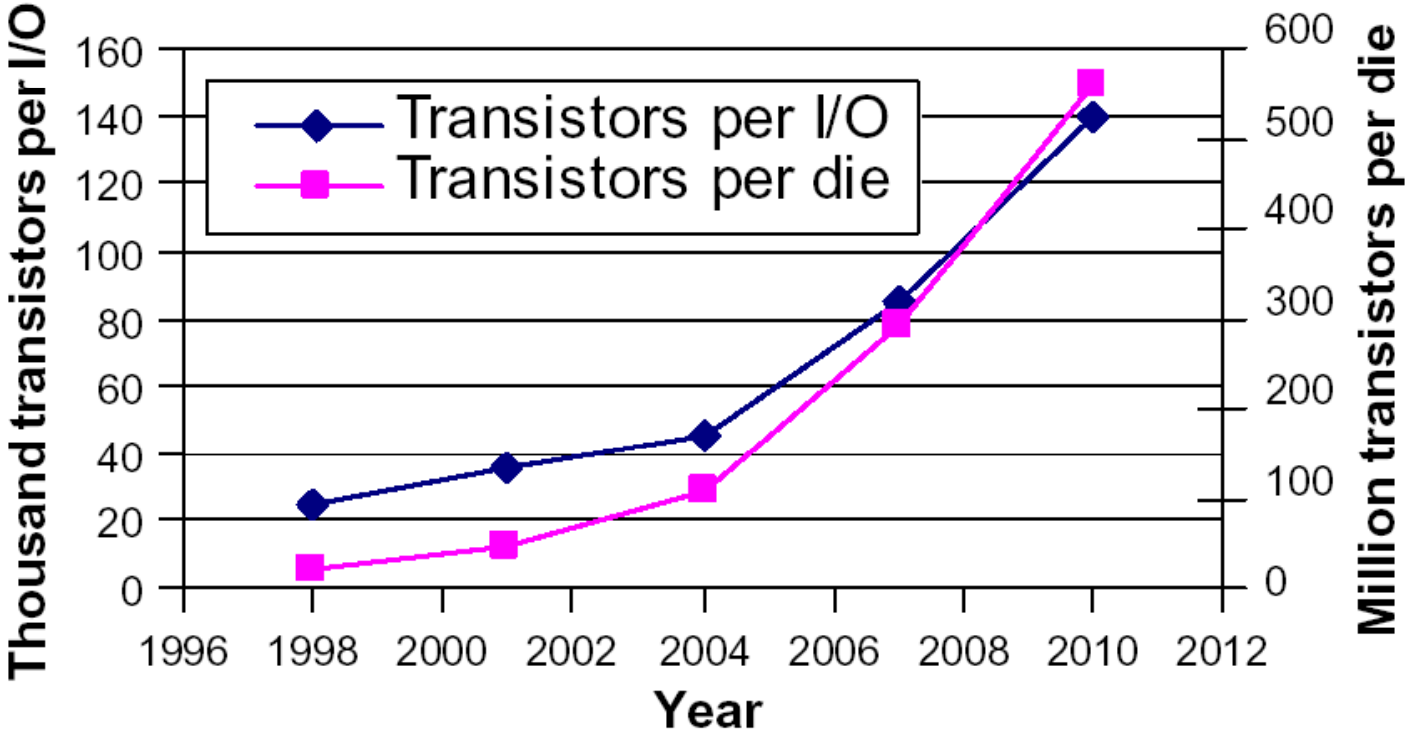
Present and Future

- Semiconductor Industry Association's (SIA's) projection



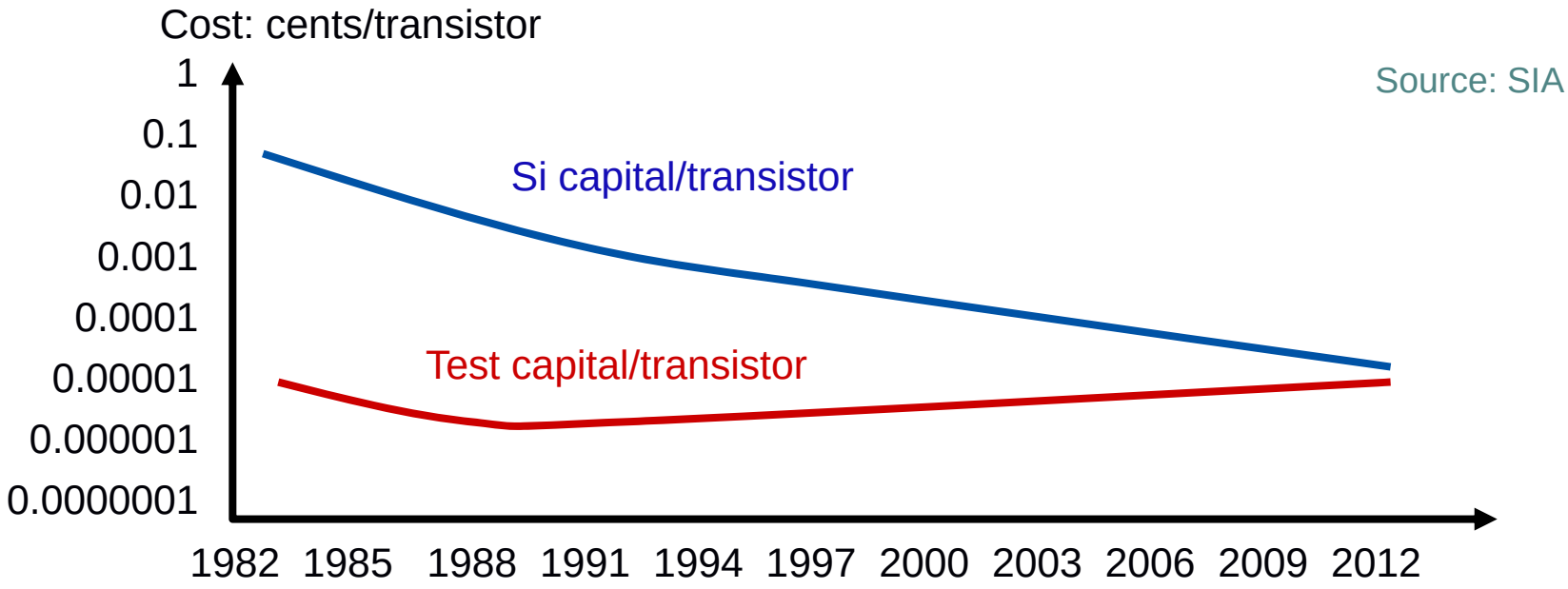
Present and Future

- Semiconductor Industry Association's (SIA's) projection



Trends of Testing

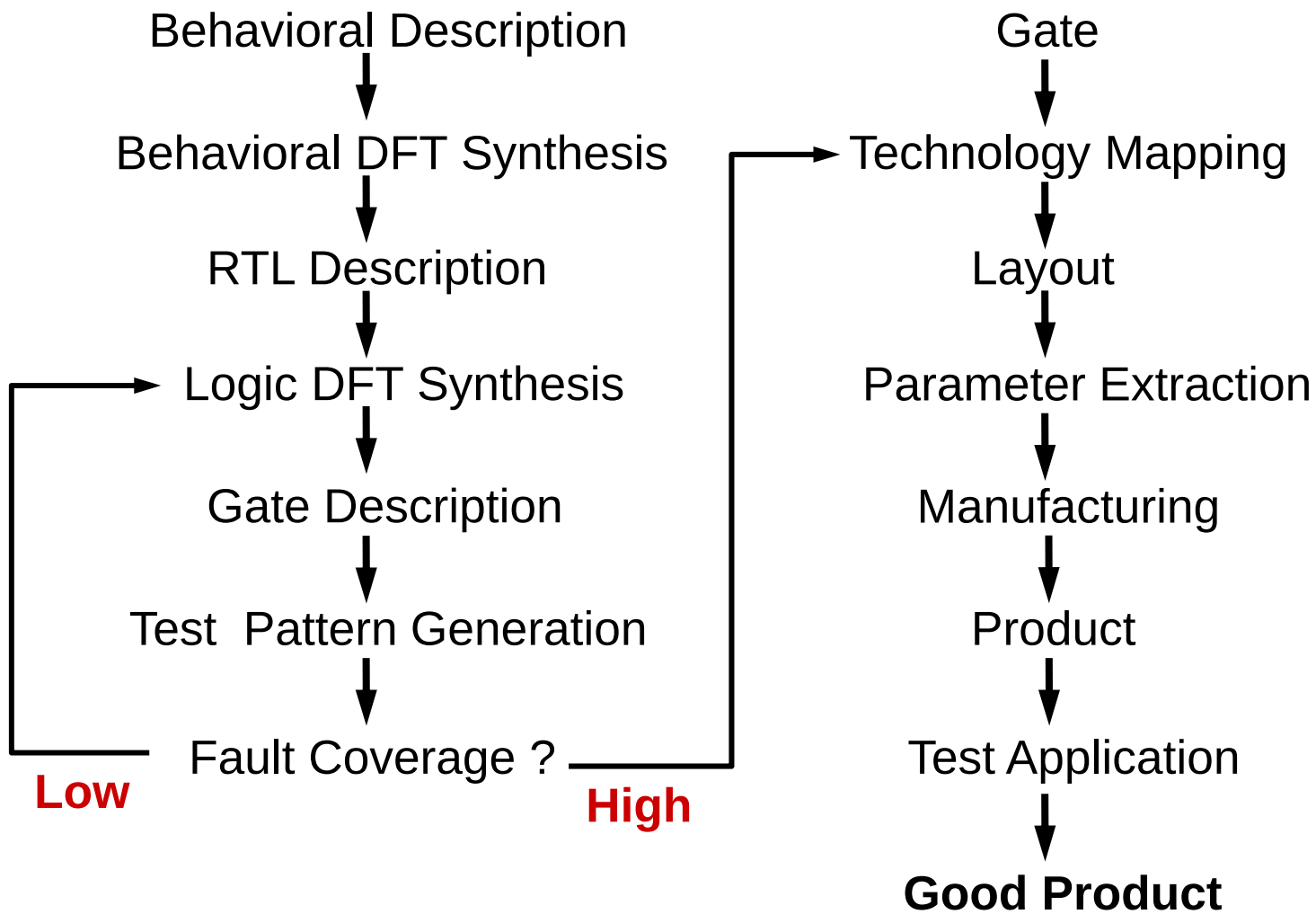
- Two key factors are changing the way of VLSI ICs testing
  - The manufacturing test cost has been not scaling
  - The effort to generate tests has been growing geometrically along with product complexity



Test Knowledge is Important

- *Testing* is becoming a factor in design optimization
- Designers customarily strive for an optimal design
  - *A high-speed, low-power design occupying the smallest possible area*
- Conventionally, the designer often optimize one of the tree attributes: *speed* (or delay), *area*, and *power*
- At present, a fourth attribute is considered
  - *Testability*
- Nowadays, the *testability cycle* should *parallel* the *design cycle*

DFT Cycle


Behavioral Description
Behavioral DFT Synthesis
RTL Description
Logic DFT Synthesis
Gate Description
Test Pattern Generation
Fault Coverage ?
Low
High
Gate
Technology Mapping
Layout
Parameter Extraction
Manufacturing
Product
Test Application
Good Product

As Technology Scales Continuously

- Die size, chip yield, and design productivity have so far limited transistor integration in a VLSI design
- Now the focus has shifted to energy consumption, power dissipation, and power delivery
- As technology scales further we will face new challenges, such as variability, single-event upsets (soft errors), and device (transistor performance) degradation– these effects manifesting as inherent ***unreliability*** of the components, posing design and test challenges

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Possible Solution to Conquer Unreliability

- *The key to the reliability problem might be to exploit the abundance of transistors—use Moore's low to advantage. Instead of relying on higher and higher frequency of operation to deliver higher performance, a shift toward **parallelism** to deliver higher performance is in order, and thus **multi** might be the solution at all levels—from multiplicity of functional blocks to multiple processor cores in a system*

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

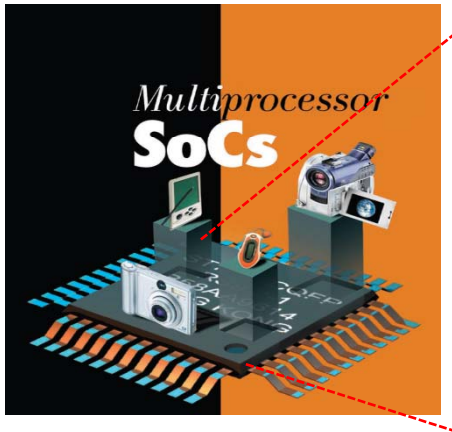
Possible Solution to Conquer Unreliability

- *We could distribute test functionality as a part of the hardware to dynamically detect errors, or to correct and isolate aging and faulty hardware. Or a subset of cores in the multicore design could perform this work. This microarchitecture strategy, with multicores to assist in redundancy, is called* ***resilient microarchitecture****. It continuously detects errors, isolates faults, confines faults, reconfigures the hardware, and thus adapts. If we can make such a strategy work, there is no need for on-time factory testing, burn in, since the system is capable of testing and reconfiguring itself to make itself work reliably throughout its lifetime.*

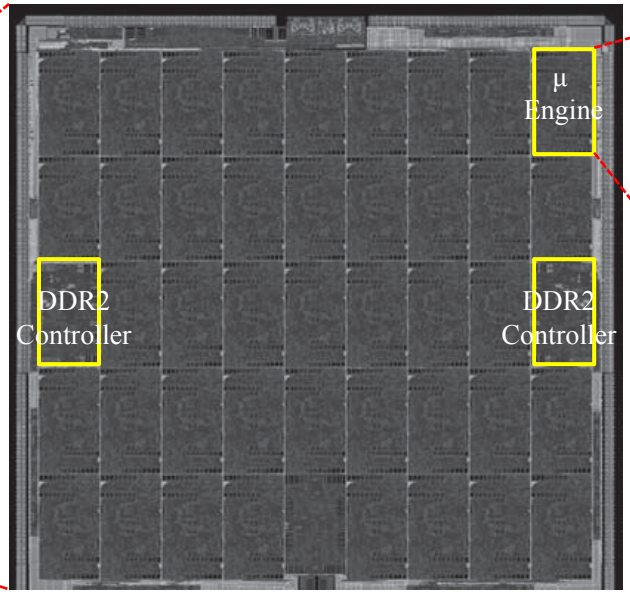
Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

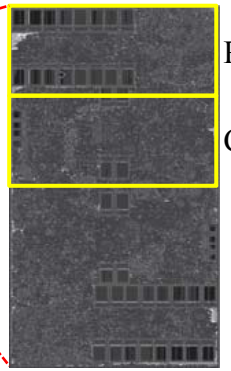
Architecture of Current SOC Chips

- Multi-core chip architecture
  - Use multiple identical cores to design a chip
- Network-on-chip communication infrastructure
  - Multiple point-to-point data links interconnected by switches (i.e., routers)



Source: IEEE Computer, 2005.

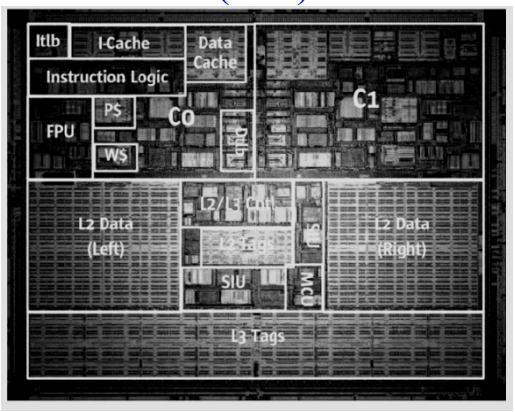




Source: IEEE Micro, 2007.

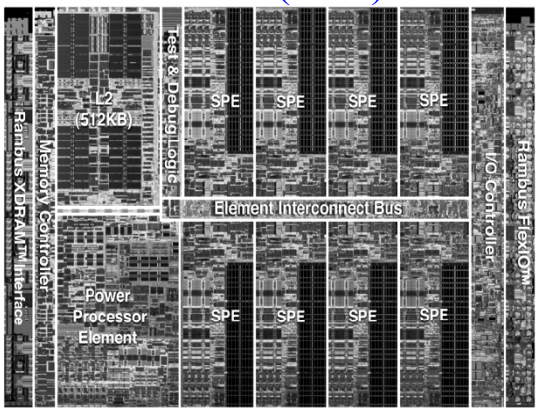
Examples

SPARC V9 (Sun)



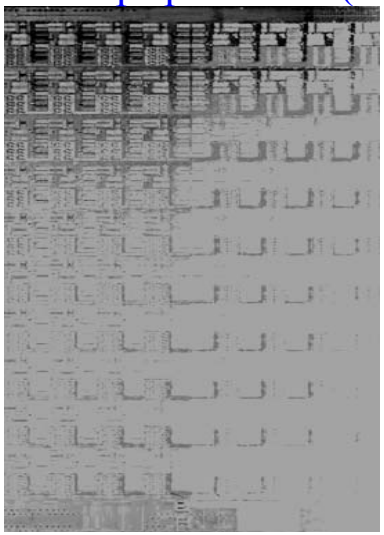
Source: IEEE JSSC, 2006.

Cell Processor (IBM)



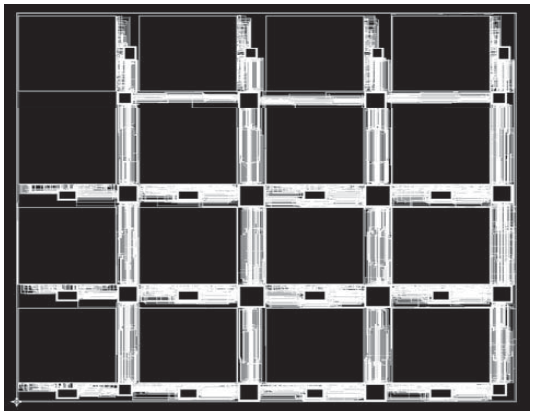
Source: IEEE JSSC, 2006.

Teraflops processor (Intel)



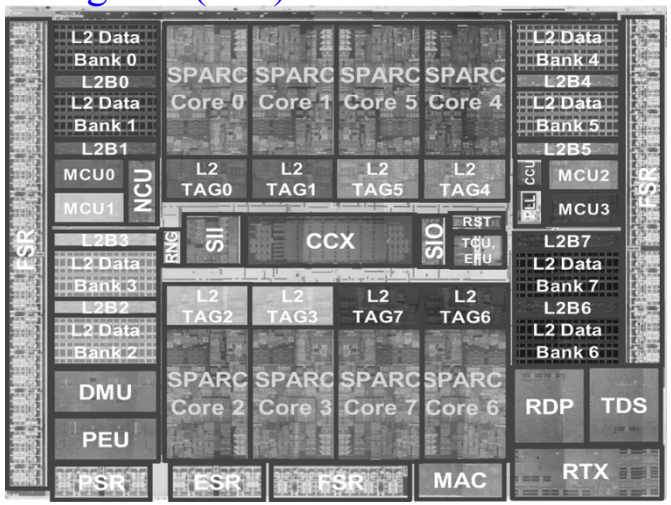
Source: IEEE Micro, 2007.

4x4 mesh built with Xpipes library components



Source: IEEE Micro, 2007.

Niagara2 (Sun)

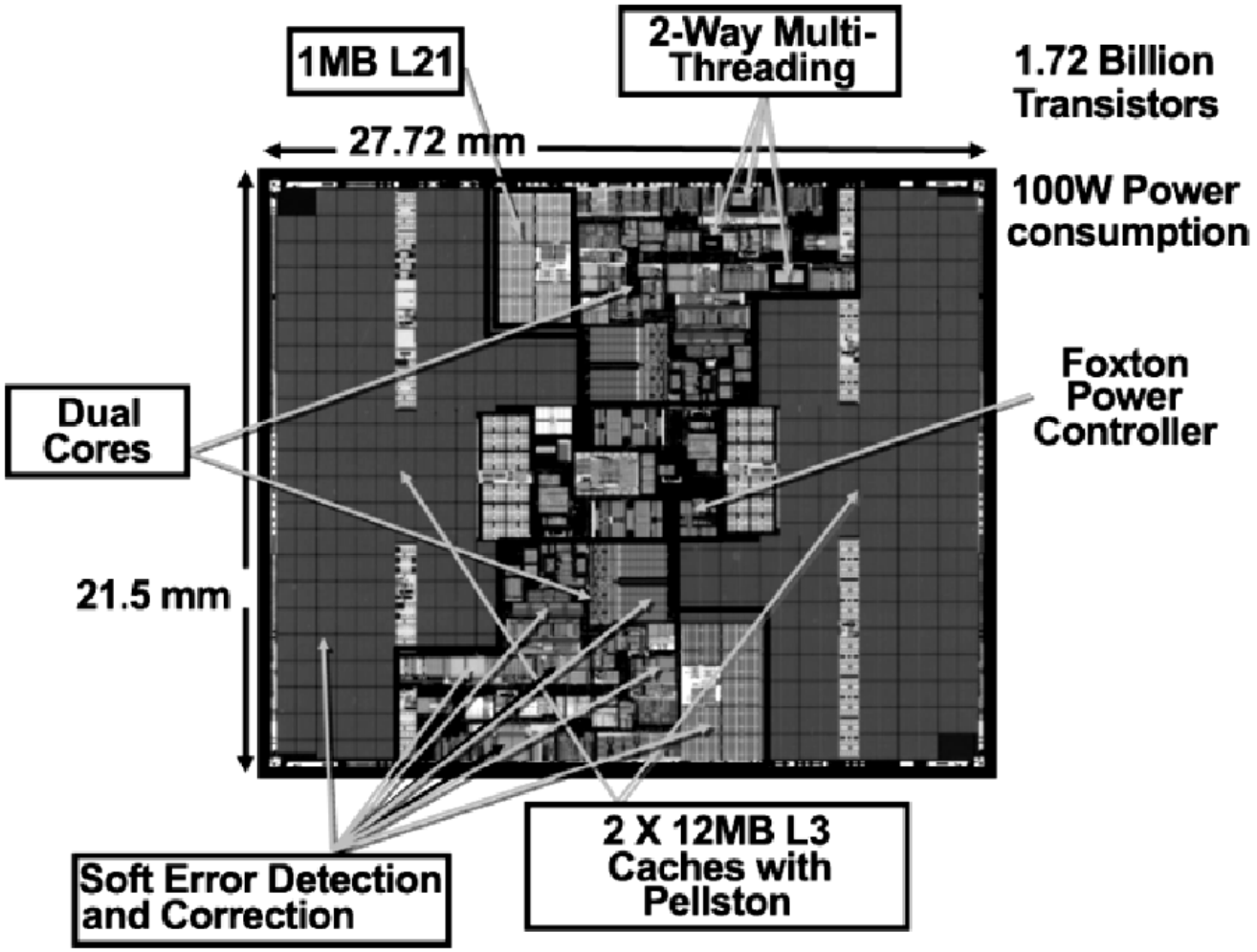


Source: IEEE JSSC, 2008.

Importance of Testing Techniques

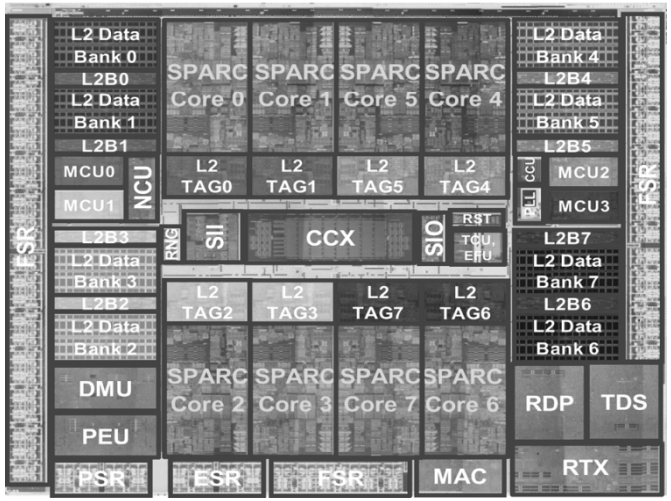
- Testing technique play an important role in current multicore chips
  - Quality insurance
  - Yield-improvement
  - Reliability-improvement
  - Monitoring
  - Diagnosis
  - …

Example: Itanium (JSSC, Jan. 2006)



Example: Niagara2 & POWER6 (JSSC, 2008)

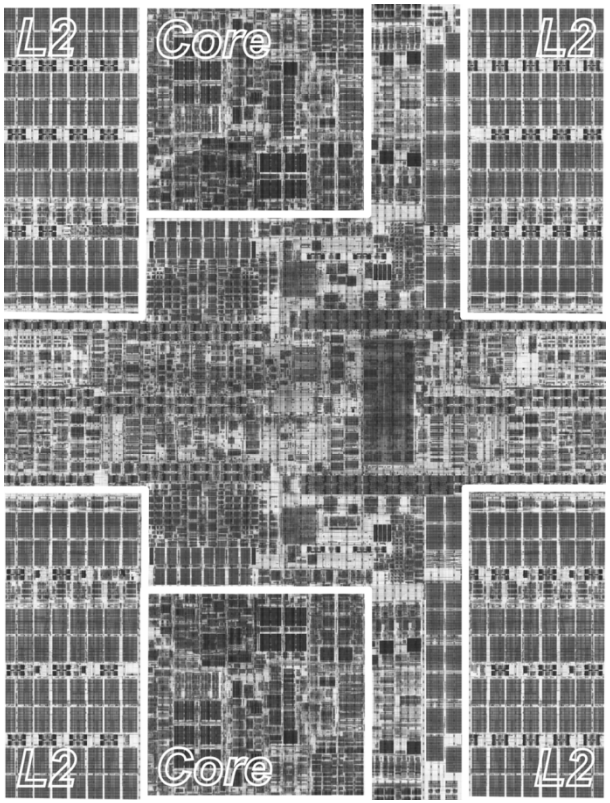
Niagara2 (Sun)



Design-for-Testability Features:

1. 32 Scans + ATPG
2. BIST for arrays
3. ….

POWER6 (IBM)

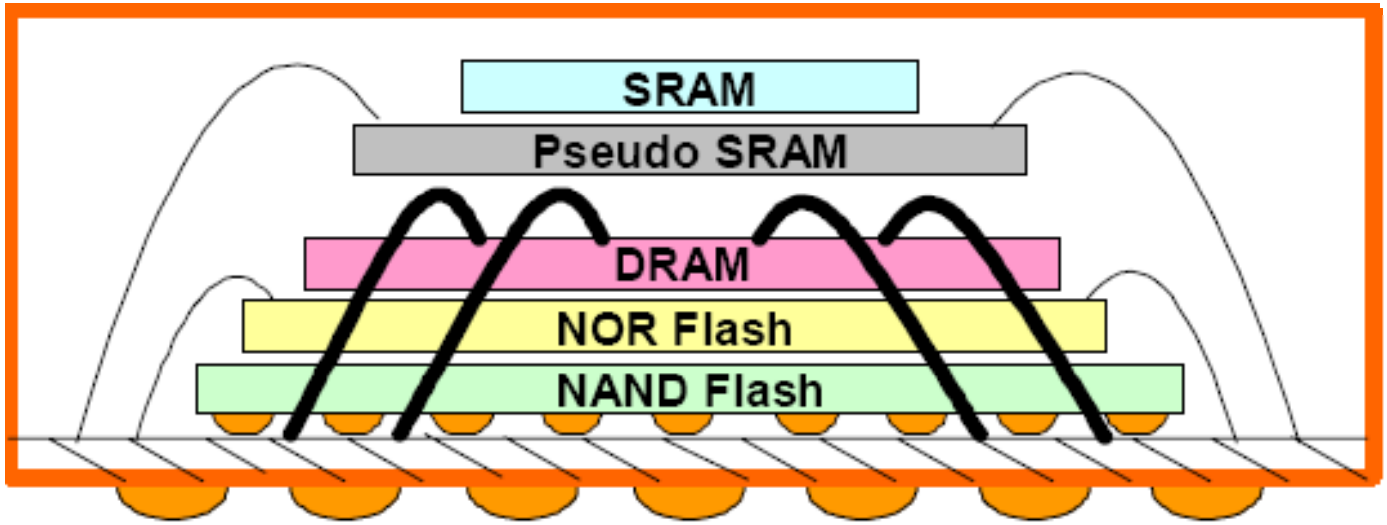


Design-for-Testability Features:

1. Logic BIST
2. BIST for arrays
3. BISR for arrays
4. …

3D-SiP: Next Technology / Architecture Transition?

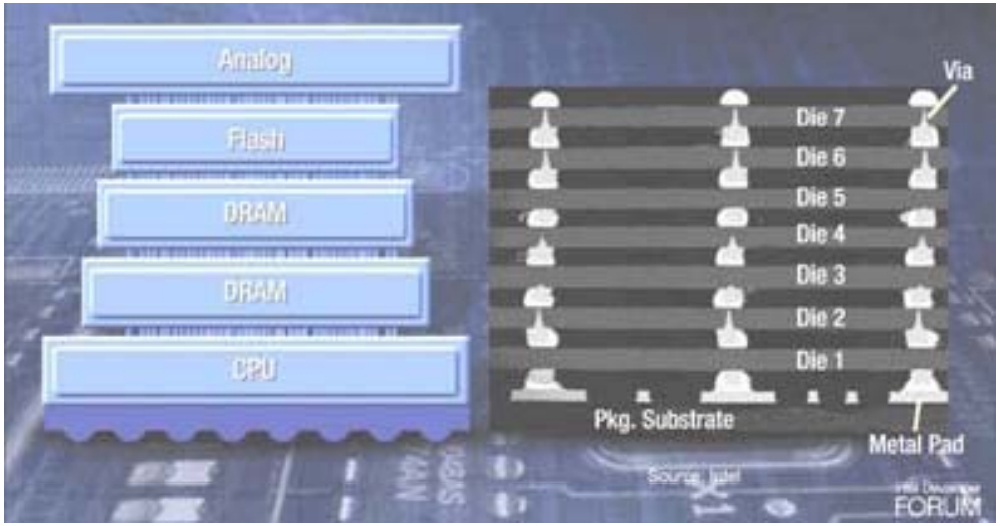
- Technology evolution
  - Bipolar → CMOS → Multicore → 3D integration + System-in-package (3D-SiP)
- System-in-package
  - stacking dies using bonding wires



Source: ISQED, 2008.

3D-SiP: Next Technology / Architecture Transition?

- 3D integration
  - Stacking dies using through silicon via (TSV)



Source: IBM, 2008.

Challenges of 3D Implementations

- Yield
  - Design for resiliency
- Thermal
  - Can we overcome it?
- Test
- Reliability
- …

Source: IBM, 2008.