Chapter 4 Digital Test Architectures

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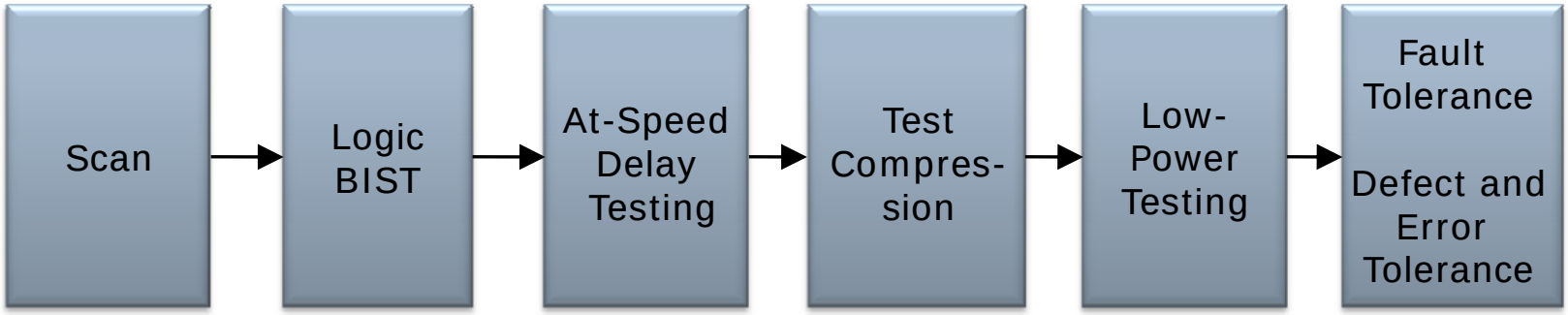
Outline

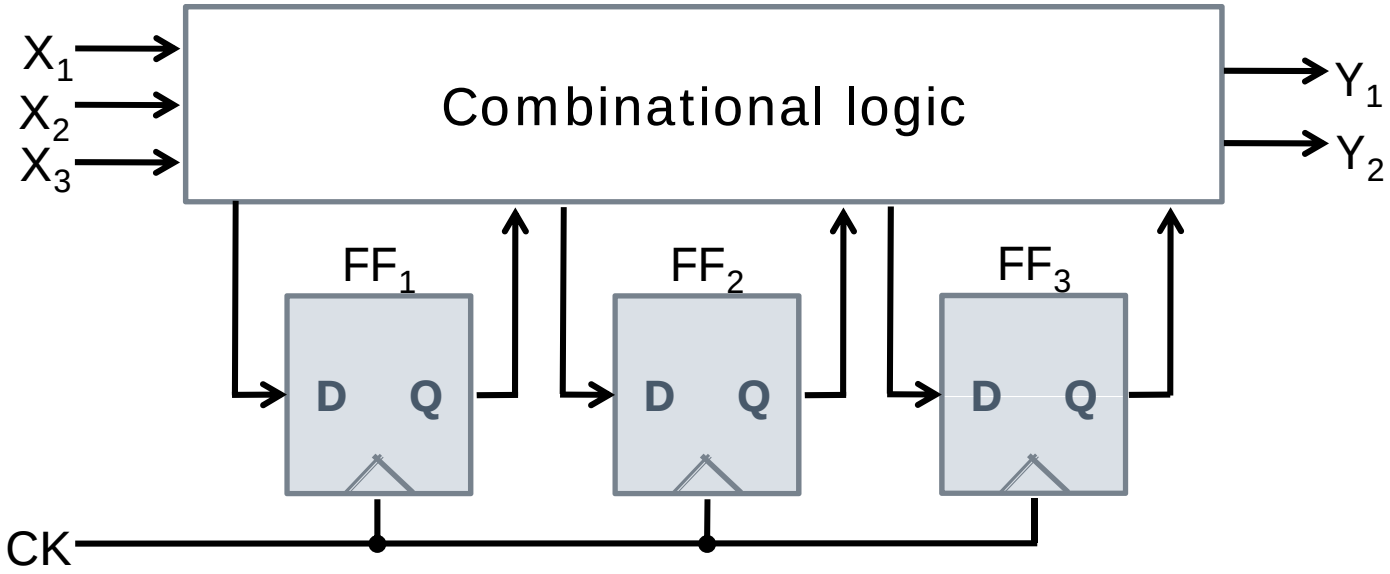
- Scan test
- Logic BIST
- Test Compression

Evolution of DFT Techniques



Scan Testing

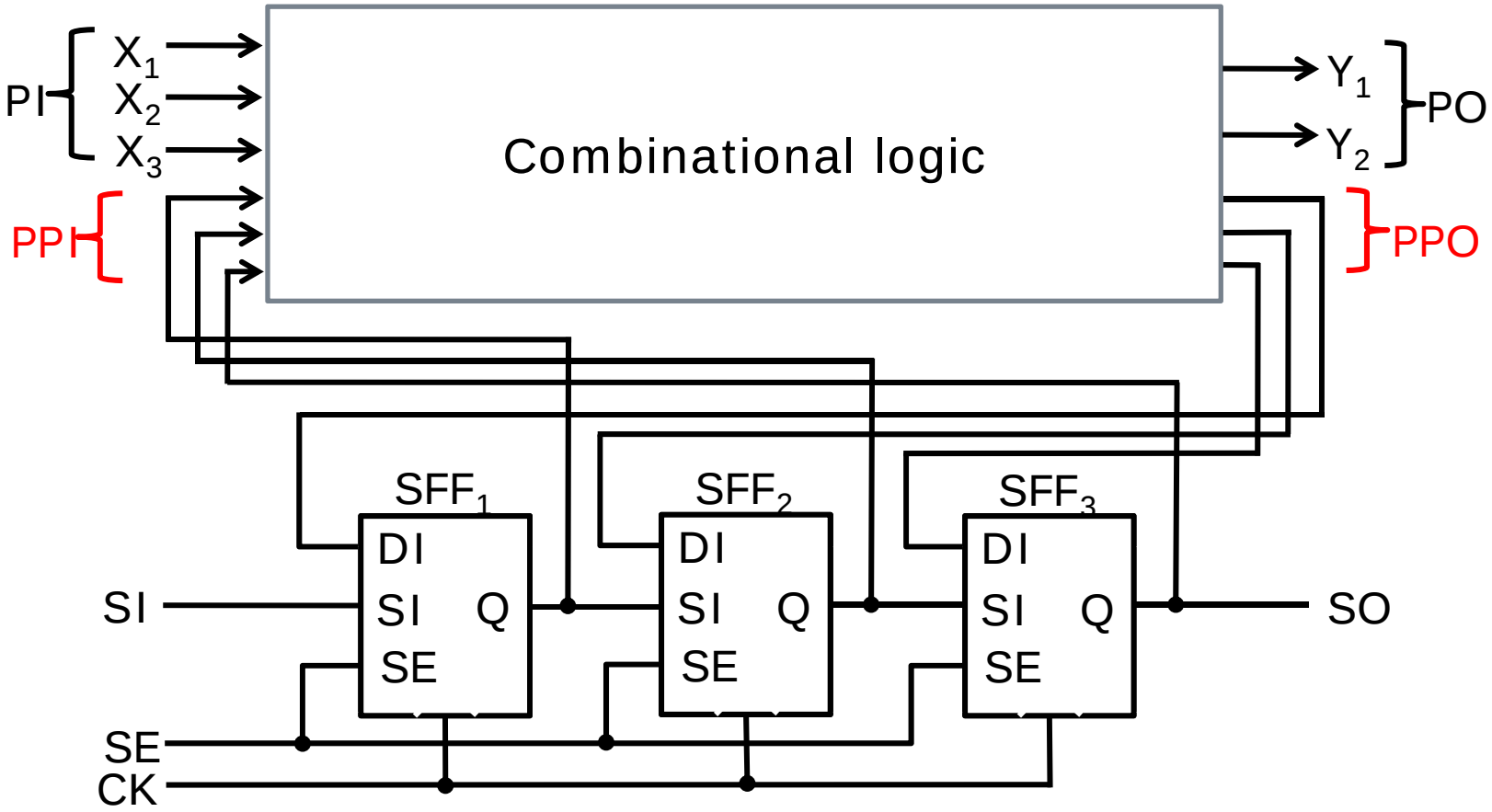
- Principle of scan testing
  - In test mode, the scan chain can change a sequential circuit into a combinational circuit. Therefore, the test complexity can be reduced
- An example of sequential circuit



Scan Chain Architectures

- Muxed-D scan design
  - Convert storage elements in a circuit into muxed-D scan cells
- Clocked-scan design
  - Convert storage elements in a circuit into clocked scan cells
- Level-sensitive scan design (LSSD)
  - Convert storage elements in a circuit into LSSD shift register latches
- Enhanced scan design
  - Convert storage elements in a circuit into enhanced scan cells each consists of D latch and a muxed-D scan cell
- Low-power scan design
  - Reduce the dynamic power of the circuit under test in test mode

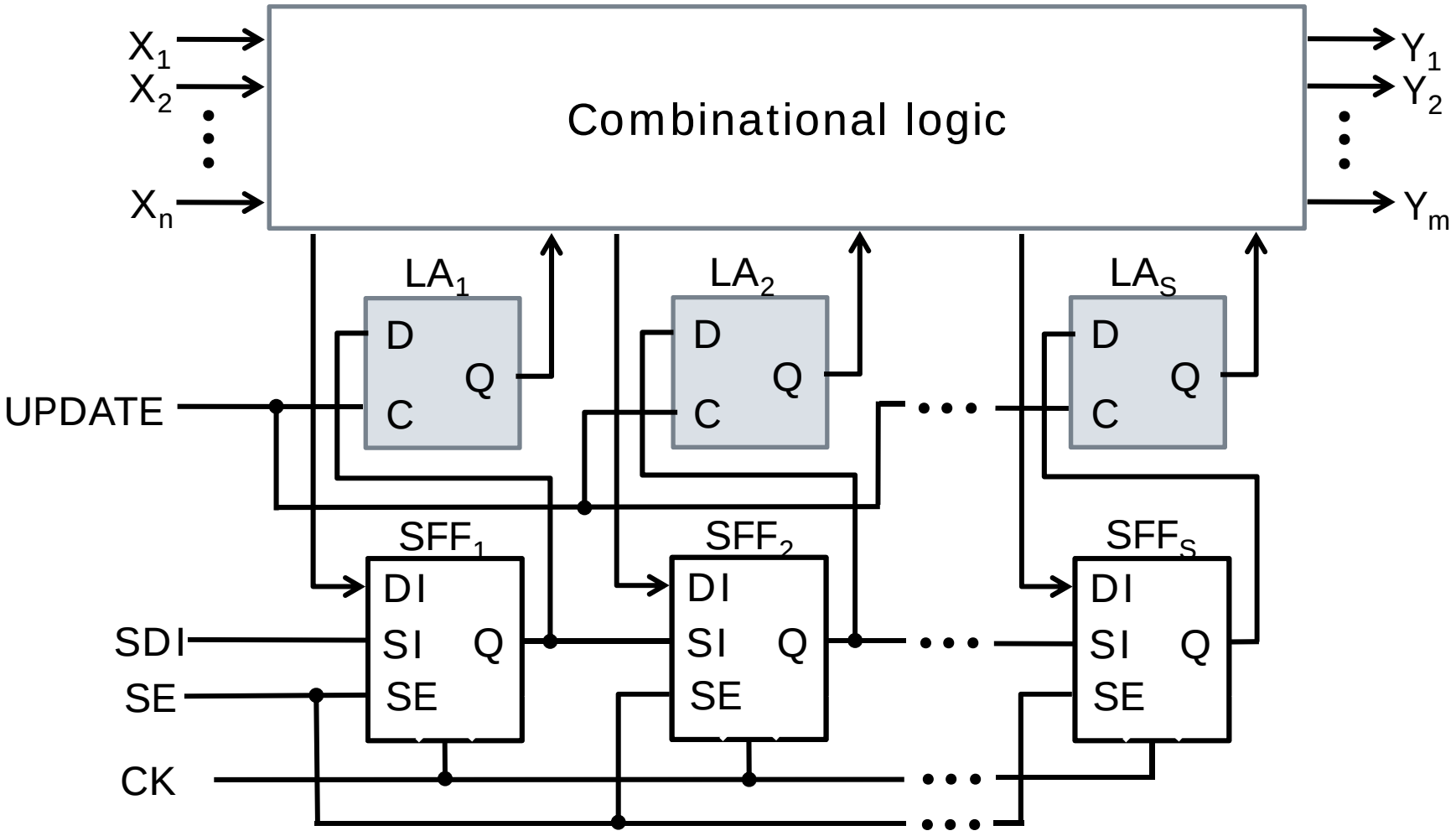
Muxed-D Scan Design



Enhanced Scan Design

- Application
  - Testing delay faults
- Testing for a delay fault requires applying a pair of test vectors in an at-speed fashion
- An enhanced scan design
  - Use an additional D latch and a muxed-D scan cell to store two bits of data that can be applied consecutively to the combinational logic driven by the scan cells

Enhanced Scan Design

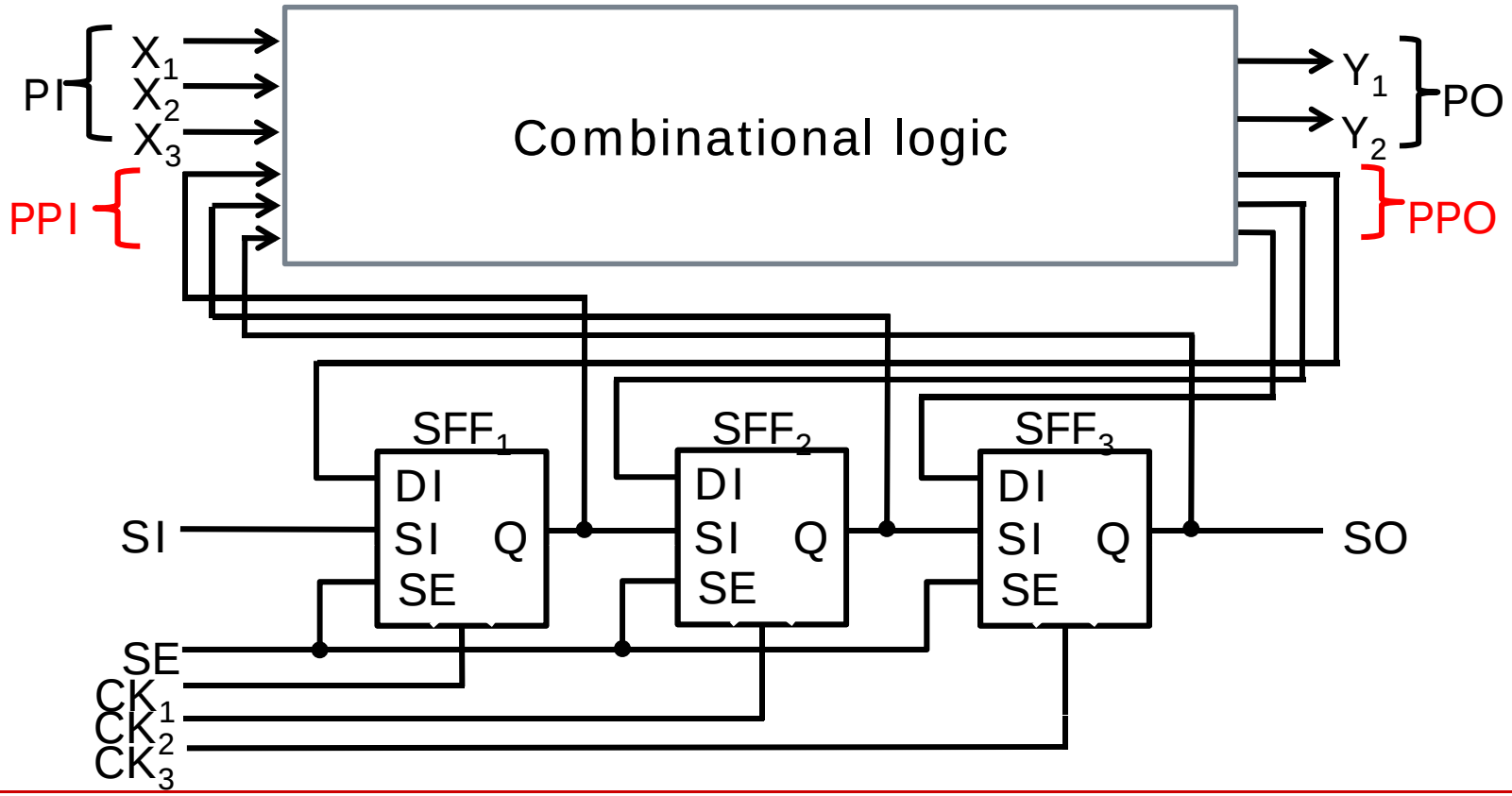


Enhanced Scan Design

- Advantage
  - Achieve high delay fault coverage by applying any arbitrary pair of test vectors
- Disadvantages
  - An additional scan-hold D latch is required
  - Maintaining the timing relationship between UPDATE and CK for at-speed testing may be difficult
  - Many false paths, instead of functional data paths, may be activated during test, causing an over-test problem

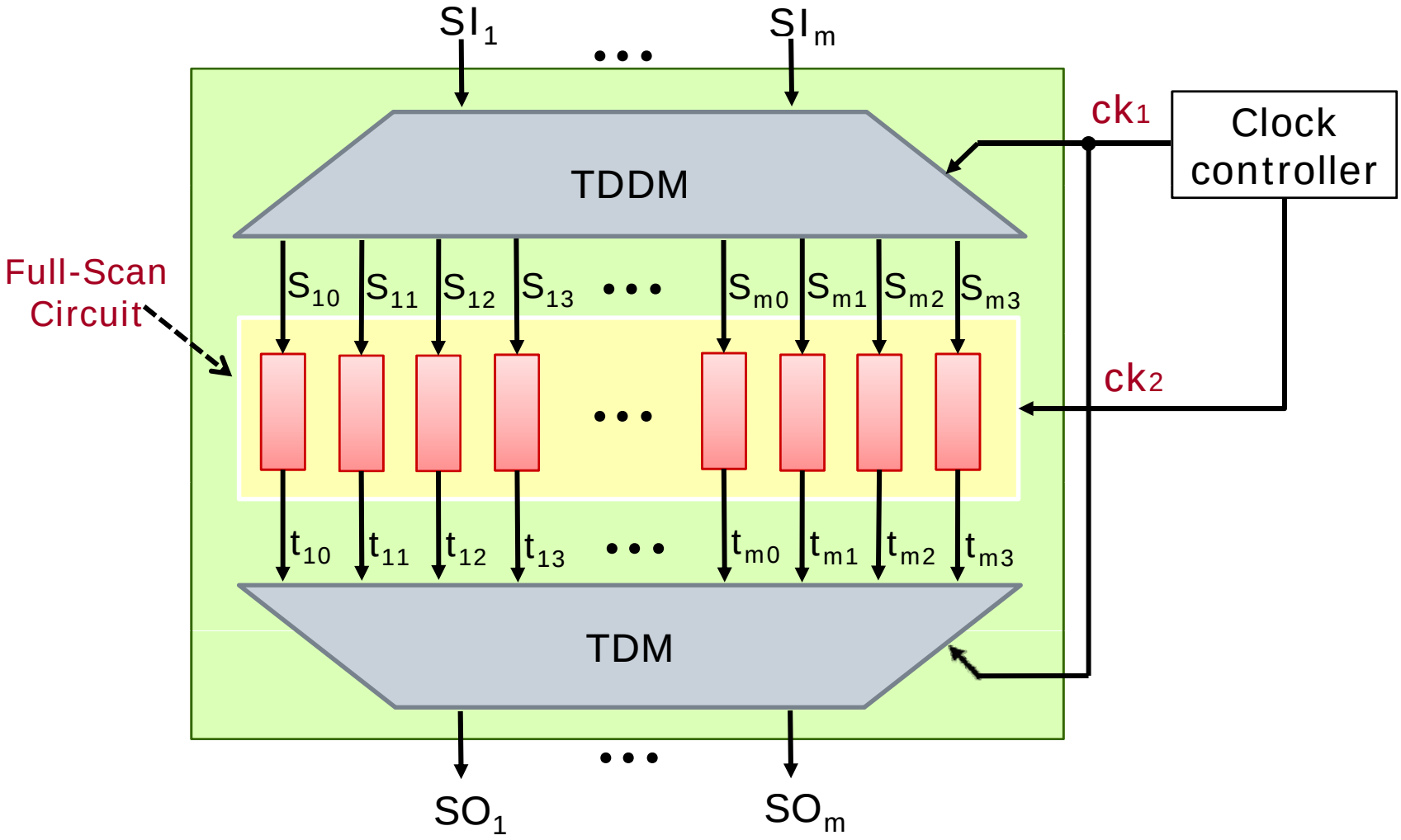
Low-Power Scan Architectures

- Test power is related to dynamic power
  - $P = 1/2fCV^2$
- Multi-phase low-power scan design

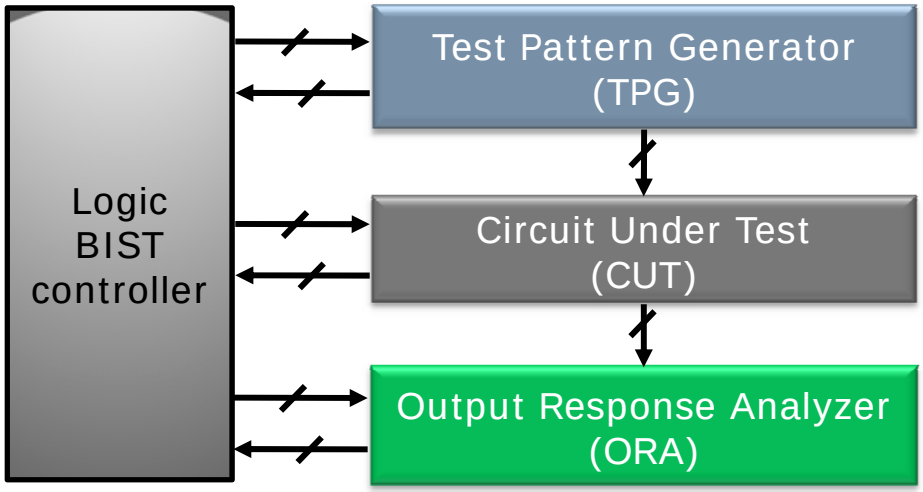


Low-Power Scan Architectures

- Bandwidth-matching low-power scan design



Typical Logic BIST System



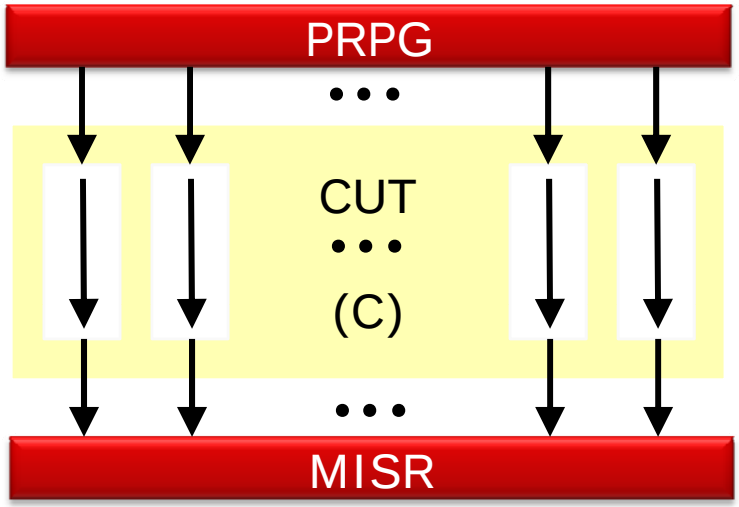
- TPG: generate test patterns
- ORA: compact the test responses of the CUT into a signature
- Controller: generates the scan enable signals and clocks

Logic BIST Architectures

- Off-line BIST architectures can be classified into two classes
  - Using the test-per-clock BIST scheme
  - Using the test-per-scan BIST scheme
- Comparison of test-per-clock and test-per-scan BIST schemes
  - Test-per-scan BIST: long test time, but low area cost
  - Test-per-clock BIST: short test time, but high area cost

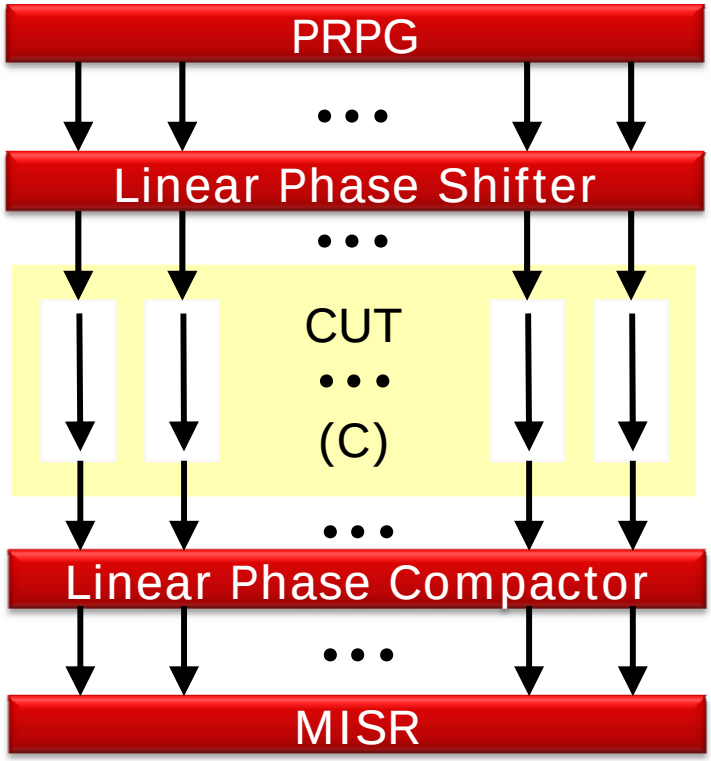
STUMPS

- STUMPS (self-testing using MISR and parallel SRSG)
  - A test-per-scan BIST design
  - MISR: multiple-input signature register
  - SRSG: shift register sequence generator
  - PRPG: parallel SRSG



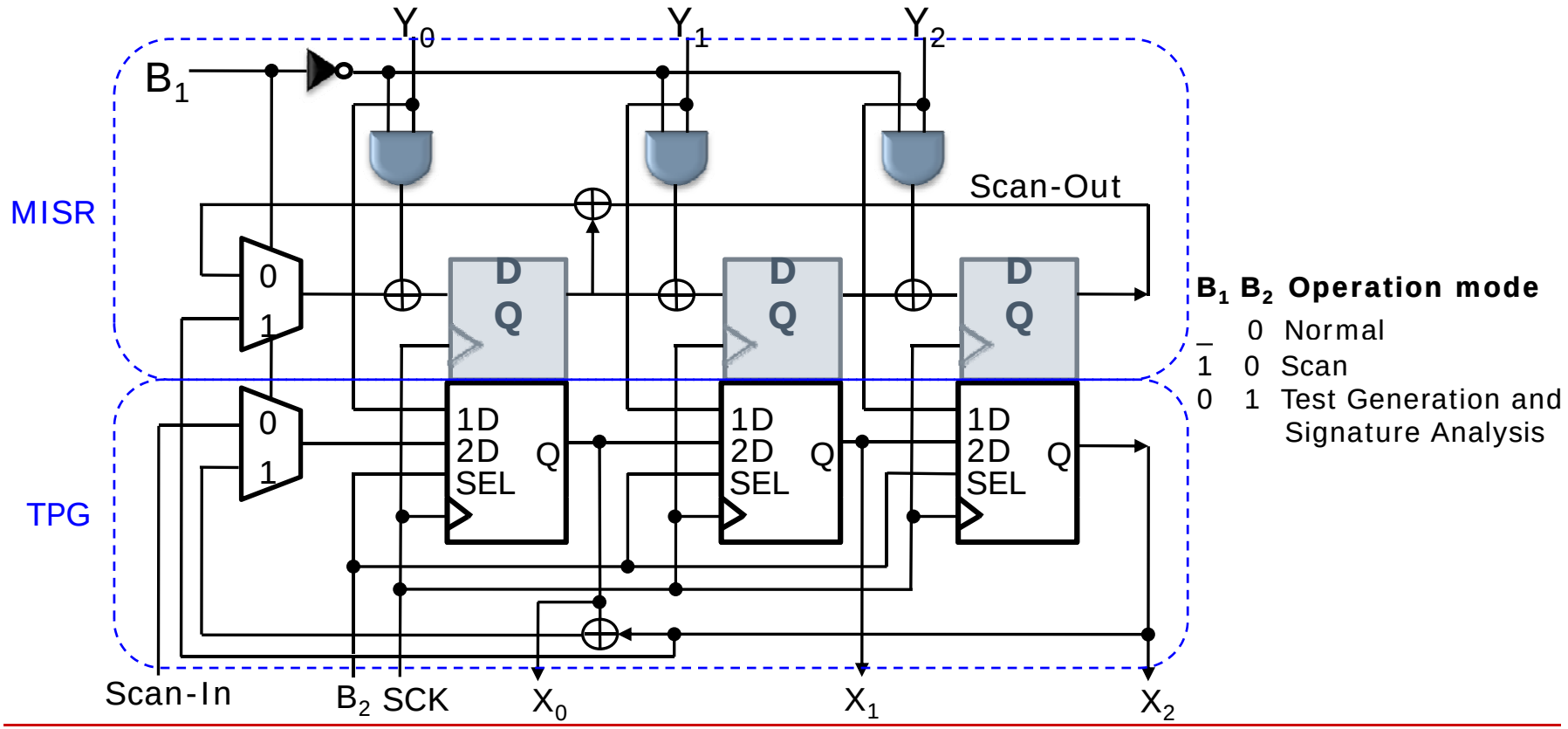
STUMPS-Based BIST Architecture

- To reduce the lengths of the PRPG and MISR and improve the randomness of the PRPG
  - An optional linear phase shifter and an optional linear phase compactor is used in industrial applications



CBILBO

- Concurrent built-in logic block observer (CBILBO)
  - Test-per-clock BIST scheme
  - No fault simulation is required
  - Area cost is higher than that of the STUMPS

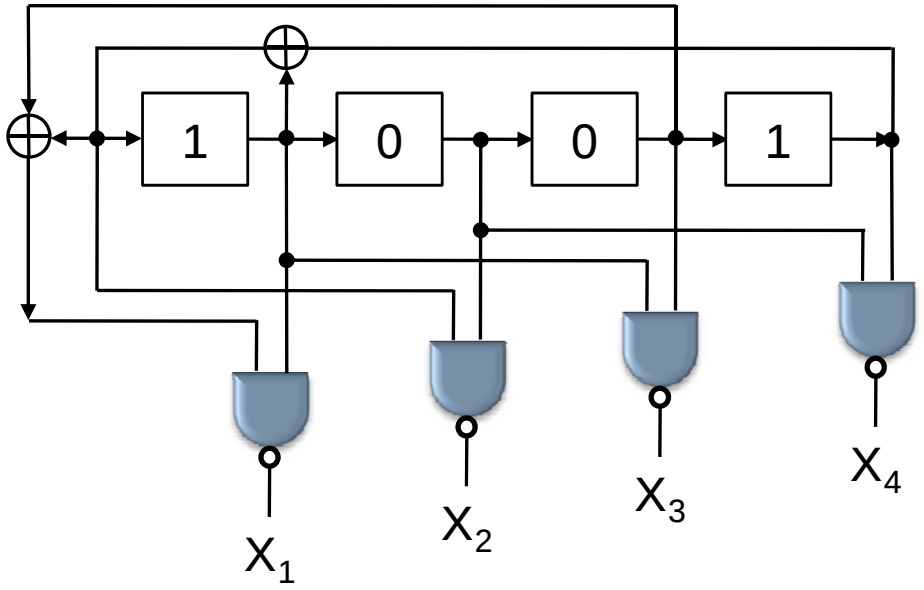


Coverage-Driven Logic BIST Scheme

- Pseudo-random test generation is usually used to serve as a TPG of a logic BIST
  - Fault coverage is limited by the presence of random-pattern resistant (RP-resistant) faults
- Four approaches can be used to enhance the fault coverage of a BIST scheme
  - Weighted pattern generation
  - Test point insertion
  - Mixed-mode BIST
  - Hybrid BIST

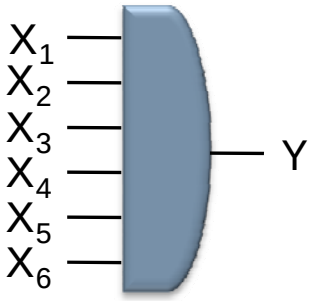
Weighted LFSR as PRPG

- Weighted pattern generator
  - Insert a combinational circuit between the LFSR and the CUT
  - Probabilities of the distributions of 0's and 1's at the input of the CUT can be changed



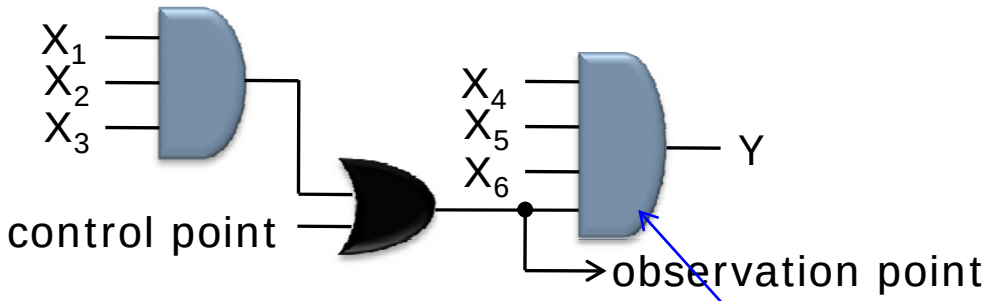
Test Point Insertion

- Weighted pattern generation is simple in design, but achieving adequate fault coverage for a BIST circuit remains a problem
- Test points can be used to increase the circuit's fault coverage to a desired level
- Example of inserting test points to improve detection probability



Min. Detection Probability $= \frac{1}{64}$

for Y SA0 or X_i SA1 faults



Min. Detection Probability $= \frac{7}{128}$

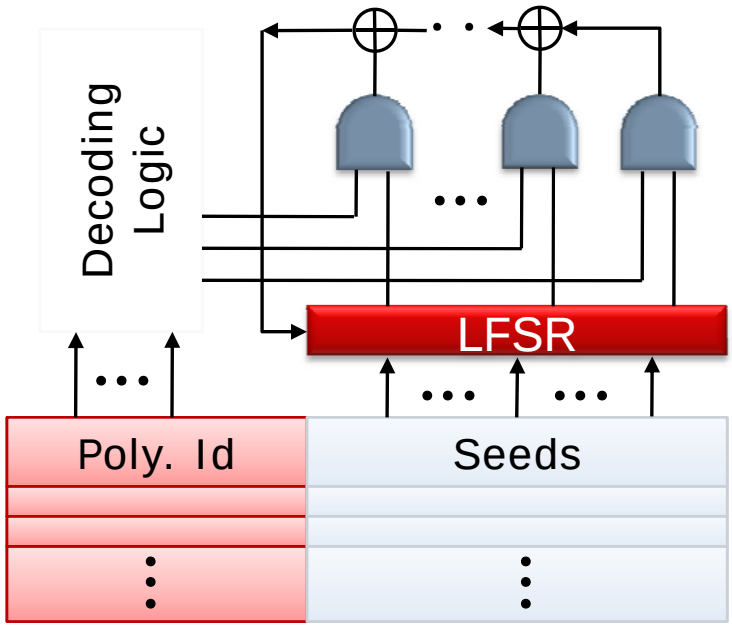
for Y SA0 or X_i SA1 faults

Mixed-Mode BIST

- A major drawback of test point insertion is that it requires modifying the circuit under test
- Mixed-mode BIST
  - Without modifying the CUT
  - Pseudo-random patterns are generated to detect RP-testable faults and then some additional deterministic patterns are generated to detect the PR-resistant faults
- Methods for generating deterministic patterns on-chip
  - ROM compression
  - LFSR reseeding
  - Embedding deterministic patterns
- ROM compression
  - The size of the required ROM is often prohibitive

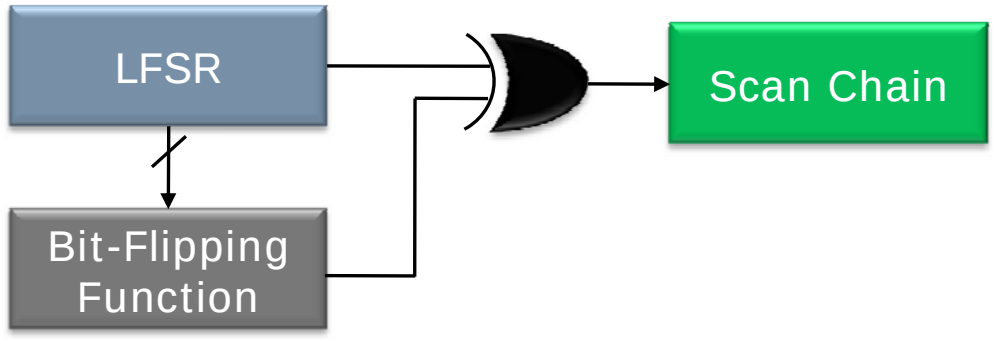
LFSR Reseeding

- Reseeding with multiple-polynomial LFSR



Embedded Deterministic Patterns

- Many pseudo-random patterns generated during pseudo-random testing do not detect any new faults
  - Some useless patterns can be transformed into deterministic patterns that detect RP-resistant faults
  - This can be done by adding mapping logic between the scan chains and the CUT or in a less intrusive way by adding the mapping logic at the inputs to the scan chains to either performing *bit-fixing* or *bit-flipping*
- Bit-flipping BIST

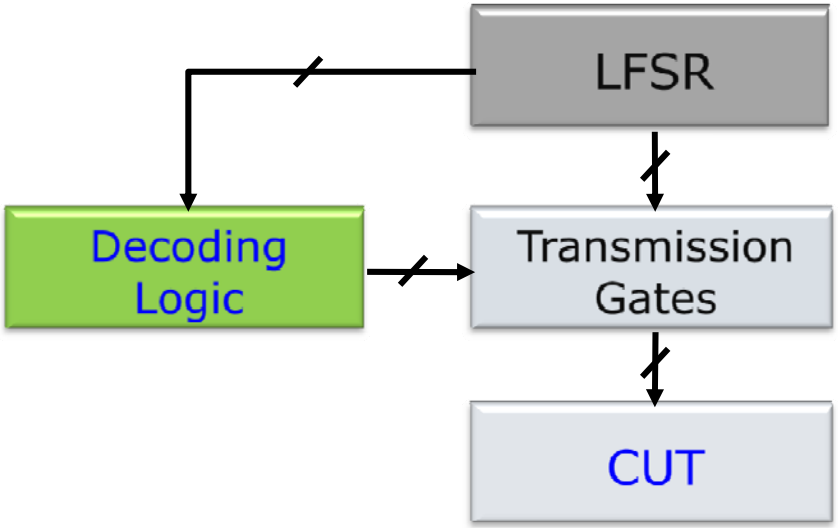


Hybrid BIST

- Using BIST circuit to detect the PR-testable faults and using ATE which applies deterministic patterns to detect the PR-resistant faults
- In an system-on-chip, test scheduling can be done to overlap the BIST run time with the transfer time for loading the deterministic patterns from the tester

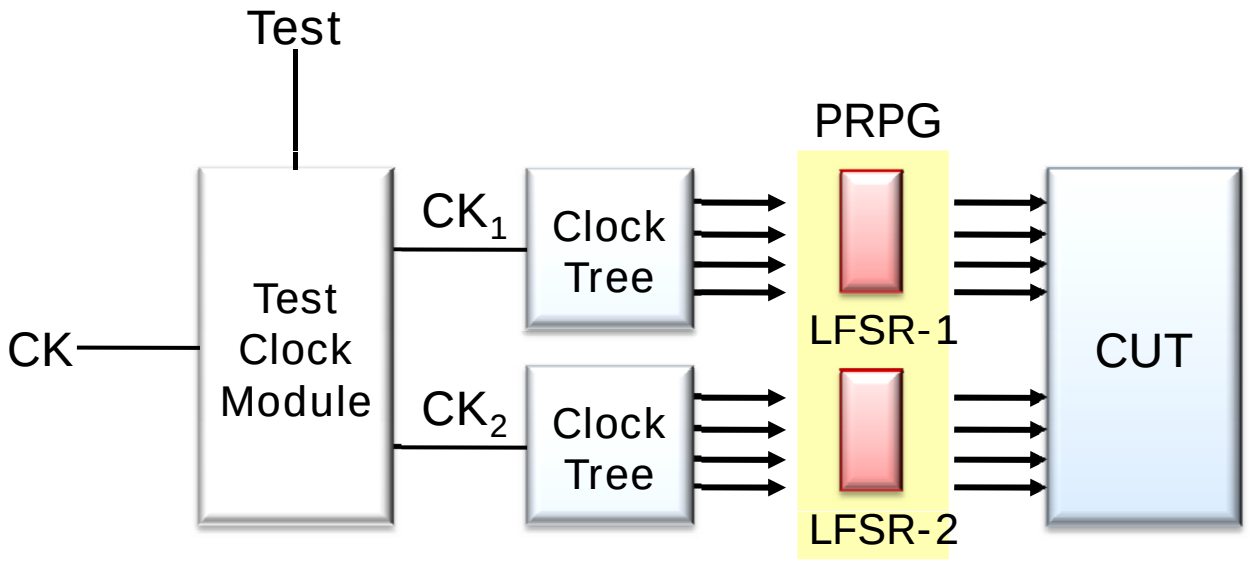
Low-Power Logic BIST Schemes

- Test-vector-inhibiting BIST scheme
  - Inhibit LFSR-generated pseudo-random patterns, which do not contribute to fault detection from being applied to the circuit under test



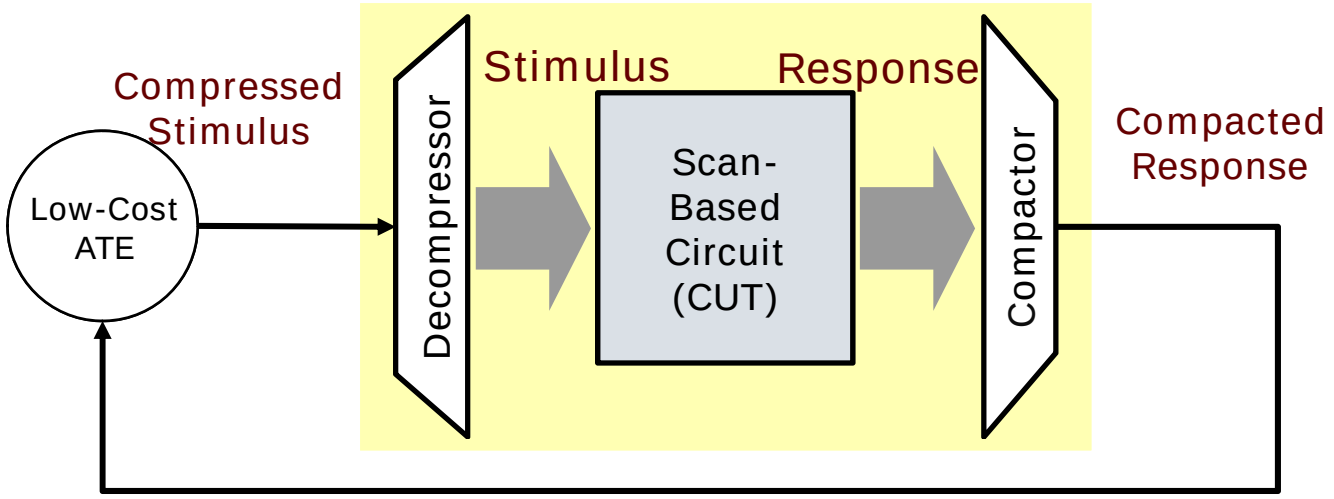
Low-Power Logic BIST Schemes

- Modified LFSR low-power BIST scheme
  - Partition an n-stages LFSR into two separated or interleaved n/2-stages LFSRs
  - A test clock module is used to generate the two non-overlapping clock, CK_1 and CK_2, for deriving LFSR-1 and LFSR-2
  - Only one part of the CUT is activated at any given time



Test Compression

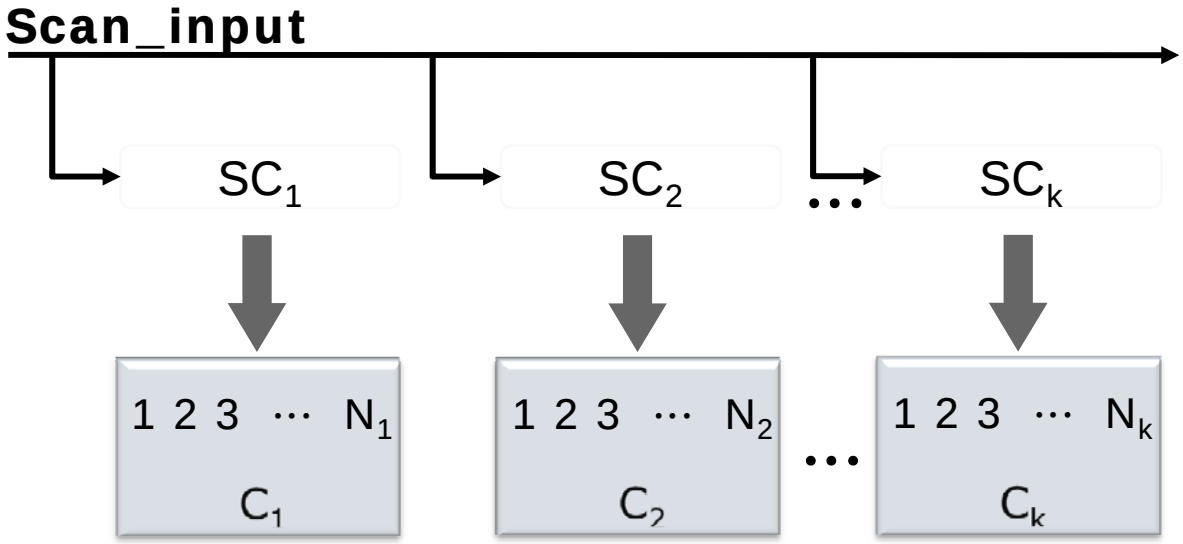
- Test data are inherently highly compressible because typically only 1% to 5% of the bits on a test pattern that generated by an ATPG program have specified (care) values
- Lossless compression techniques can thus be used to significantly reduce the amount of test stimulus data that must be stored on the tester



Broadcast Scan

- This method has been used as the basis of many test compression architectures, including some commercial DFT tools
- Concept of broadcast scan
  - Consider two independent circuits C1 and C2. Assume that these two circuits have their own test sets $T_1 = <t_{11}, t_{12}, \ldots t_{1k}>$ and $T_2 = <t_{21}, t_{22}, \ldots t_{2l}>$, respectively
  - In the beginning of the ATPG process, usually random patterns are initially used to detect the easy-to-detect faults. Some random patterns are used for C_1 and C_2, thus we may have $t_{11} = t_{21}$, $t_{12} = t_{22}$, …., up to some *i*th pattern
  - Then, deterministic patterns are generated for hard-to-detect faults. Typically, these patterns have many "don't care" bits
  - For a pattern for C_1, we can assign specific values to the don't care bits in the pattern to detect faults in C_2

Broadcast Scan Architecture

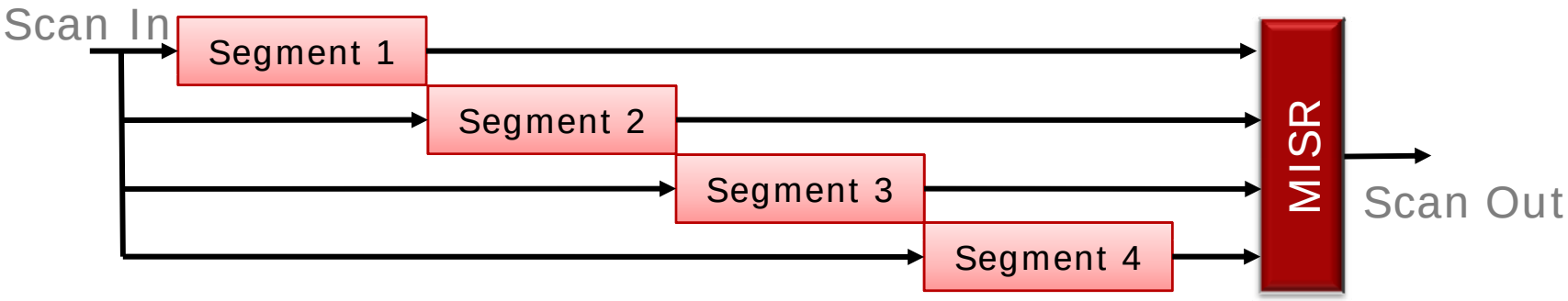


- Advantages
  - All faults that are detectable in all original circuits will also be detectable with the broadcast structure
- Broadcast scan can also be applied to multiple scan chains of a single circuit if all subcircuits driven by the scan chains are independent

Illinois Scan

- Issue in broadcast scan
  - If two scan chains are sharing the same channel, then the ith scan cell in each of the two scan chains will always be loaded with identical values. If some fault requires two such scan cells to have opposite values in order to be detected, it will not be possible to detect this fault with broadcast scan
- Illinois scan architecture
  - The scan architecture consists of two modes of operations, namely a broadcast mode and a serial scan mode
  - The serial scan mode is used for the remaining faults that cannot be detected in broadcast mode
  - Drawback: the compression ratio is degraded

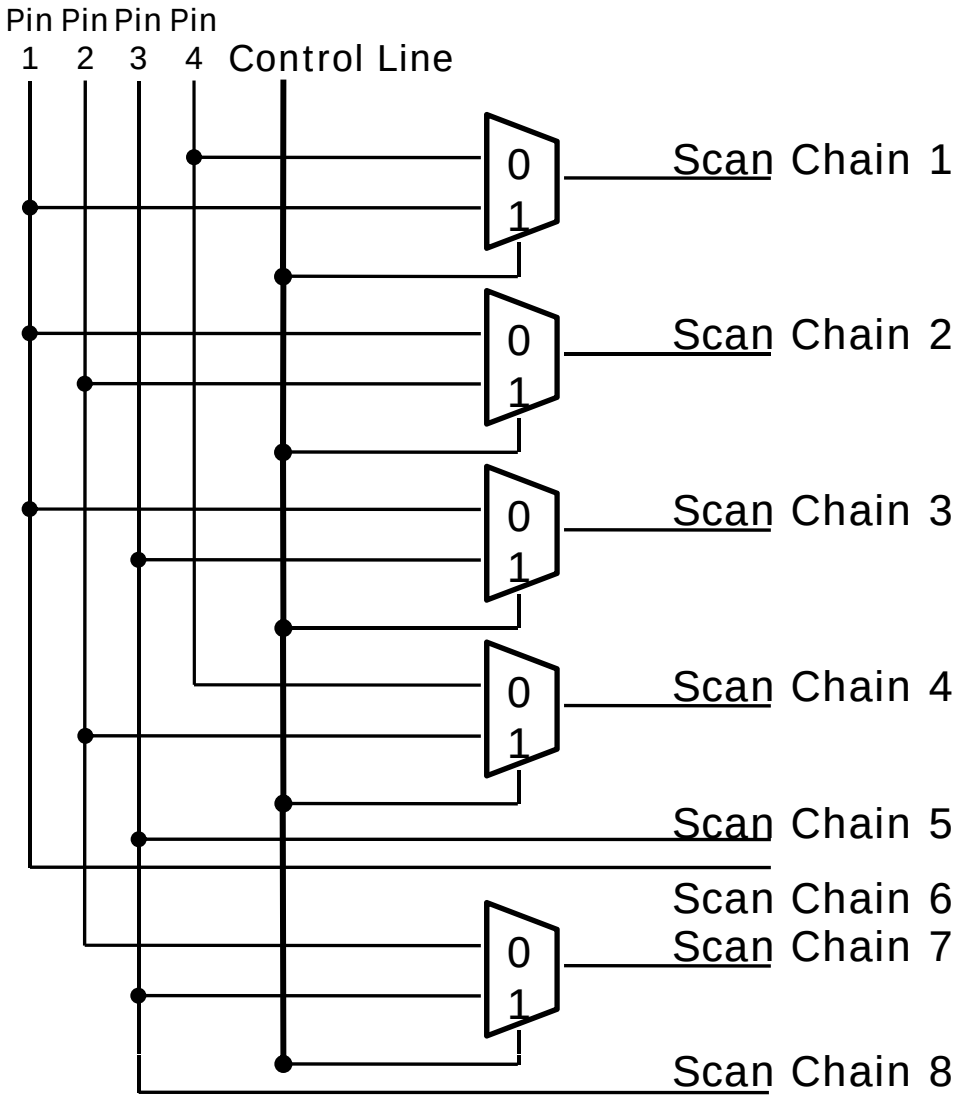
Illinois Scan Architecture



(a) Broadcast mode

(b) Serial chain mode

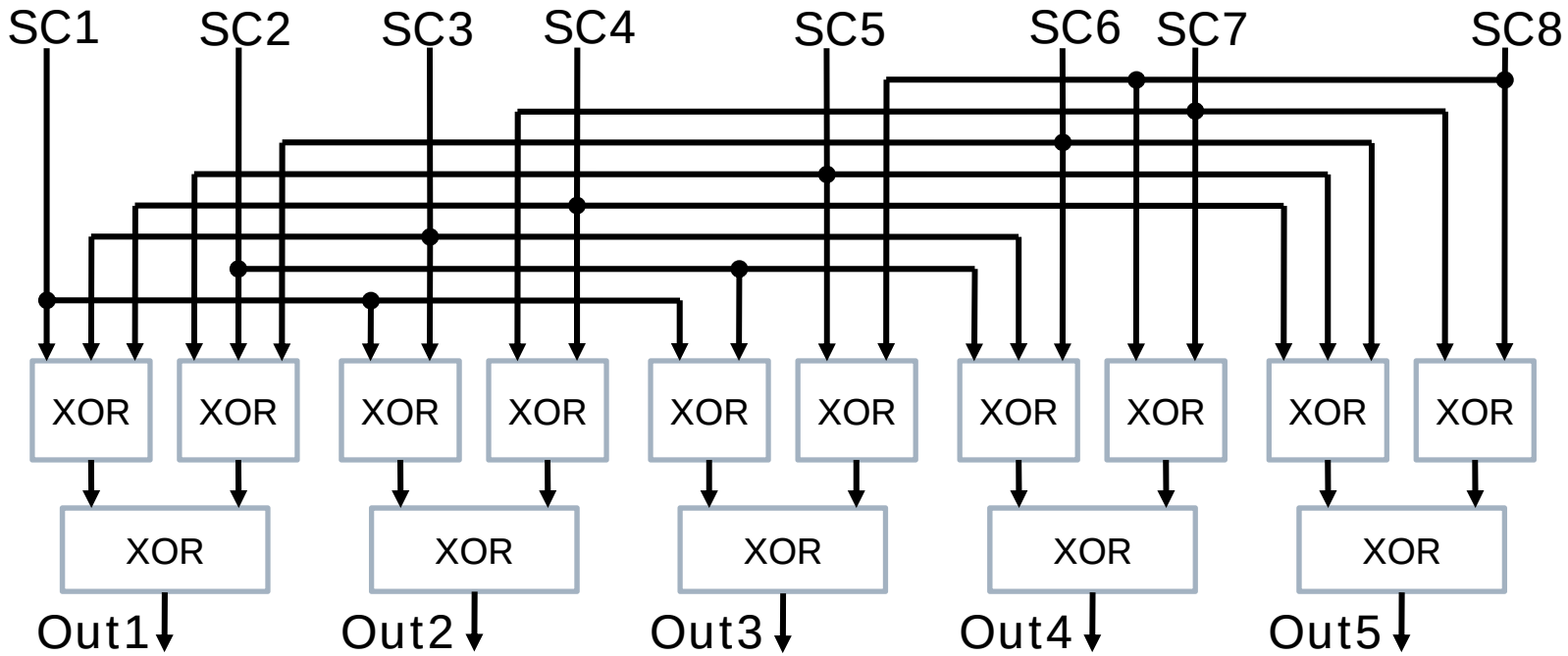
Reconfigurable Broadcast Scan



Test Response Compaction

- Test stimulus compression must be lossless, but test response compaction can be lossy
- Test compaction schemes
  - Space compaction
  - Time compaction
  - Mixed space and time compaction
- Difference between space compaction and time compaction
  - A space compactor compacts an m-bit-wide output pattern to a p-bit-wide output pattern, where p<m
  - A time compactor compacts n output patterns into q output patterns, where q<n

X-Tolerant Response Compaction

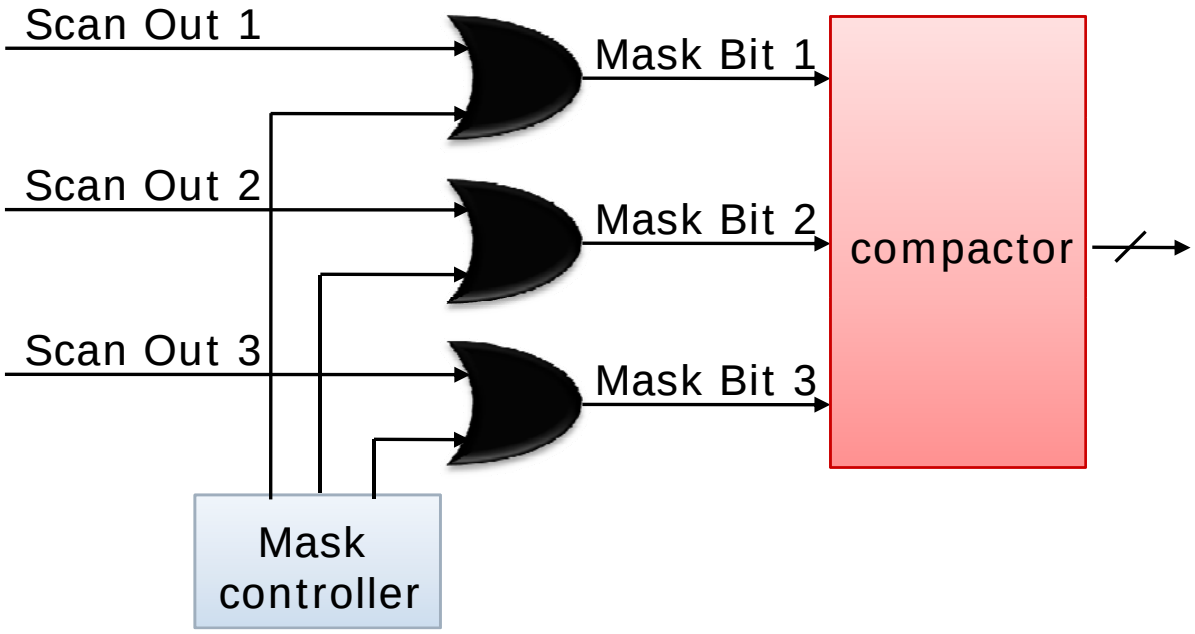


$$M = \begin{pmatrix} 11100 \\ 10110 \\ 11010 \\ 11001 \\ 10101 \\ 10011 \\ 01011 \\ 00111 \end{pmatrix}$$

X-Tolerant Response Compaction

- Theorem 1
  - If only a single scan chain produces an error ay any scan-out cycle, the X-compactor is guaranteed to produce errors at the X-compactor outputs at the scan-out cycle if and only if no row of the X-compact matrix contains all 0's.
- Theorem 2
  - Errors from any one, two, or odd number of scan chains at the same scan-out cycle are guaranteed to produce errors at the X-compactor outputs at that scan out cycle if every row of the X-compact matrix is nonzero, distinct, and contains an odd number of 1's.

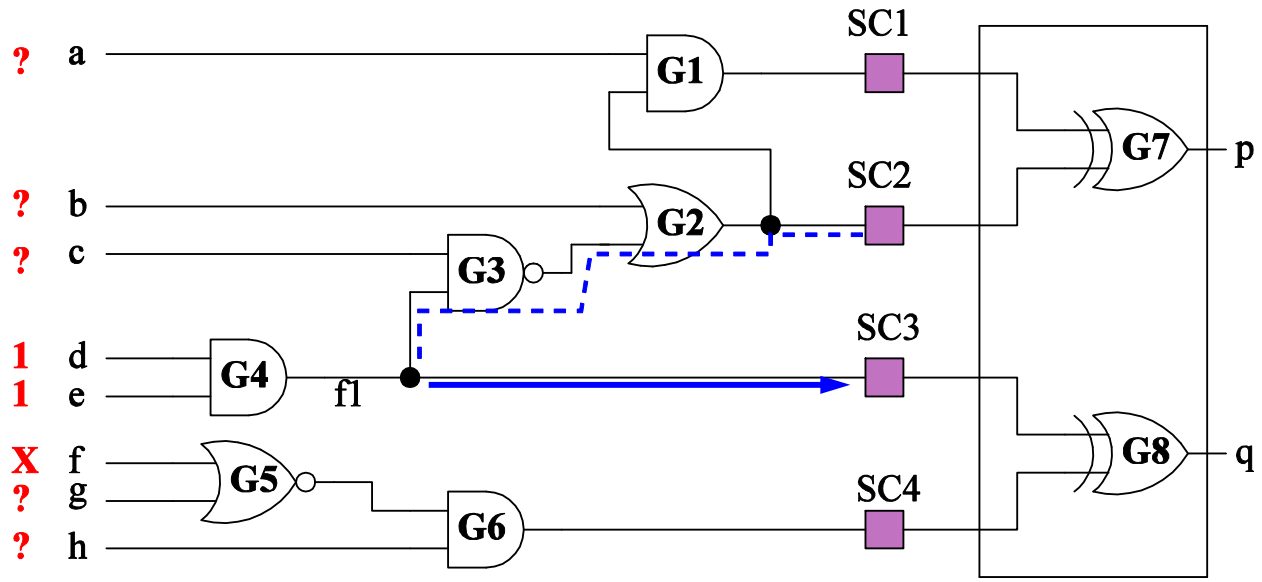
X-Masking Technique



- Mask data are needed to indicate when the masking should take place. These mask data can be stored in compressed format and can be decompressed using on-chip hardware.

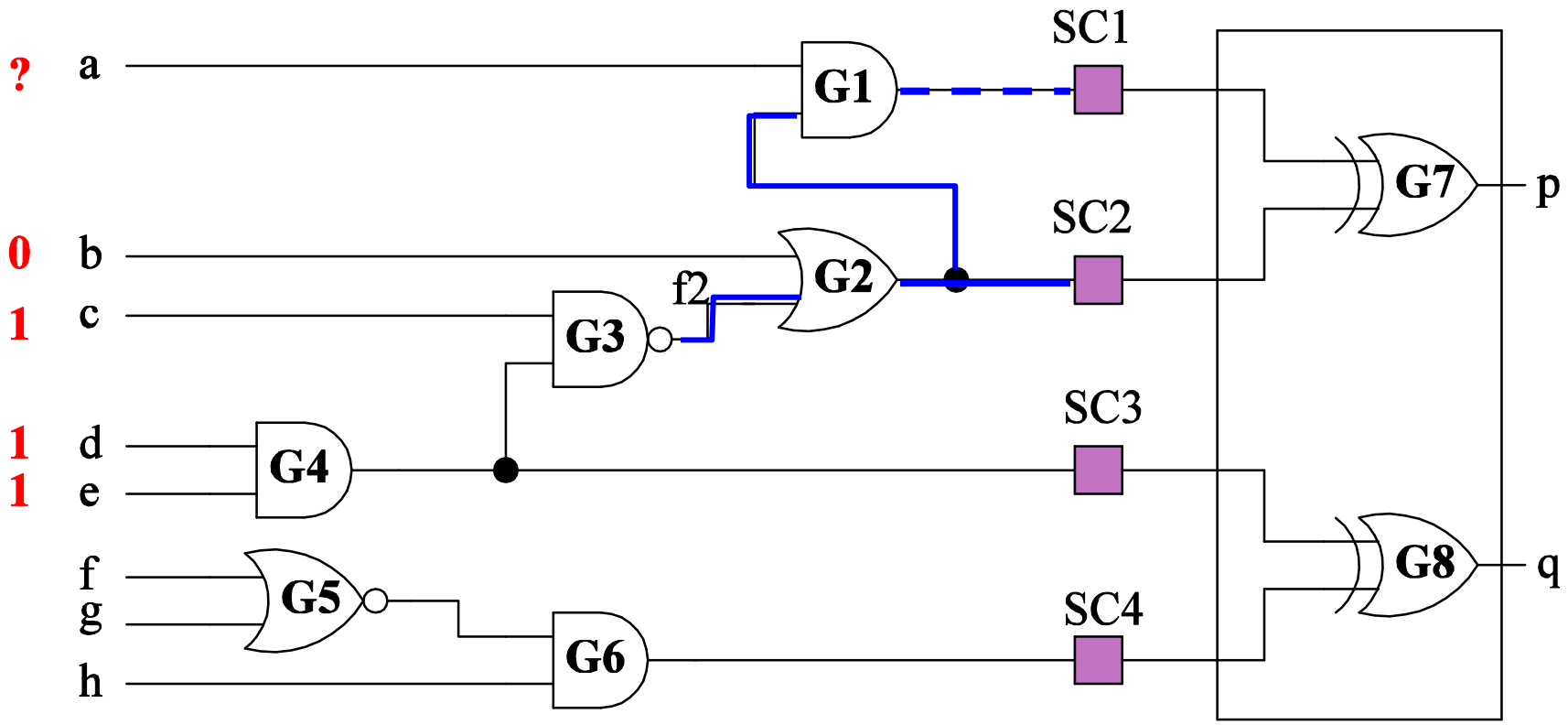
X-Impact Technique

- X-impact technique uses ATPG to algorithmically handle the impact of residual X's on the space compactor without adding any extra circuitry
- Example 1: handling of Xs (f1 has a stuck-at-0 fault)



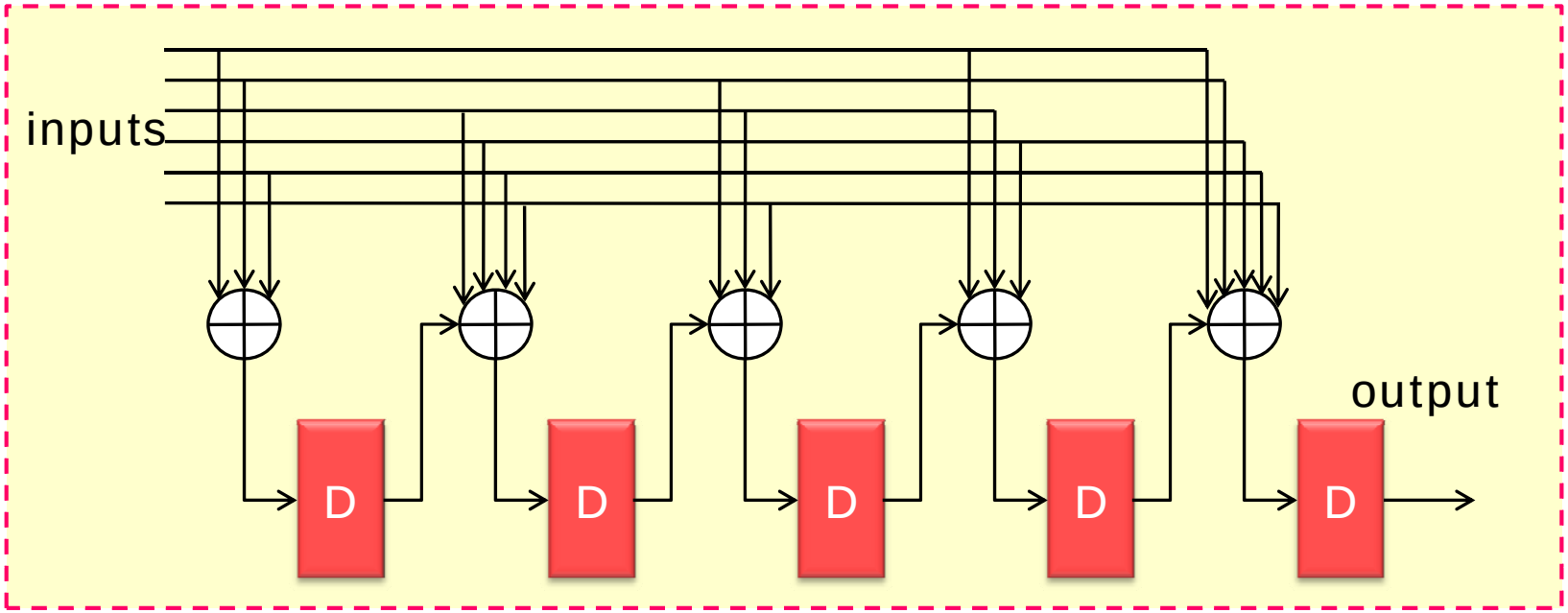
X-Impact Technique

- Example 2: handling of aliasing (f2 has a stuck-at-1 fault)



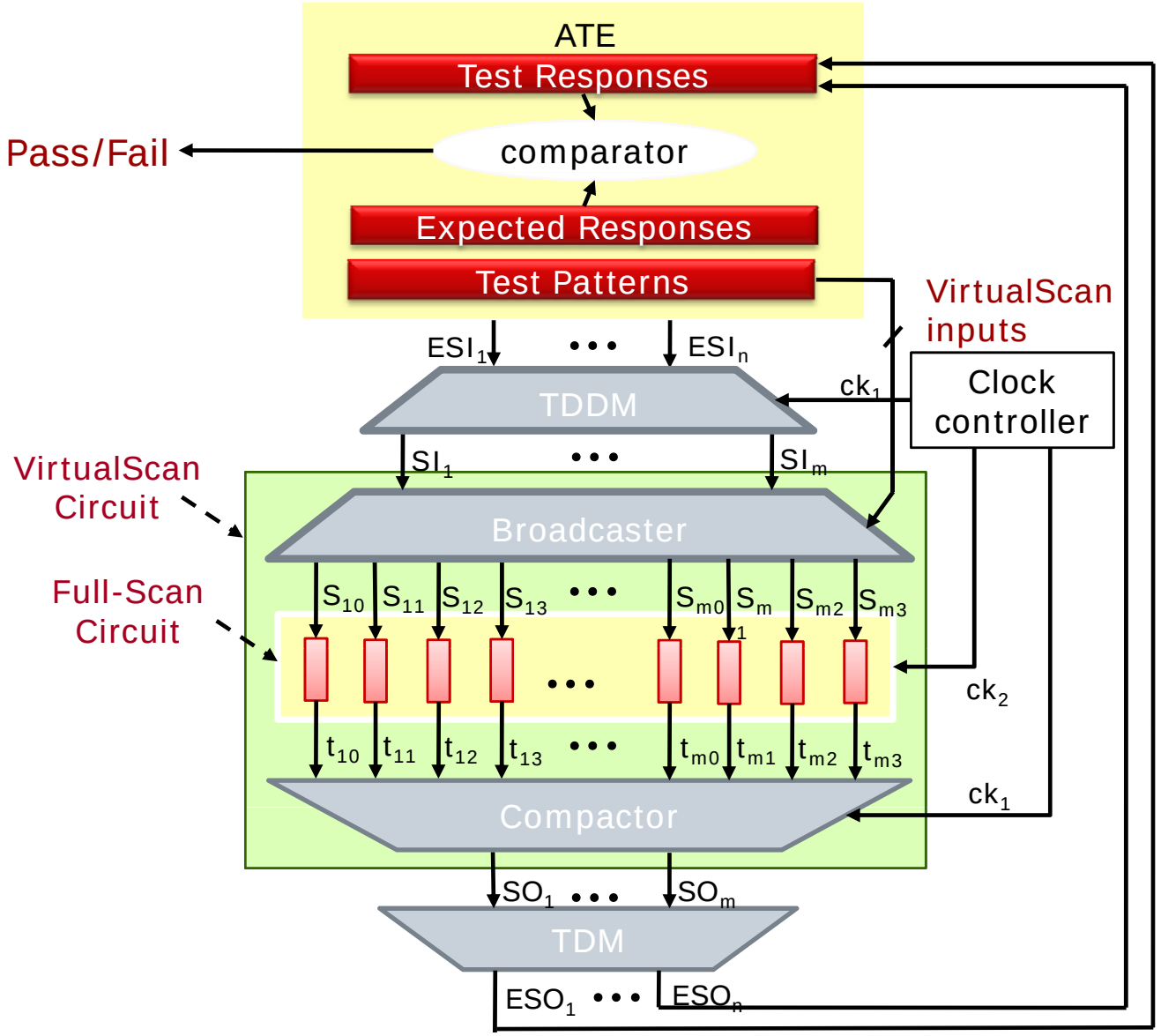
Mixed Time and Space Compaction

- q-compactor with single output



- Different from a conventional MISR, a q-compactor does not have a feedback path
  - Any error or X injected into the compactor is shifted out after at most five cycles

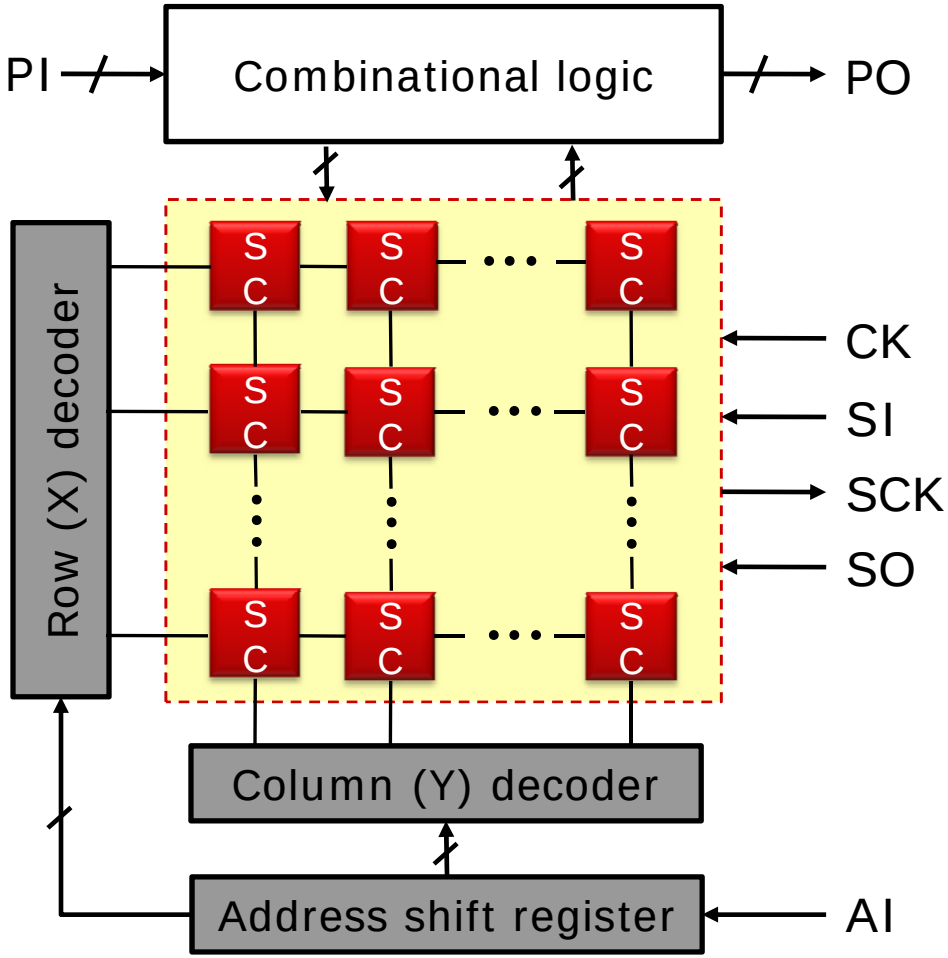
UltraScan Architecture



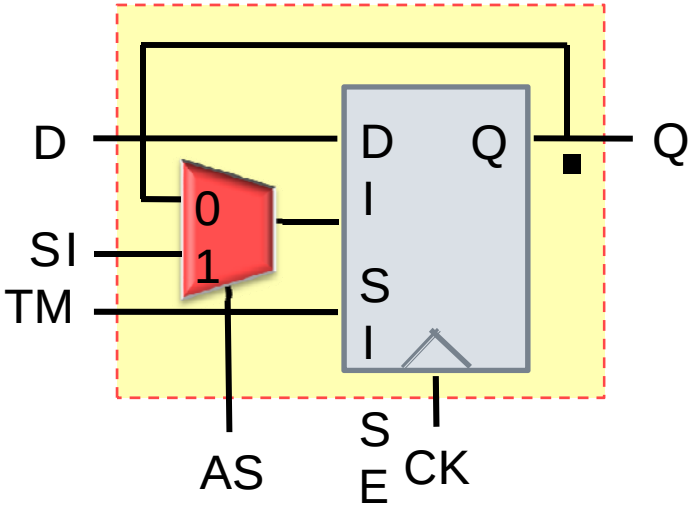
Random Access Scan

- Serial scan design
  - Advantage: low routing area overhead
  - Disadvantages: high power dissipation during shifting and capture operations; fault diagnosis is difficult
- Random access scan offers a promising solution
  - Rather than using various hardware and software approaches to reduce test power dissipation in serial scan design, random-access scan attempts to alleviate these problems by making each scan cell randomly and uniquely addressable

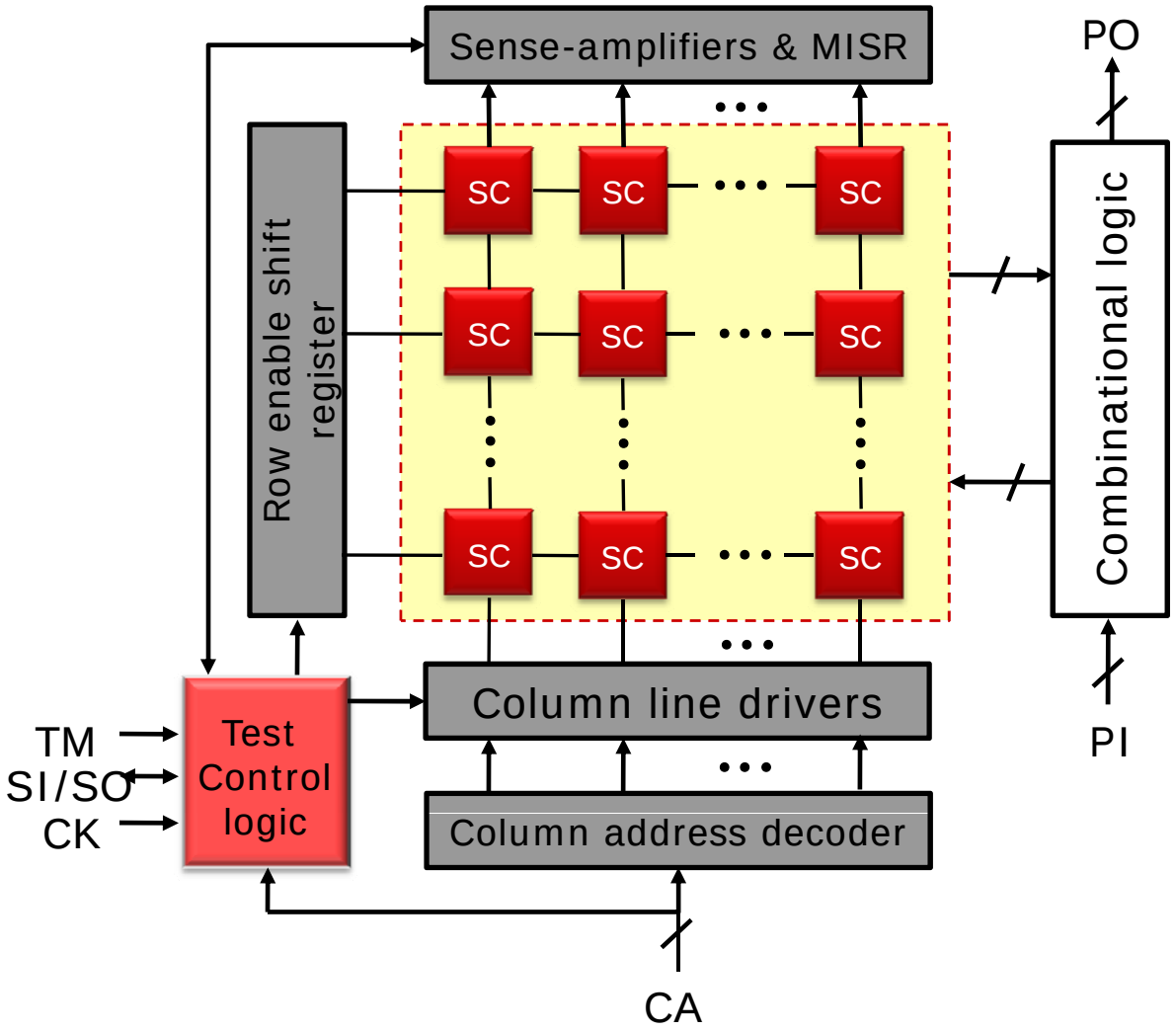
Typical Random Access Scan Architeture



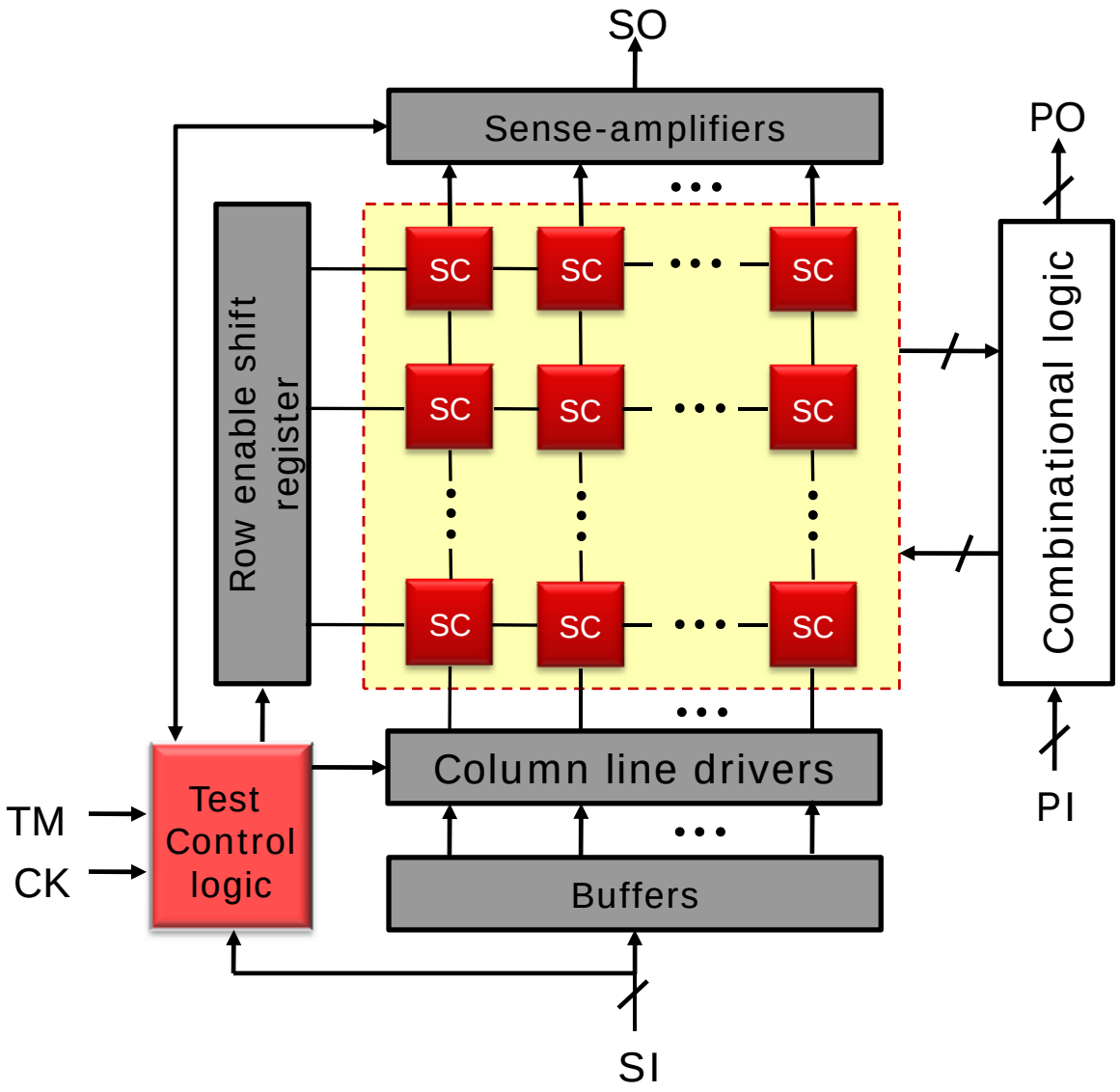
Typical Random-Access Scan Cell



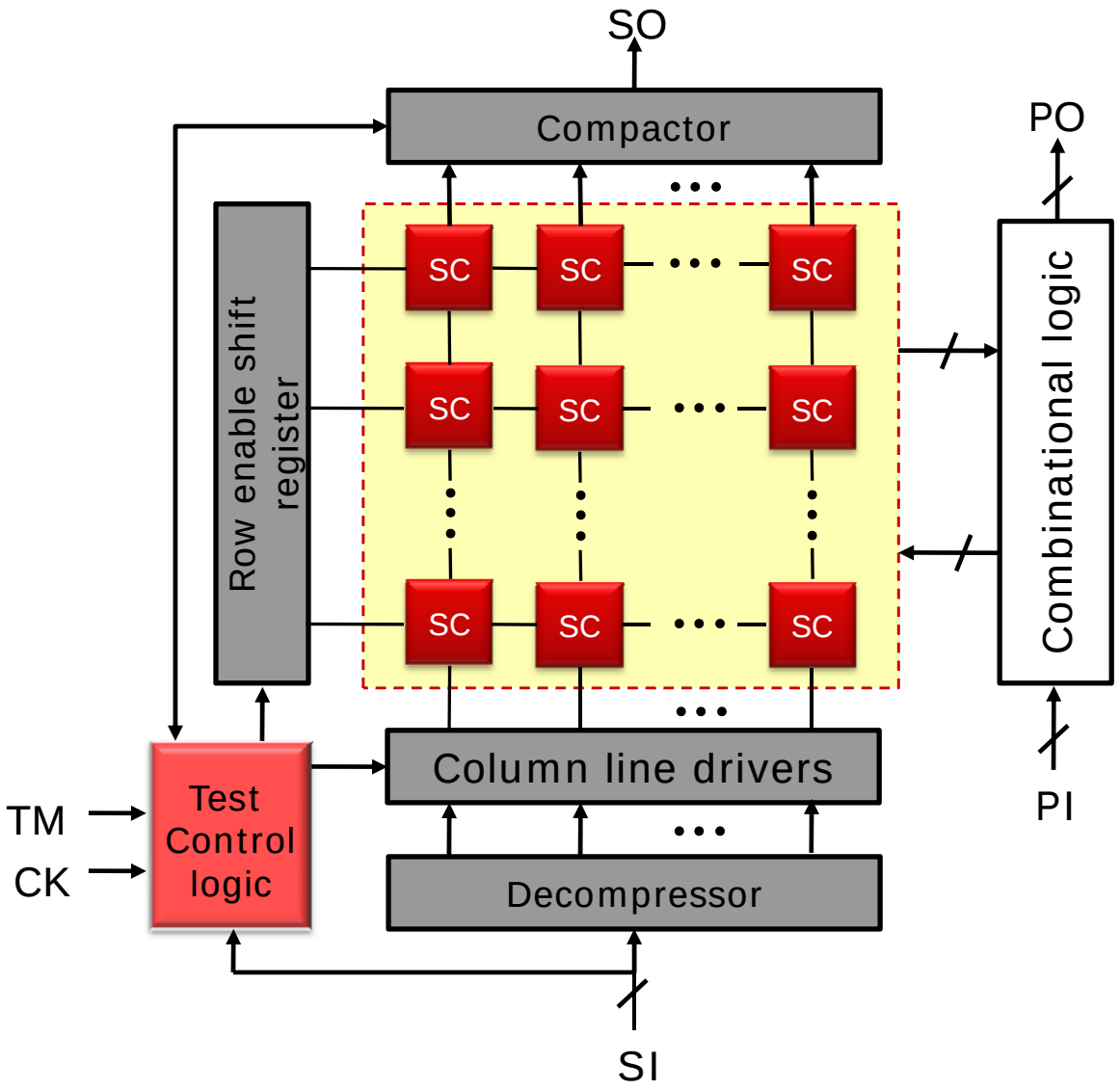
Progressive Random-Access Scan



Shift-Addressable Random-Access Scan



STAR Compression Architecture



Reconfigurable STAR Compression Architecture