Chapter 5
System / Network-on-Chip Test Architectures

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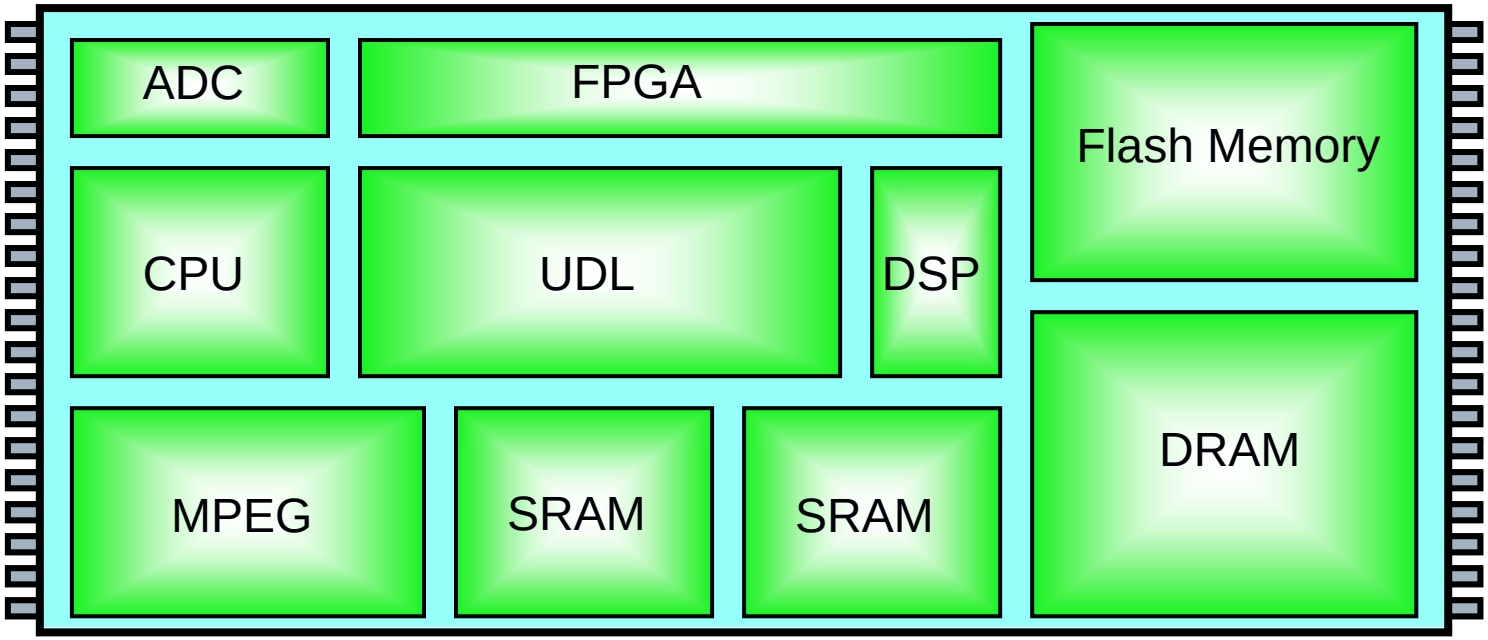
Outline

- Introduction
- SoC Test Challenge
- SoC Test Access Mechanisms
- SoC Test Control Architectures
- NoC Testing

What is an SOC?

- Definition
  - Integration of multiple cores (e.g., microprocessor, digital signal processor, RAM, ROM, flash memory, I/Os, and analog components which make a complete system) onto a single chip



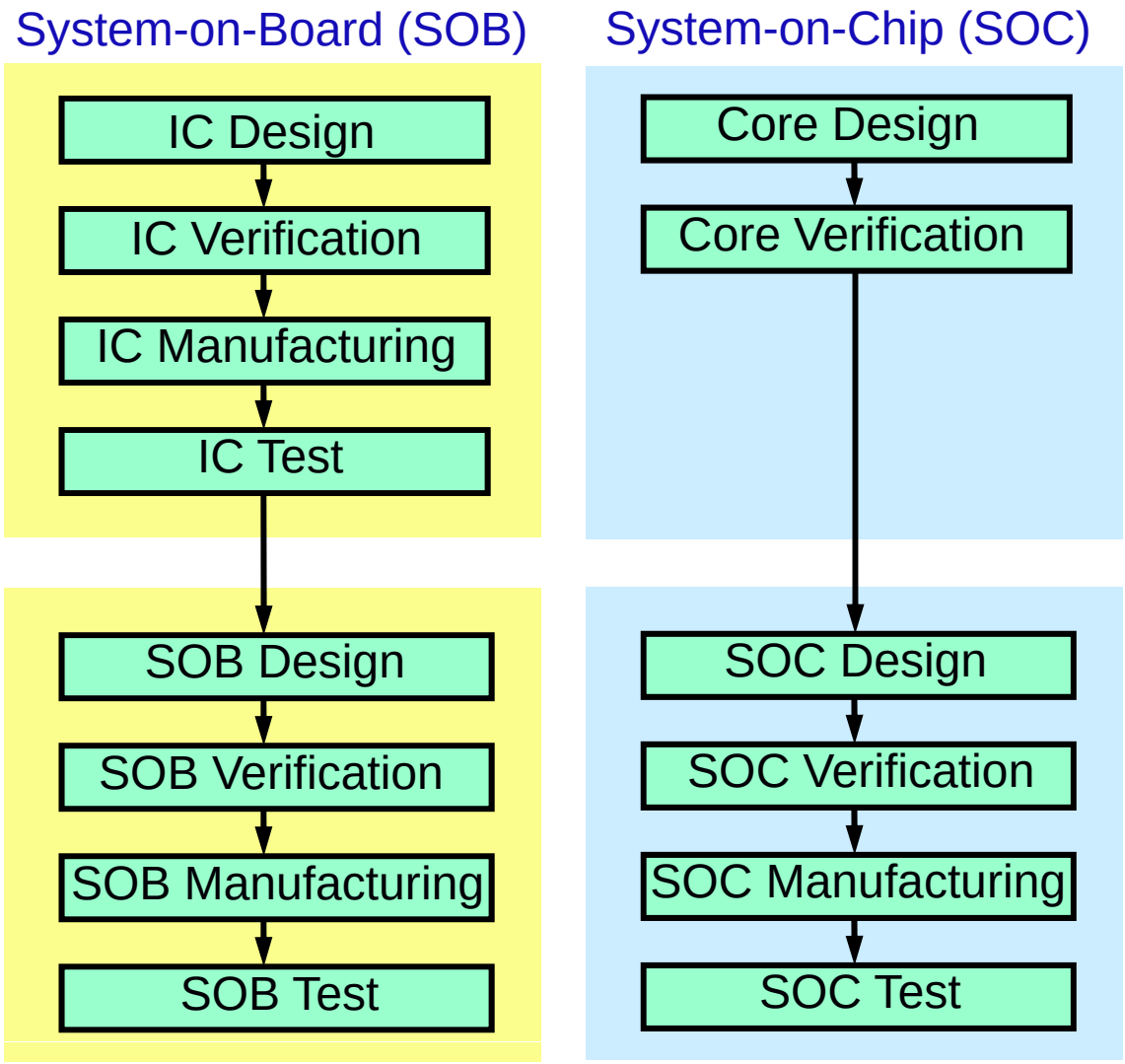
What are Cores?

- Definition
  - Predefined, pre-verified complex functional blocks, also known as IPs, virtual components
- Examples
  - Processor Cores: ARM, MIPS, IBM PowerPC
  - Peripherals: MMU, DMA Controller
  - Interface: PCI, USB, UART
  - Multimedia: JPEG compression, MPEG decoder
  - Networking: Ethernet Controller, MAC
- Various core description levels
  - Soft cores: register-transfer level (synthesizable HDL)
  - Firm cores: gate-level netlist (Verilog netlist)
  - Hard cores: layout (GDS2)

Traditional & Core-Based IC Design

- Traditional IC design
  - IC is designed from scratch
  - Reuse of small modules: standard-cell library and memory modules
- Core-based IC design
  - Reuse of large modules: cores, IP, virtual components
  - Divide-and-conquer design methodology
  - Definition of standards to make reuse easy
  - Reduce time-to-market

Difference Between SOB and SOC



- Analogy

  Reuse of predeisgned components in a system

- Difference

  Cores in SOC are fabricated and tested in the final system

[Zorian, et al.-ITC97]

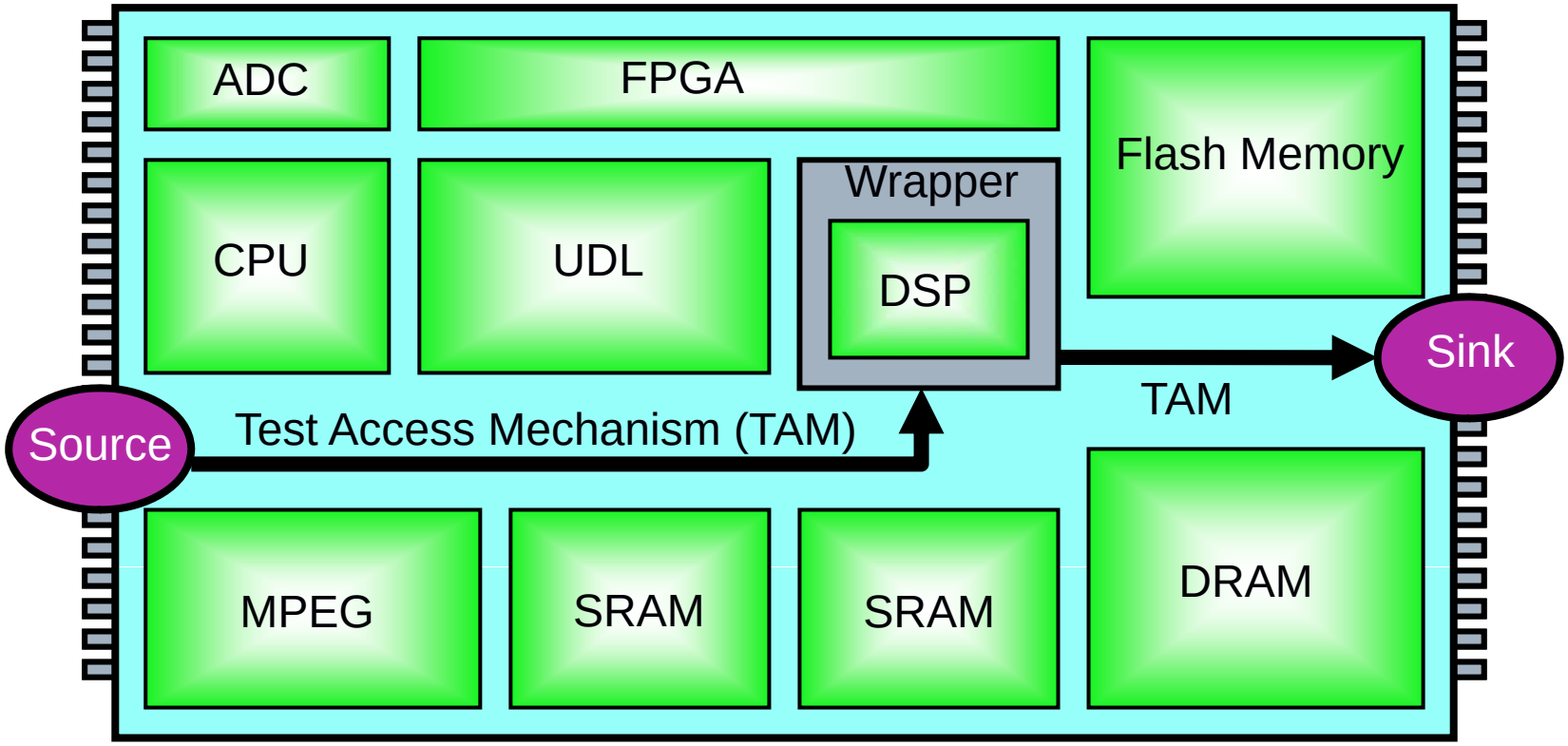
What are The Test Challenges?

- Distributed design and test development
  - Mixed technologies: logic, processor, memory, analog
    - Need various ATPG/DFT/BIST/other techniques
  - Multiple hardware description levels for cores
    - Need test plan for the various levels
  - Different core providers and SOC test developers
    - Need standard for test integration
- Deeply embedded cores
  - Need electronic test access mechanism
- Core/test reuse
  - Need plug-and-play test mechanism

What are The Test Challenges?

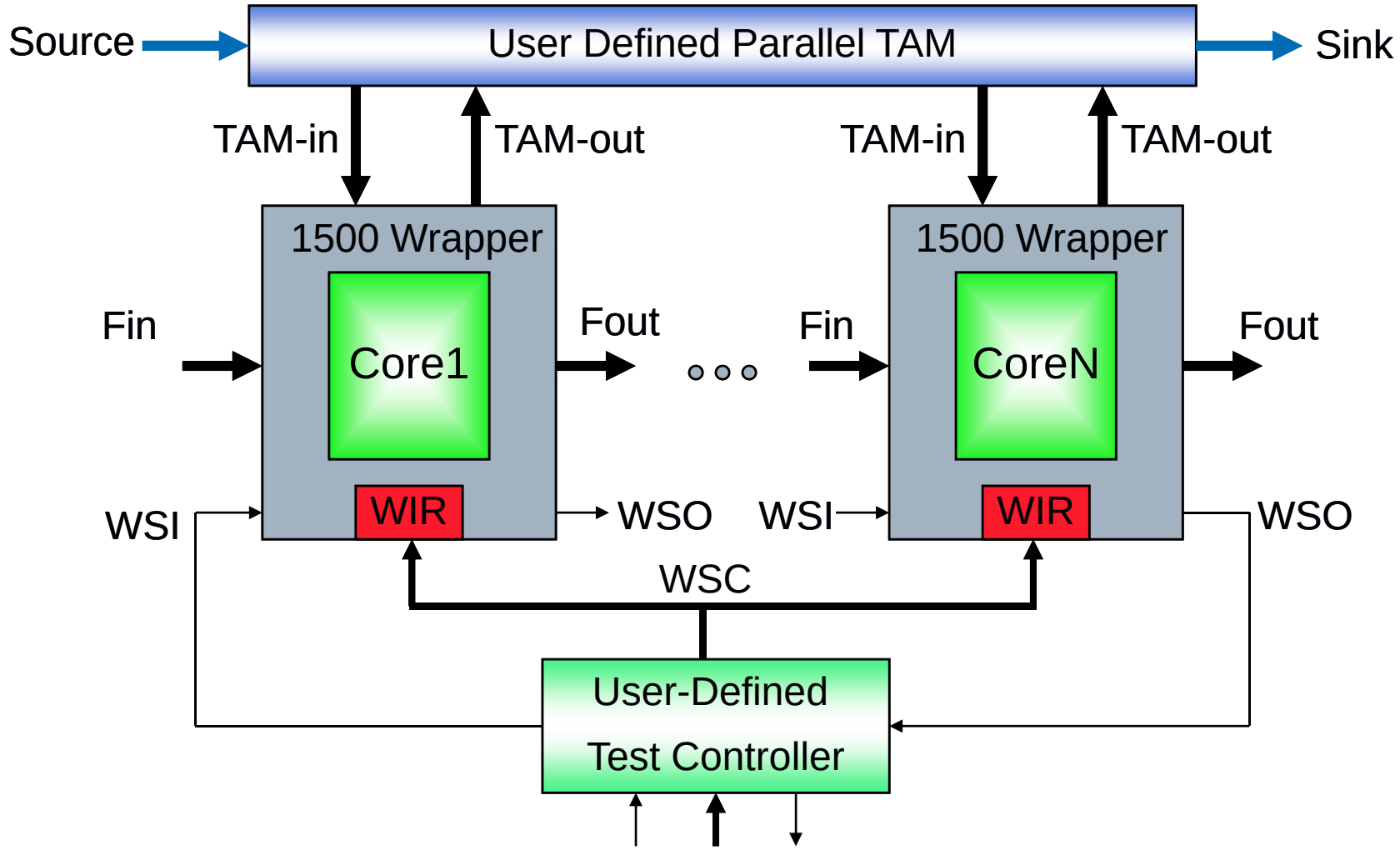
- Hierarchical core reuse
  - Need hierarchical test management
- SOC-level test optimization
  - Test time can be extremely large
    - Need parallel testing or test scheduling
  - Test power must be considered
    - Need low-power design or test scheduling
  - Testable design automation
    - Need new testable design tools and flow
  - Test economic consideration
    - Need to determine test strategy and overall test plan
- SOC yield improvement
  - Large amount of defect-sensitive memory cores
    - Need cost-effective repair techinques

Generic Test Access Structure

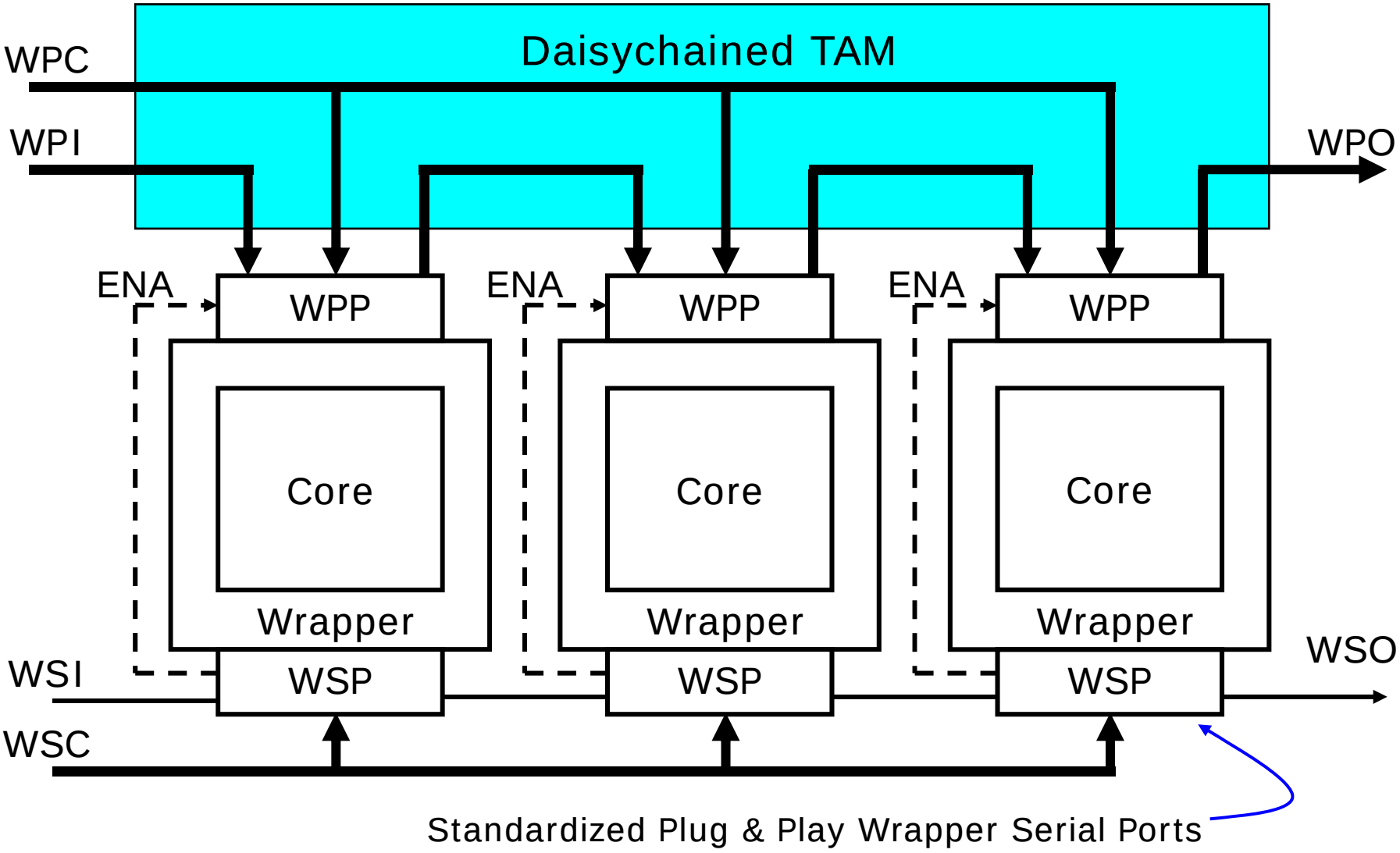


[Y. Zorian, et al.-ITC98]

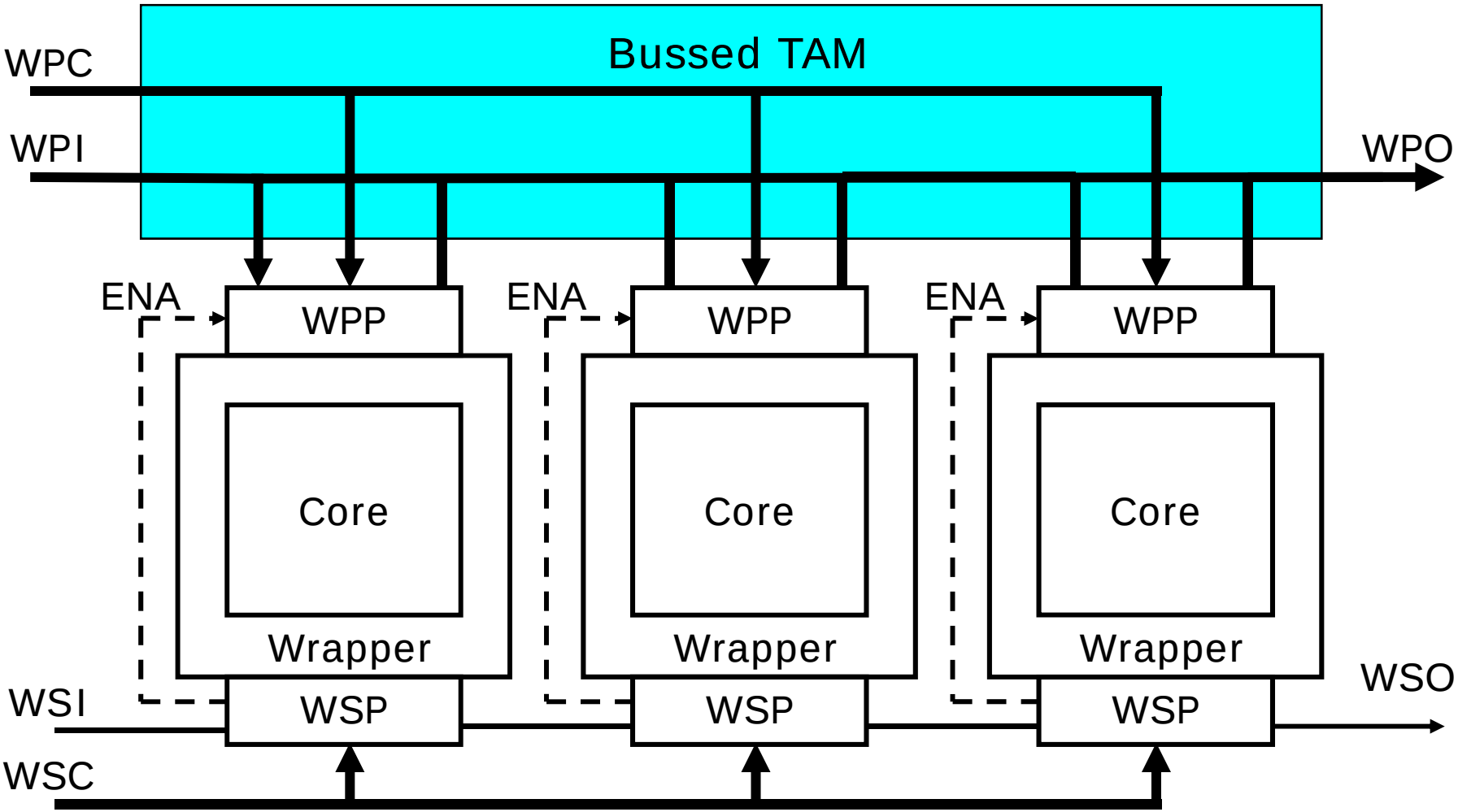
1500 Test Scalable Structure



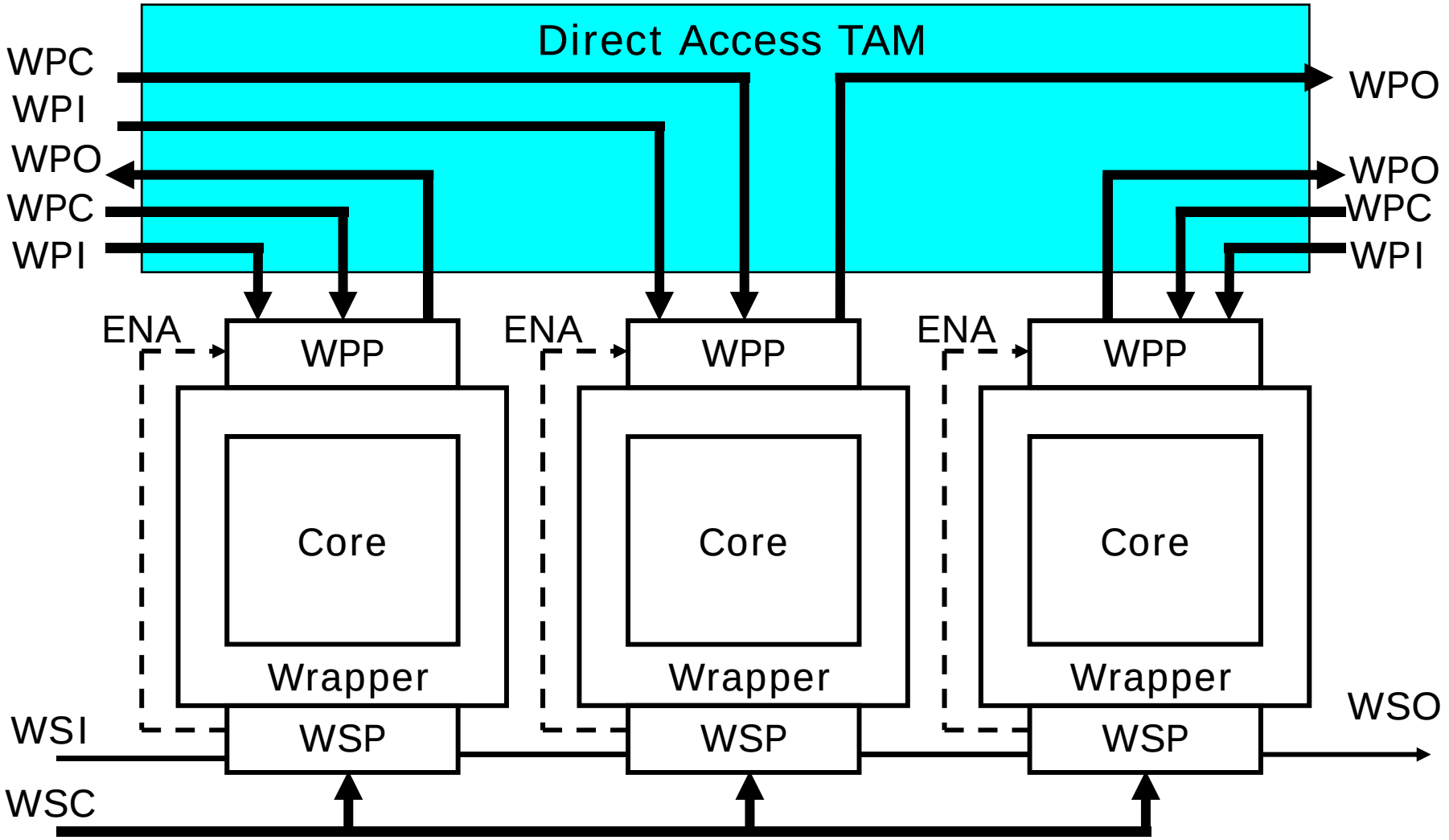
1500 Parallel TAM Configuration



1500 Parallel TAM Configuration



P1500 Parallel TAM Configuration

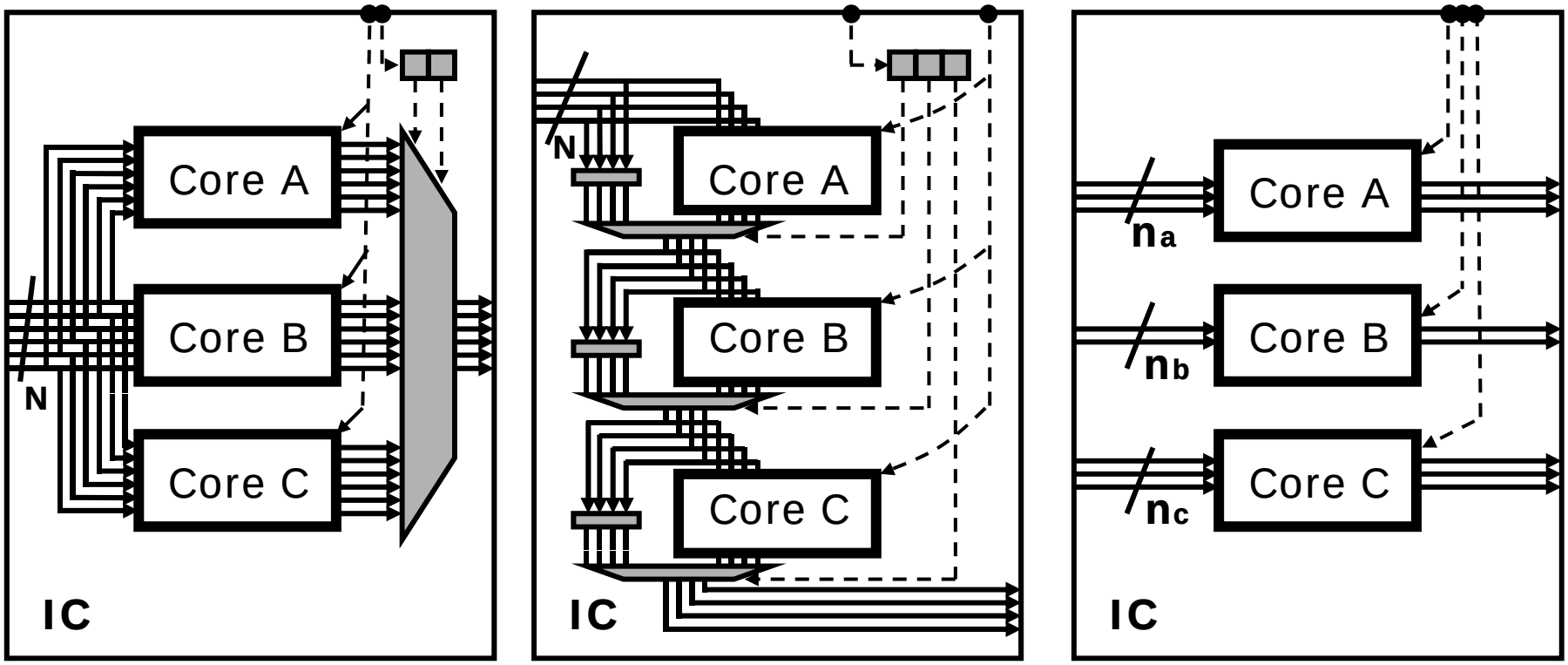


TAM Implementations

- Many TAM implementation have been reported
- Examples:
  - Multiplexed access
  - Reused system bus (AMBA)
  - Transparency
  - Boundary Scan
  - Scalable TAMs (Test bus, TestRail)
- On one SOC, different TAMs may co-exist

Multiplexed Access [E. J. Marinissen, ITC98]

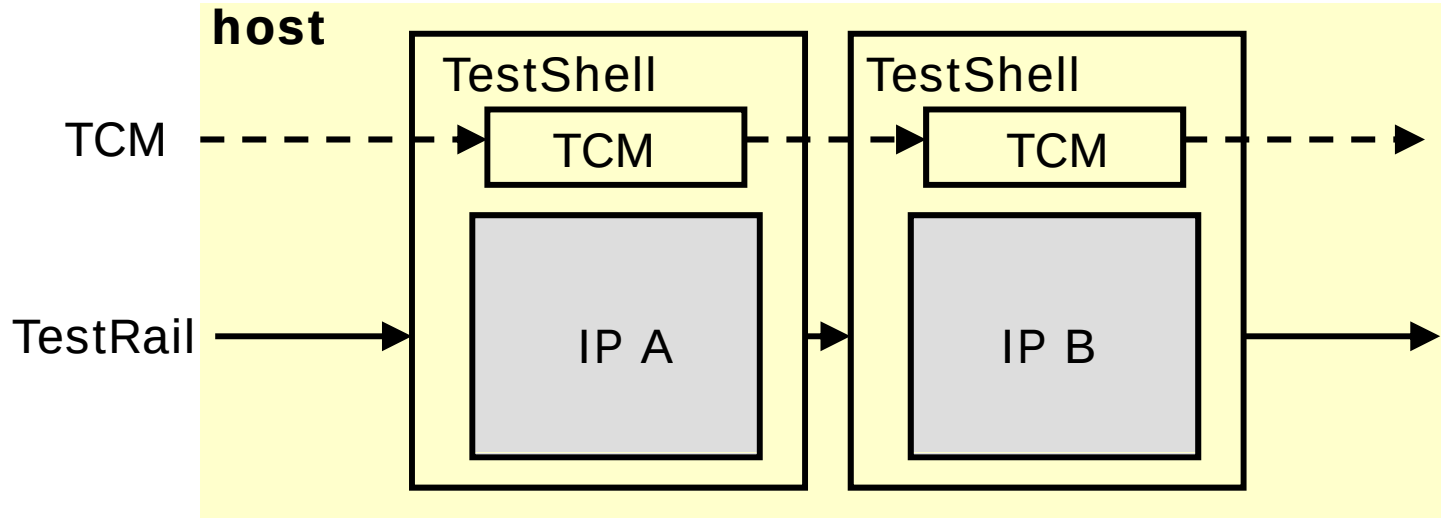
- (a): Multiplexing architecture; (b) daisy-chain architecture; (c) Distributed architecture



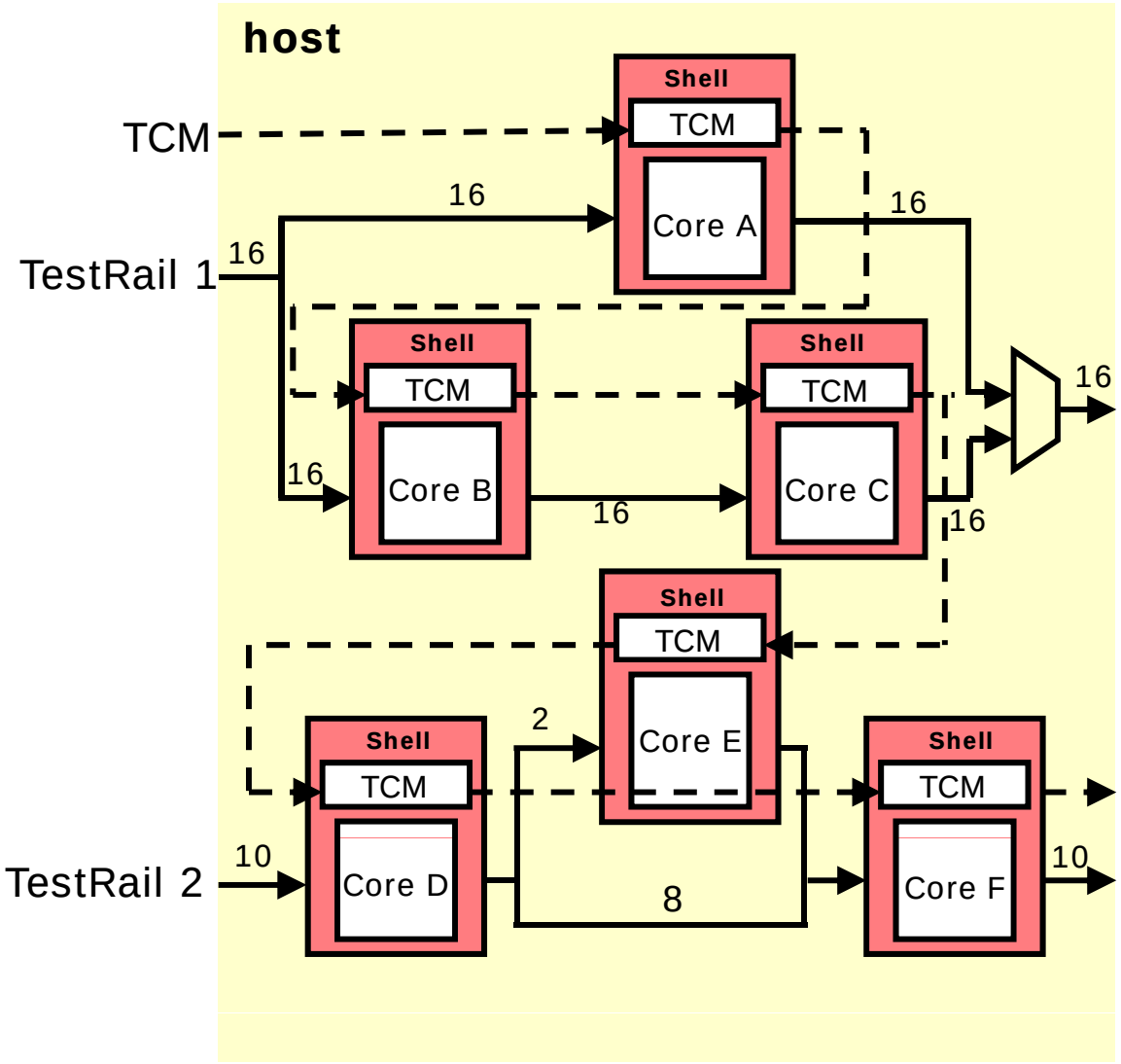
(a) (b) (c)

Test Shell / TestRail [E. J. Marinissen, ITC98]

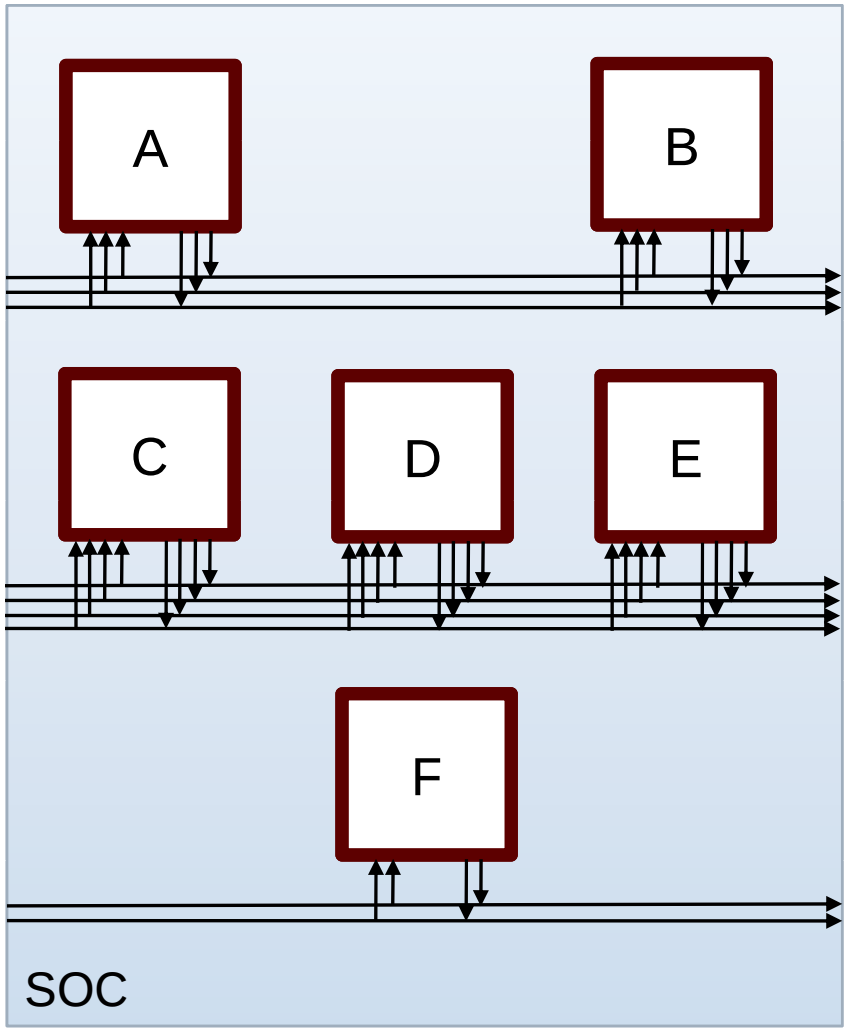
- Every core is wrapped with a TestShell
- The TestShell is the test data transport mechanism
- TCM is a standardized test control mechanism in the TestShell
- The host is the environment in which the core is embedded



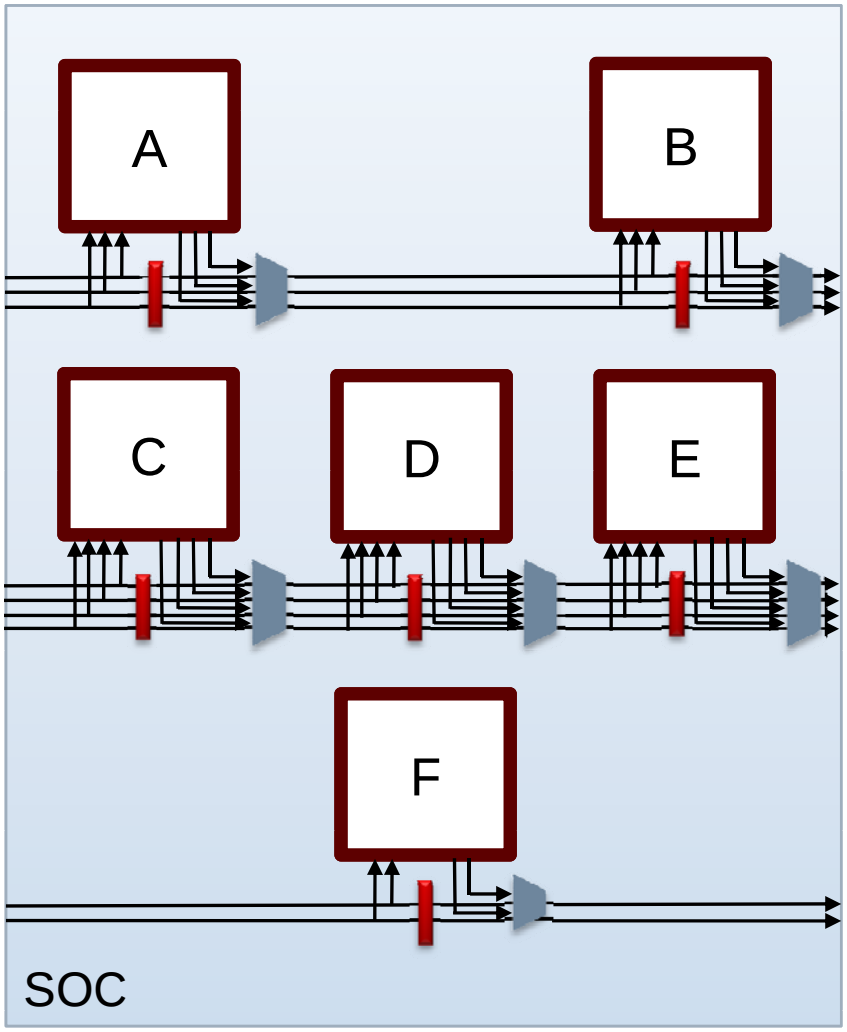
Test Shell / TestRail [E. J. Marinissen, ITC98]



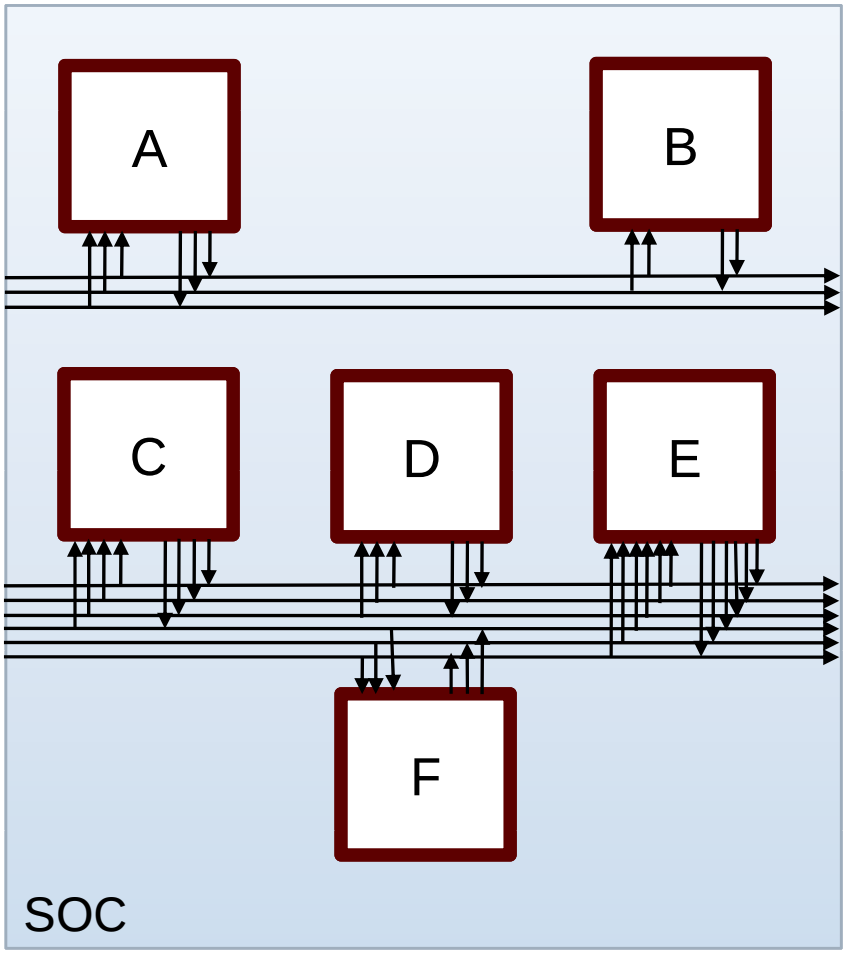
Fixed-Width Test Bus Architecture



Fixed-Width TestRail Architecture

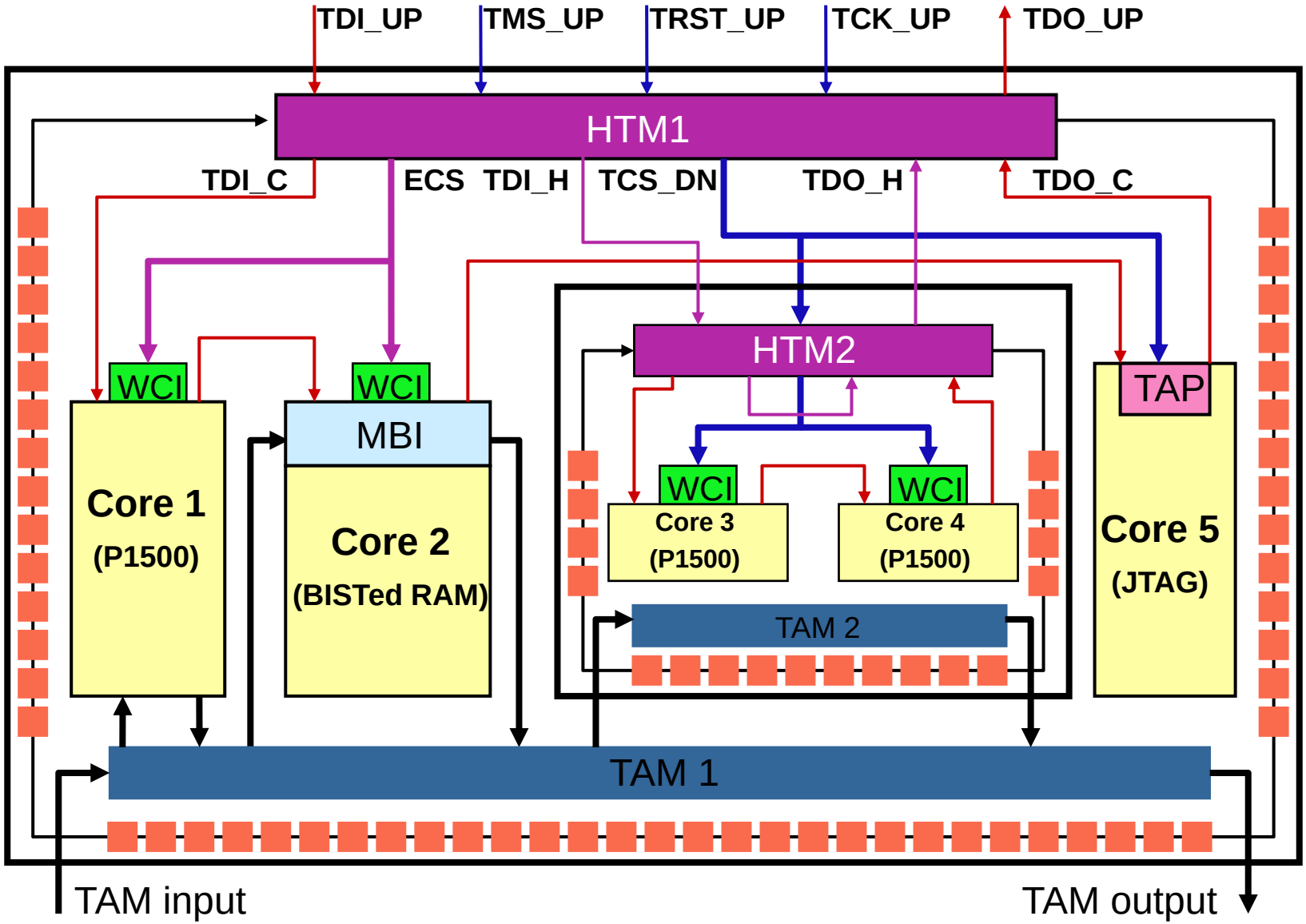


Flexible-Width Test Bus Architecture



Hierarchical Test Methodology

[J.-F. Li, et al., IEEE Micro 02]

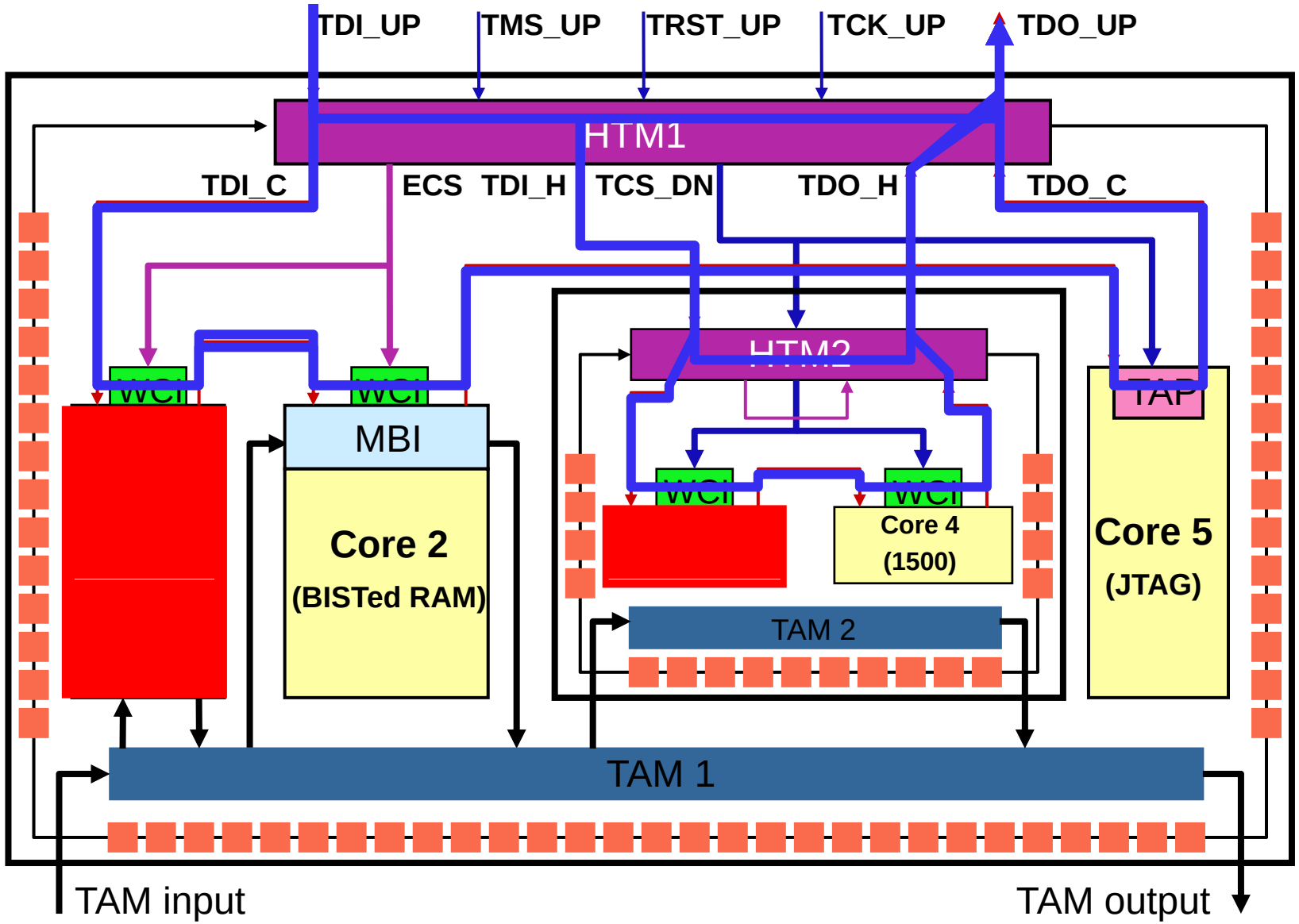


Hierarchical Test Procedure

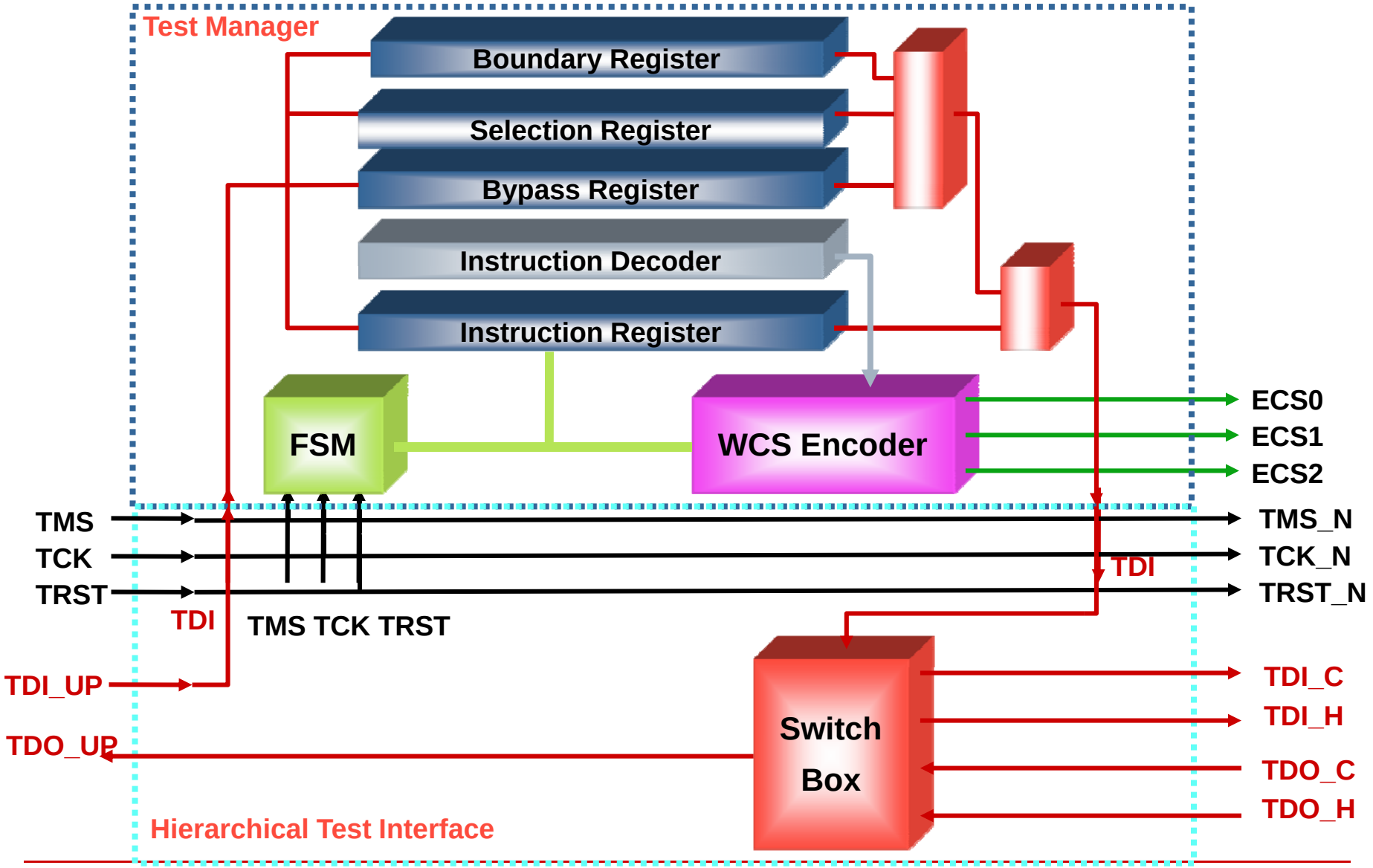
[J.-F. Li, et al., IEEE Micro 02]

- Test Configuration
  - Load the instructions for the wrappers and memory BIST interfaces (MBIs)
- TAM Specification
  - Specify the cores to be tested by the TAM
- Test Transportation
  - Import the test patterns and export the test responses

An Example

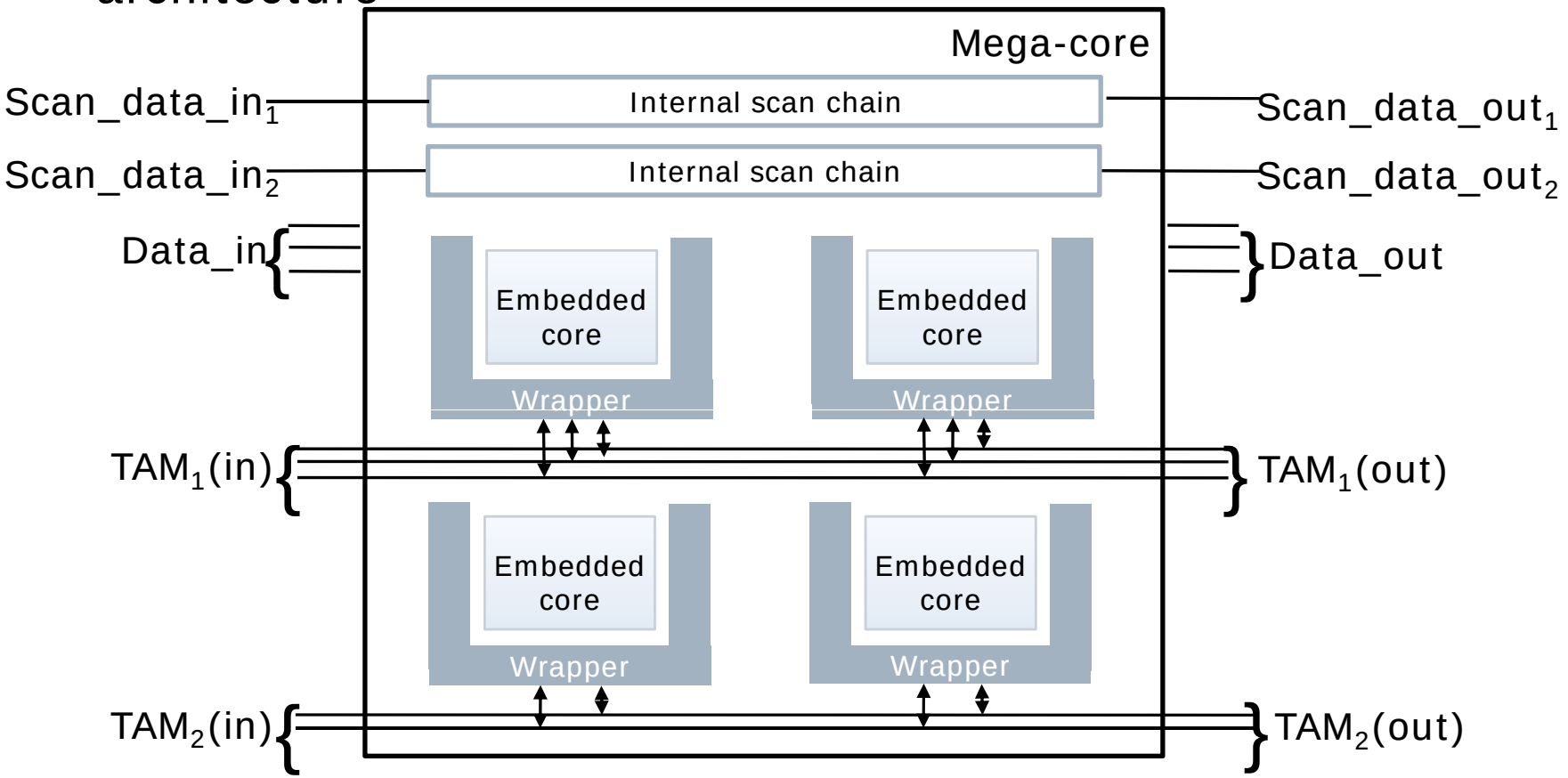

TDI_UP
TMS_UP
TRST_UP
TCK_UP
TDO_UP
HTM1
TDI_C
ECS
TDI_H
TCS_DN
TDO_H
TDO_C
WCI
WCI
MBI
Core 2
(BISTed RAM)
HTM2
WCI
WCI
Core 4
(1500)
TAP
Core 5
(JTAG)
TAM 2
TAM 1
TAM input
TAM output

Hierarchical Test Manager



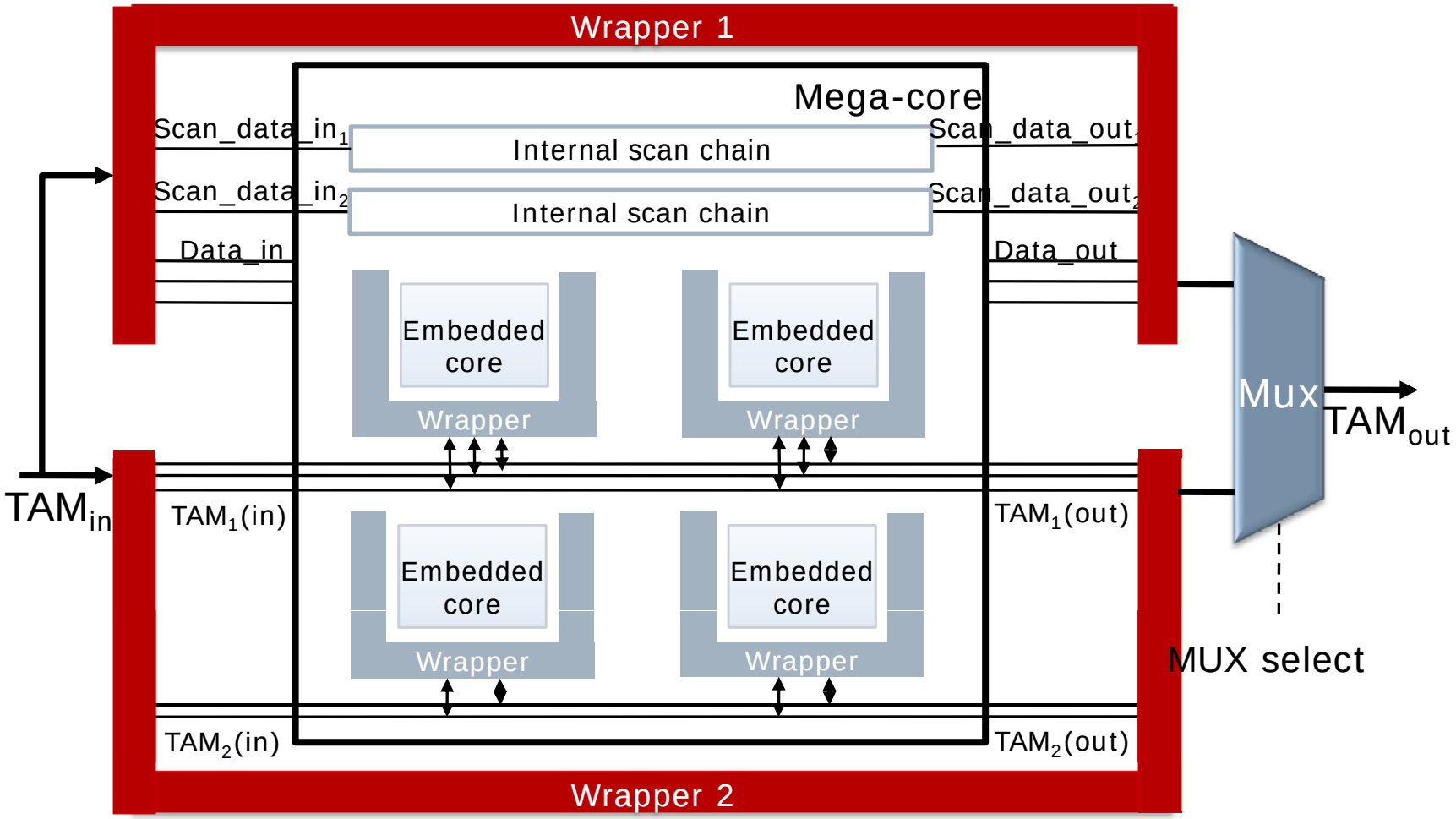
Example 1

- A megacore is defined as a design contains nonmergeable embedded cores
- An illustration of a megacore with a predesigned TAM architecture



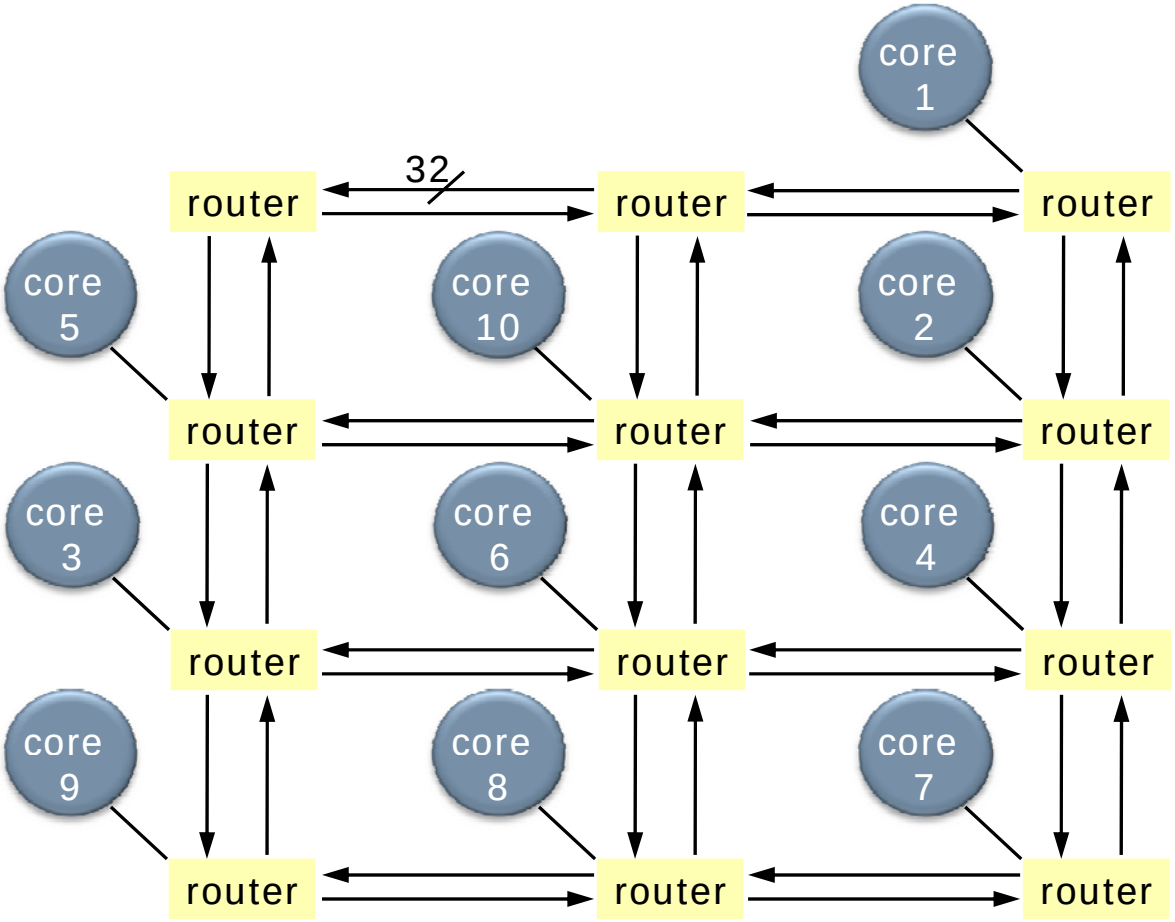
Example 2

- An illustration of a two-part wrapper for the megacore that is used to drive the TAMs in the megacore and to test the logic external to the embedded cores



Network-on-Chip (NoC)

- An example of a mesh-based network-on-chip

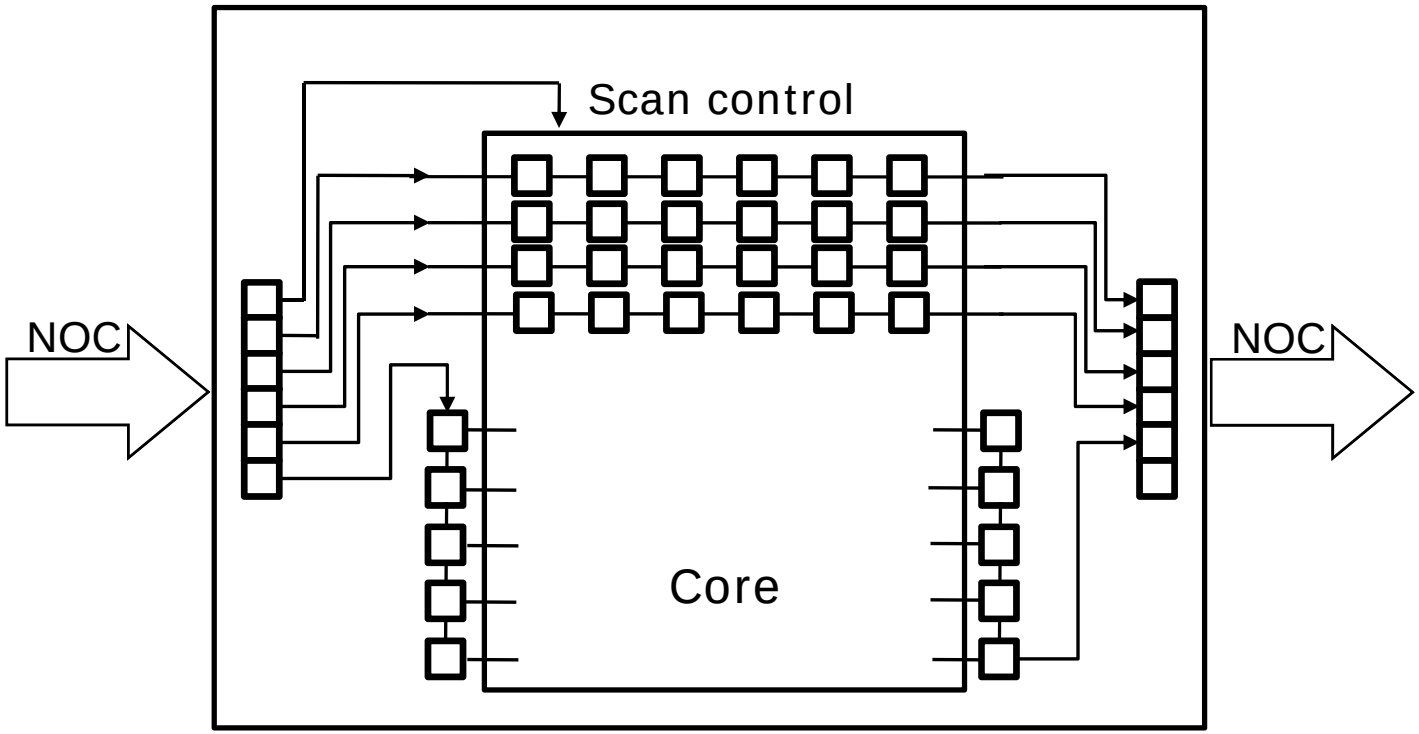


Network-on-Chip Testing

- Testing an NoC-based system includes testing of embedded cores and testing of the on-chip network
- Testing of embedded cores is similar to conventional SOC testing
- Testing of on-chip network
  - Testing of interconnects, switches/routers, input/output ports, and other mechanism other than the cores

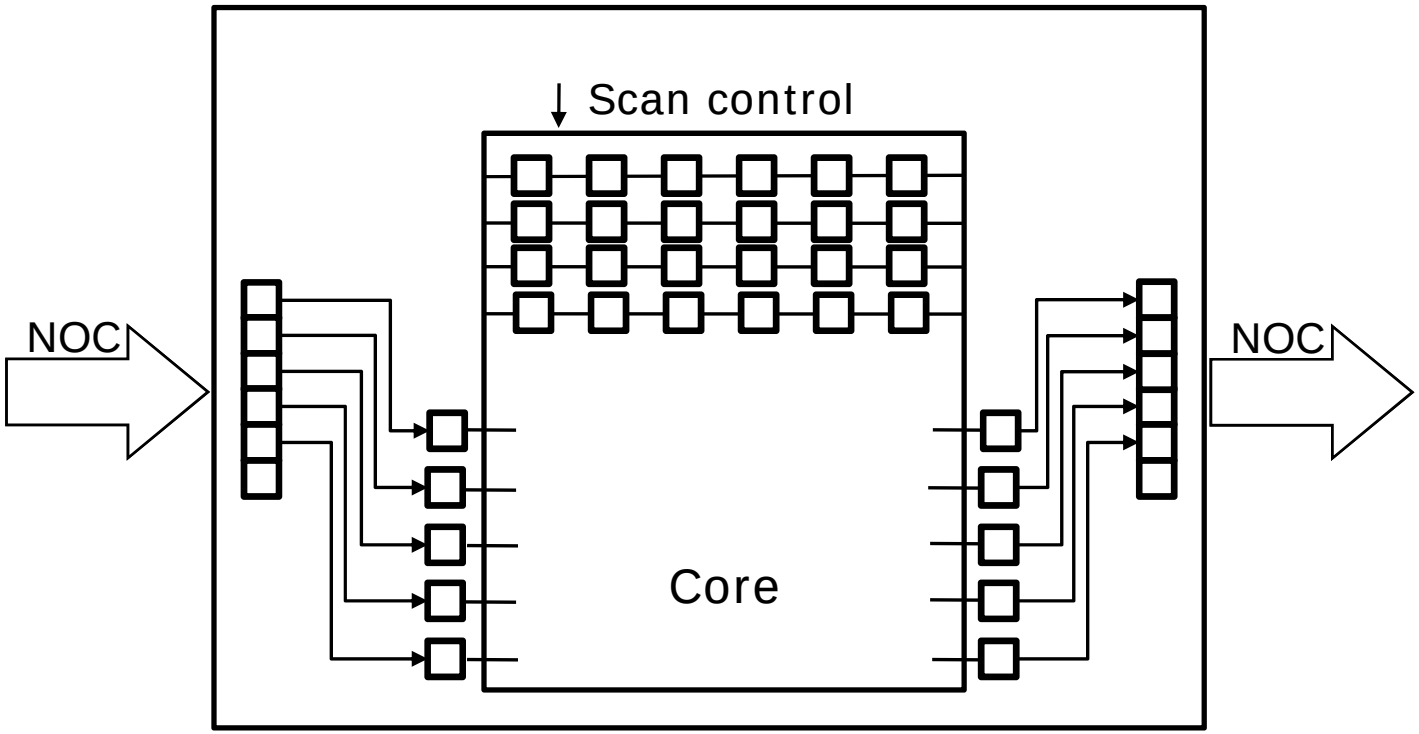
Reuse of On-Chip Network for Testing

- Wrapper configurations of cores in NoC-based system in test mode

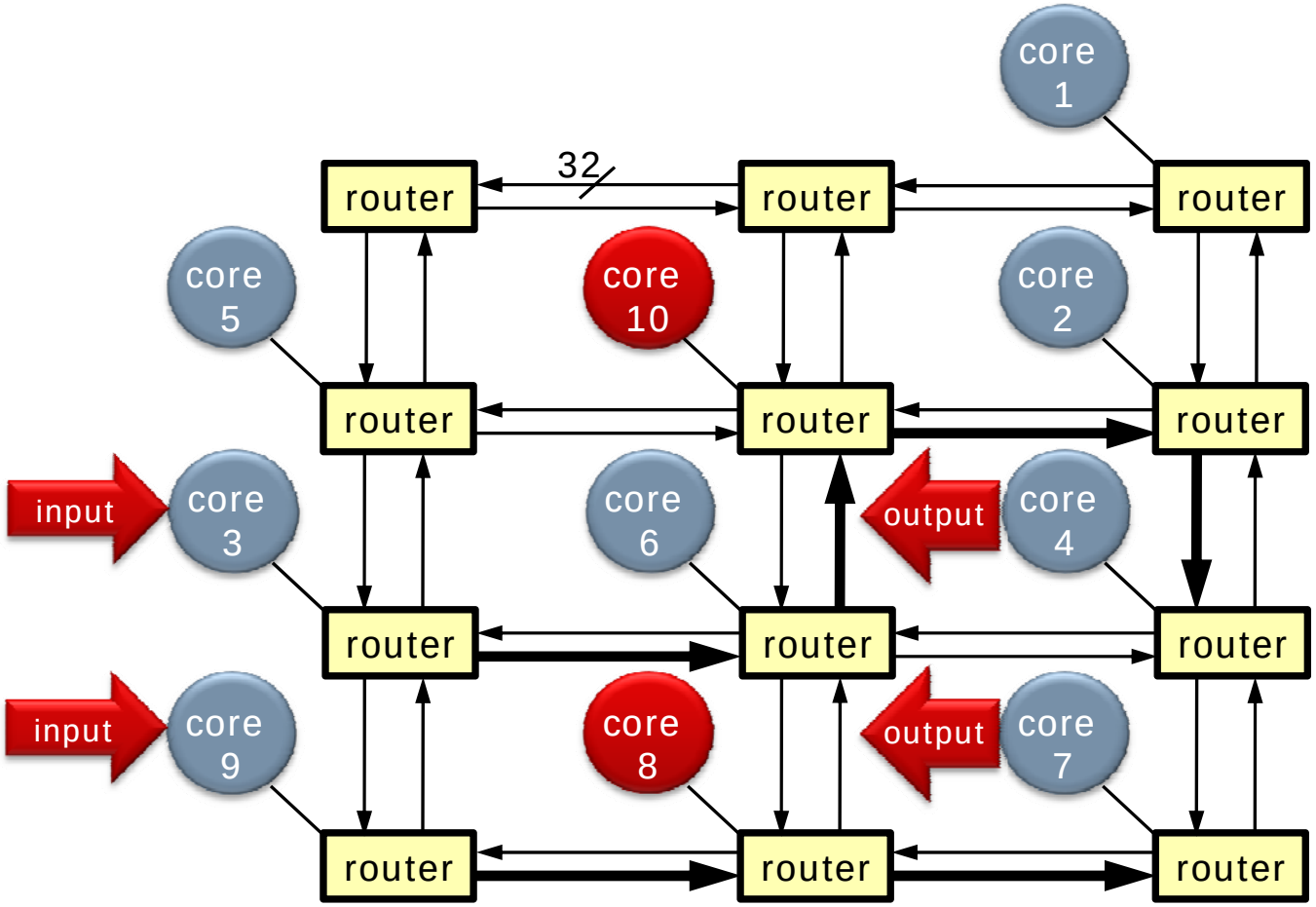


Reuse of On-Chip Network for Testing

- Wrapper configurations of cores in NoC-based system in function mode

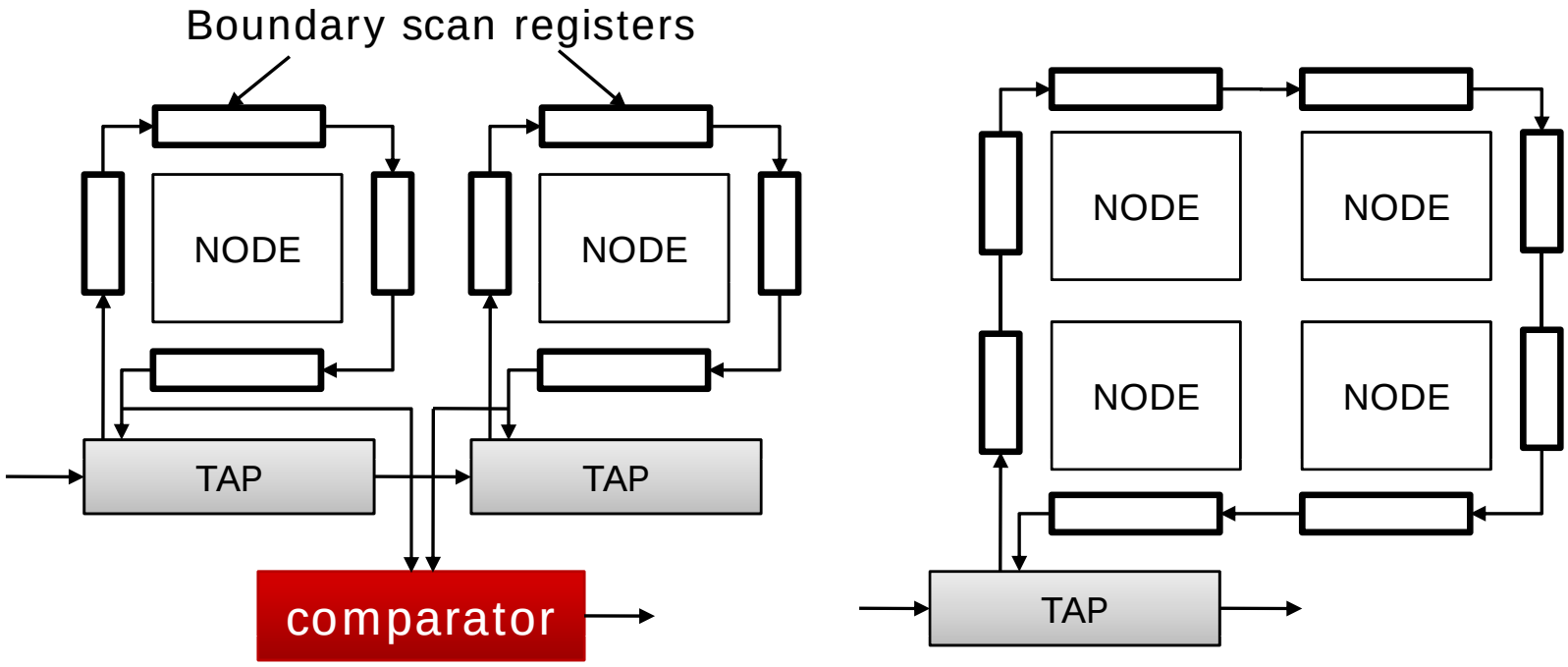


Test Ports and Routing Paths



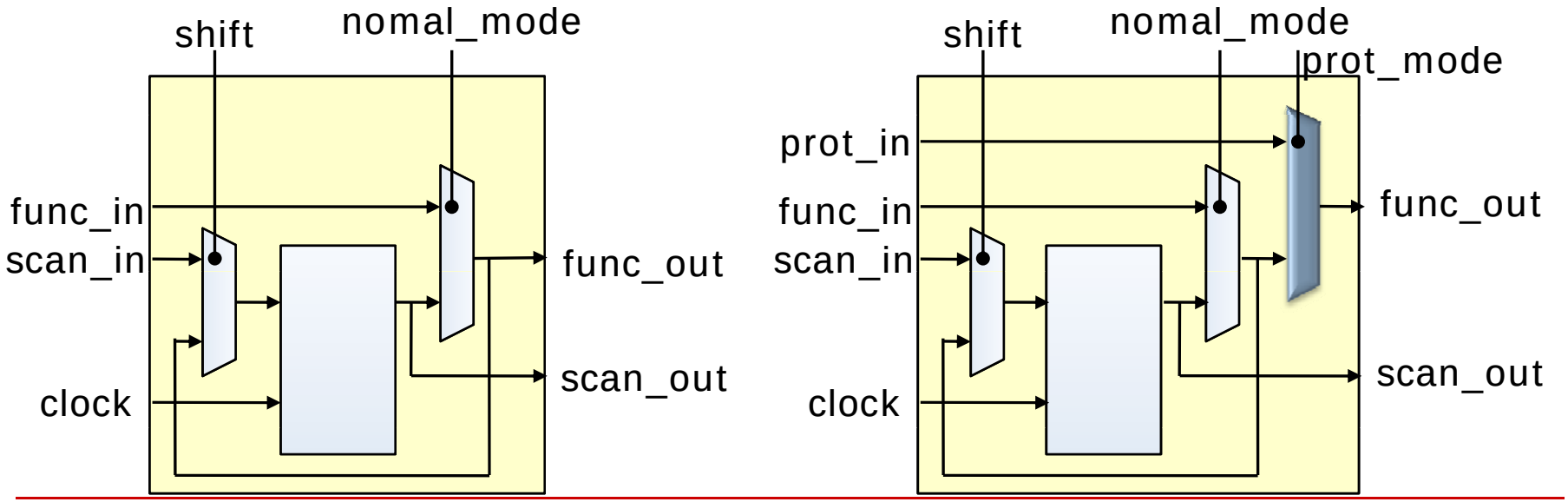
Test Access Methods

- An example of testing of identical cores using IEEE 1149.1



Test Interface

- To reuse the network to transport test data, a test interface has to be established to handle both functional protocol from network and test application to the core
- A wrapper is needed for each core as an interface
  - Left figure shows a standard IEEE1500 wrapper cell
  - Right figure shows a modified wrapper cell for NoC testing

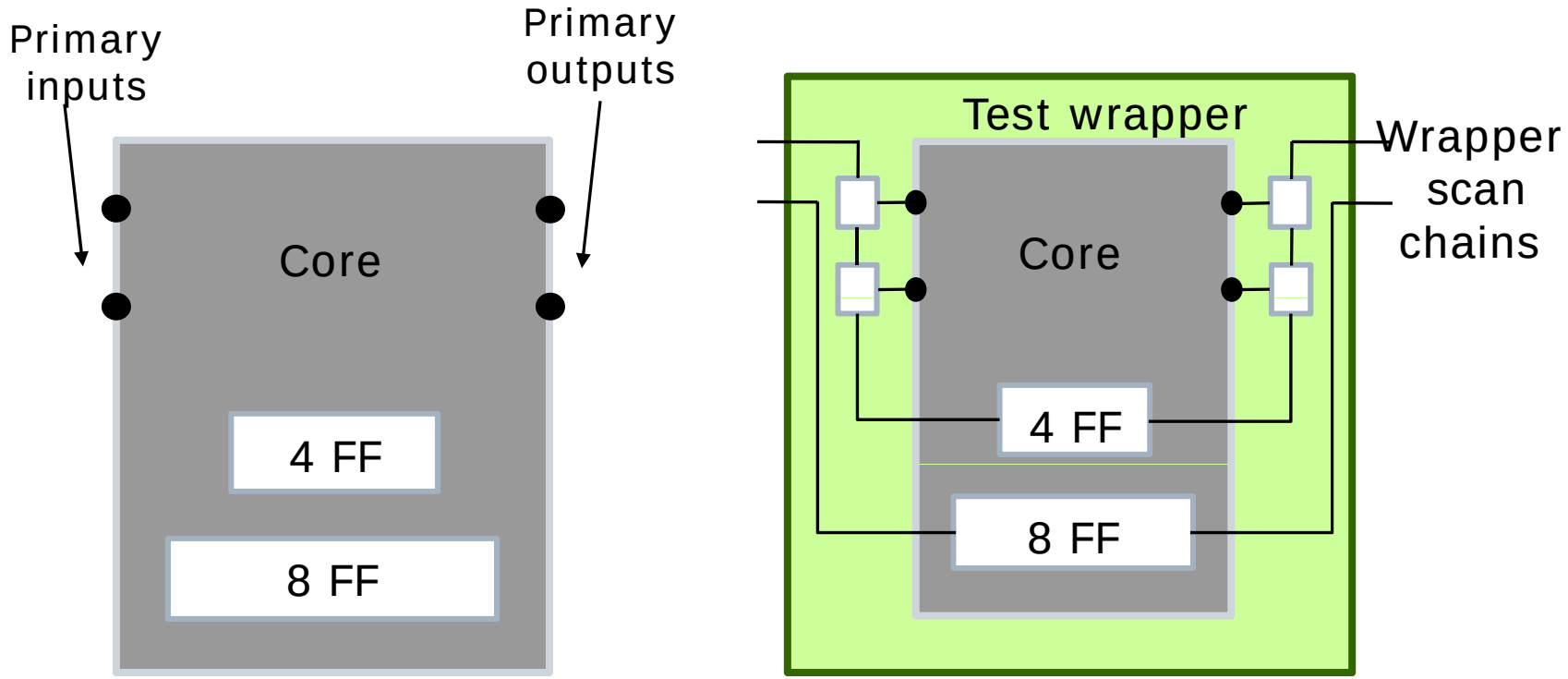


Efficient Reuse of Network

- One challenge in this reuse-based approach is that the channel width is determined by the system performance in design process and hence cannot be optimized for test purpose
- In the context of network reuse in NoC test, the available TAM or channel width for wrapper scan chain design is already determined by the bandwidth requirements of cores in mission mode, not for test mode
- For example, if the channel width is predesigned to be 4, then half of the channel wires will be idle during core test while the core under test only has two scan chains

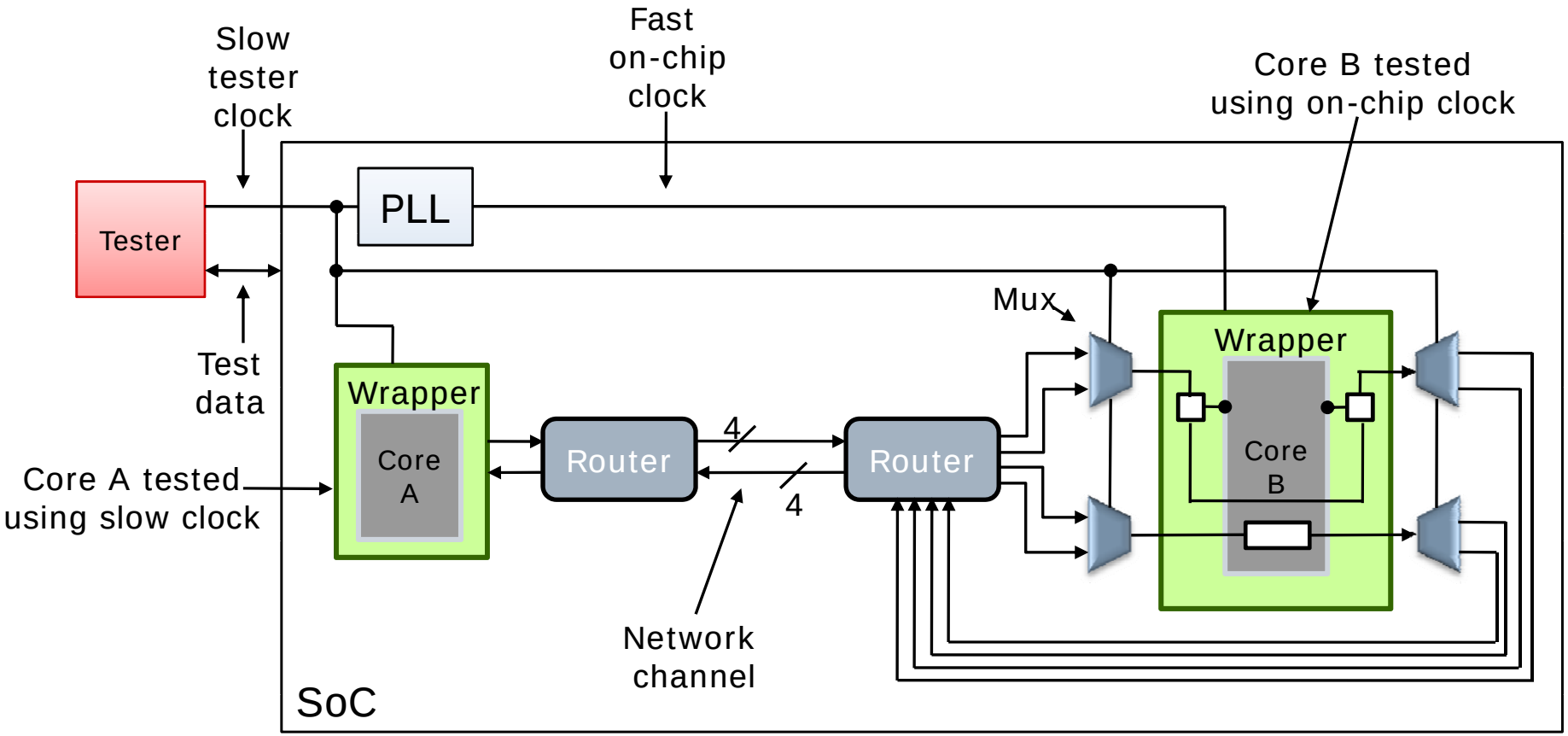
Wrapper Scan Chains

- Core test wrapper is usually designed through the use of balanced wrapper scan chains
  - Left figure is an example of unwrapped core
  - Right figure is an example of balanced wrapper scan chain design



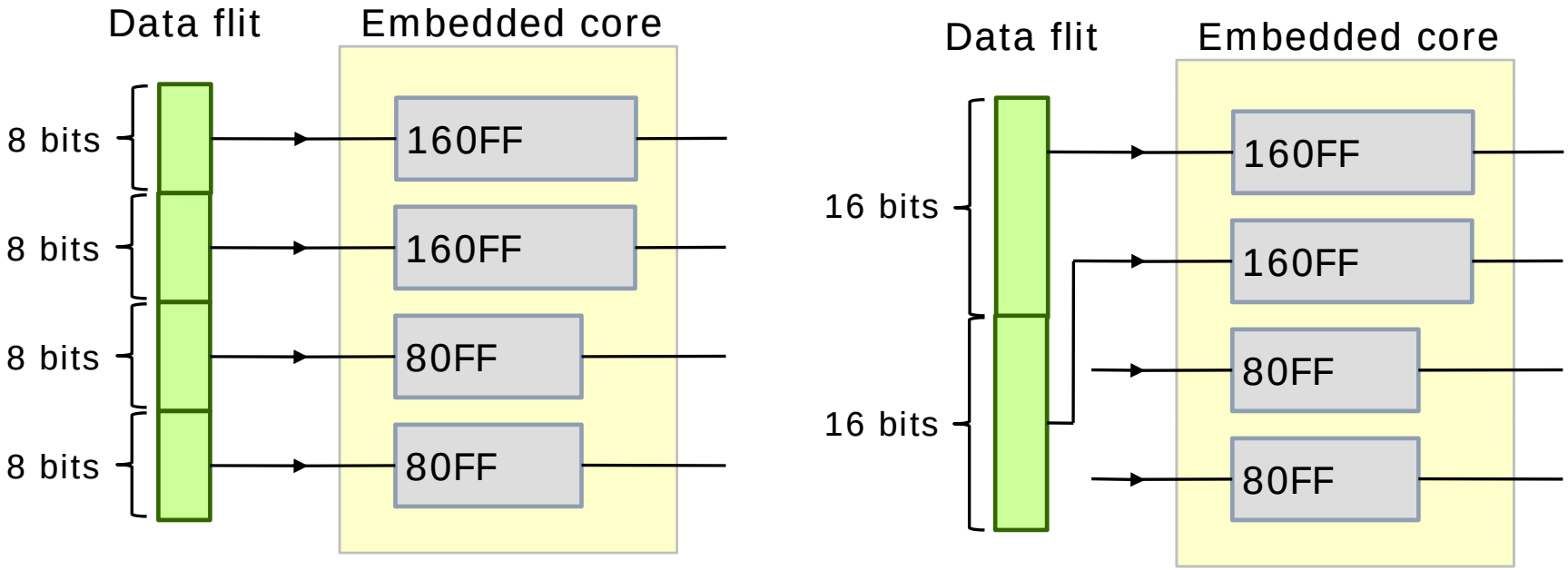
Utilization of the Reused Channel

- Time-multiplexing technique can be used to increase the utilization of test channel
- E.g., test architecture using on-chip clocking



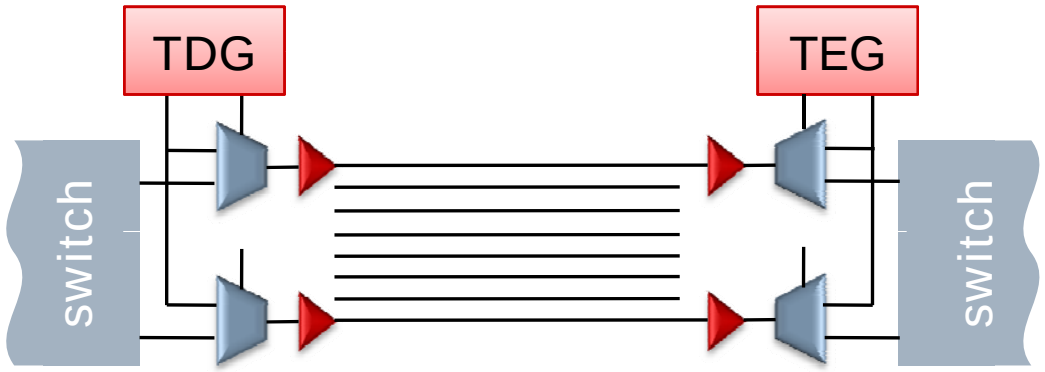
Reconfigurable Data Flit Format

- Another technique can be used to increase the utilization of the reused channel
  - Reconfigurable data flit
- Example:

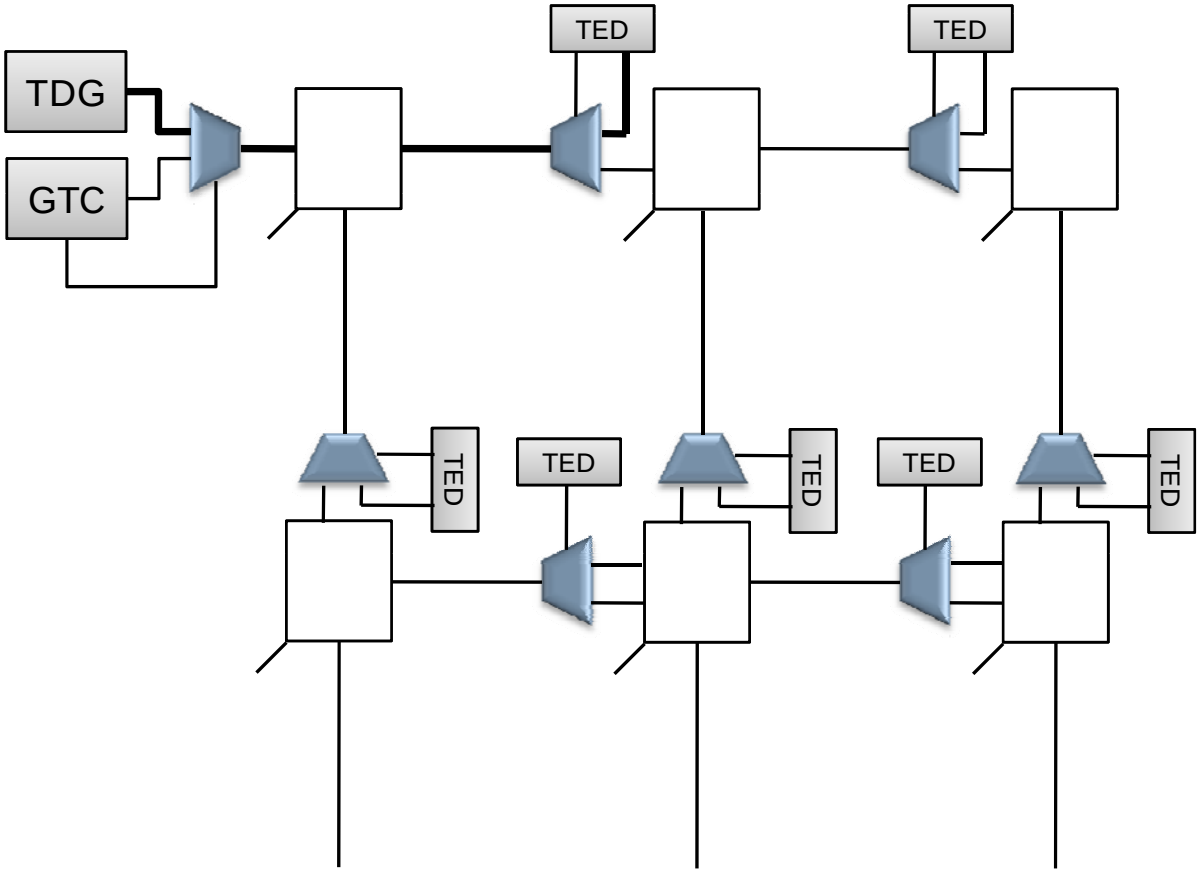


Testing of On-Chip Networks

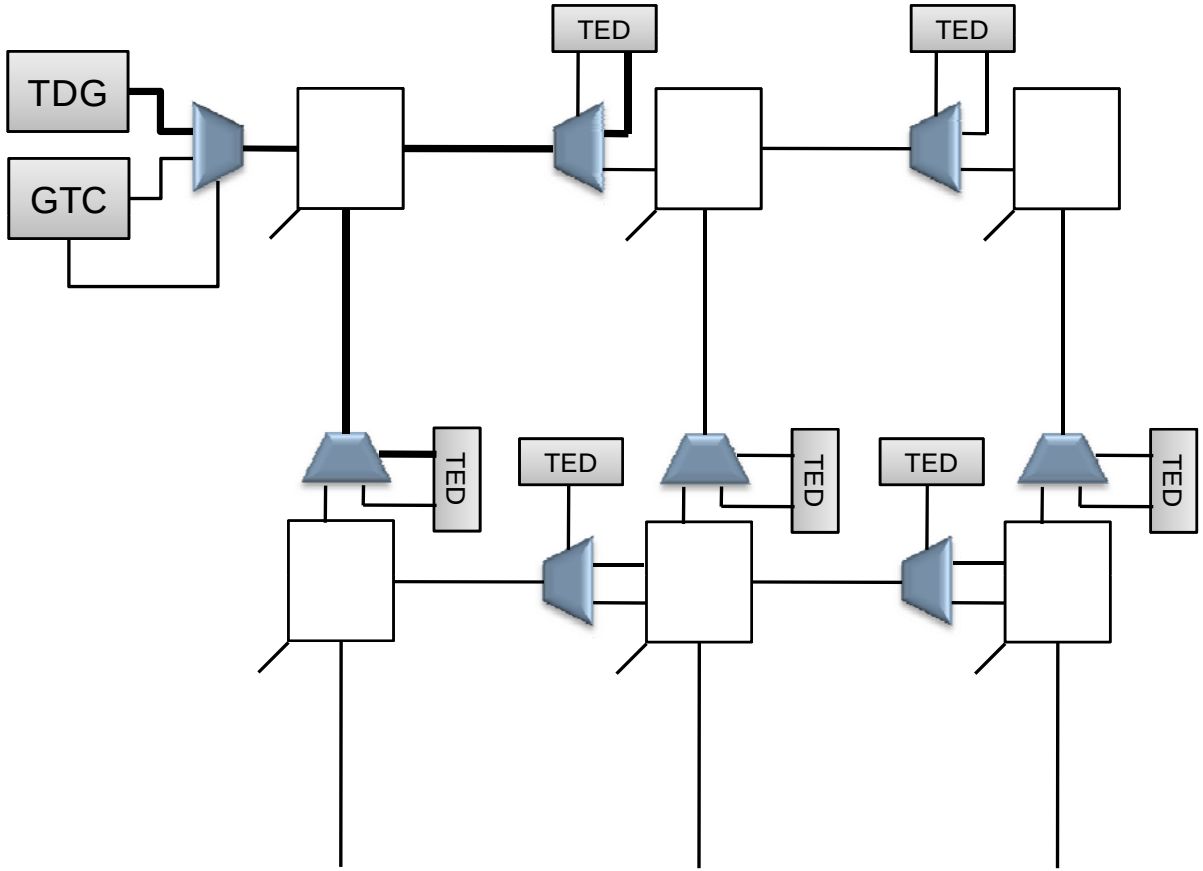
- Testing of on-chip networks
  - Testing of interconnects and routers
- Testing of interconnects
  - Maximal aggressor fault (MAF) model is typically used for testing of on-chip interconnects
- An example of BIST for interconnect testing



Interleaved Unicast MAF Test

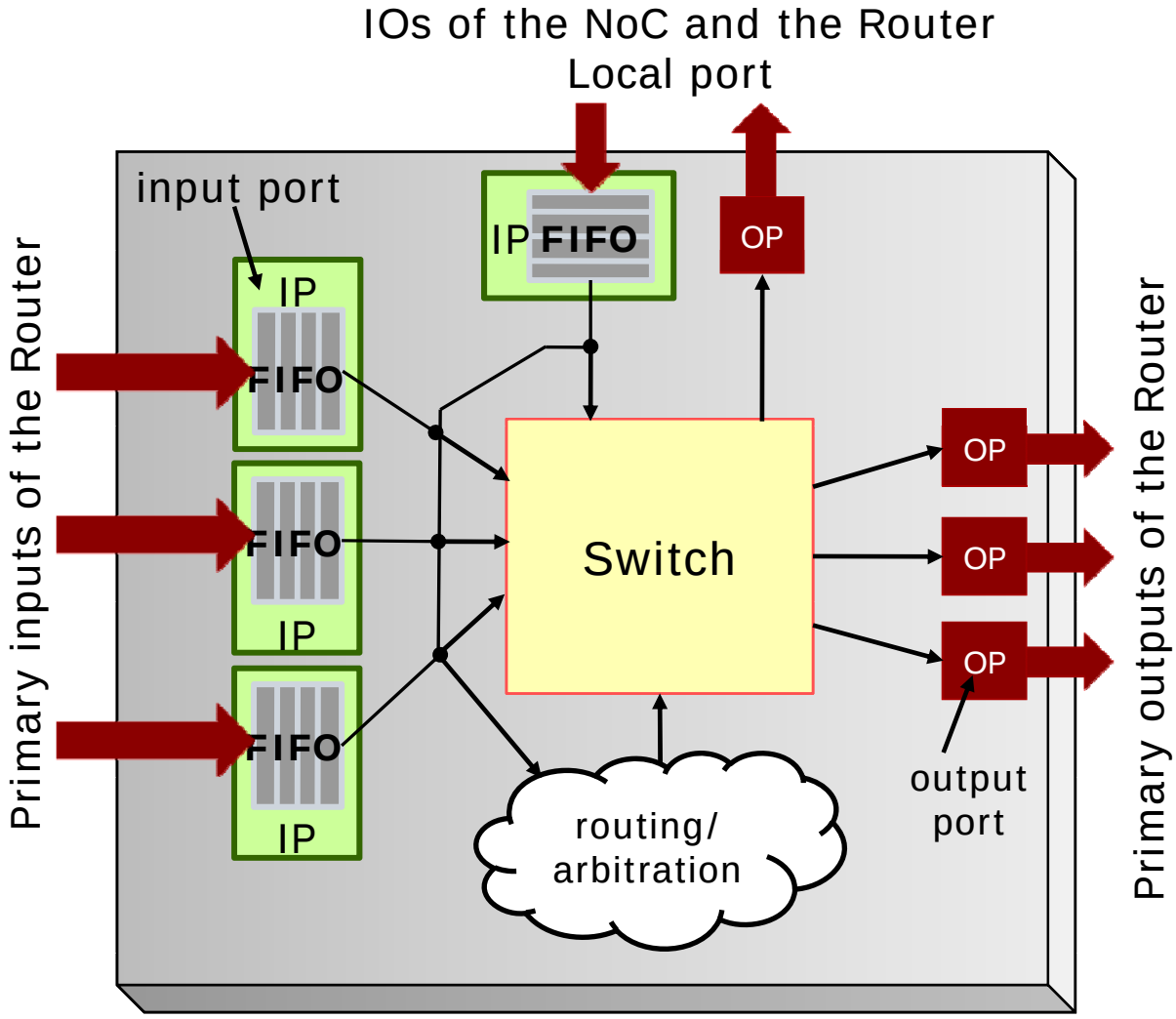


Interleaved Multicast MAF Test



Routers

- A typical organization of a router

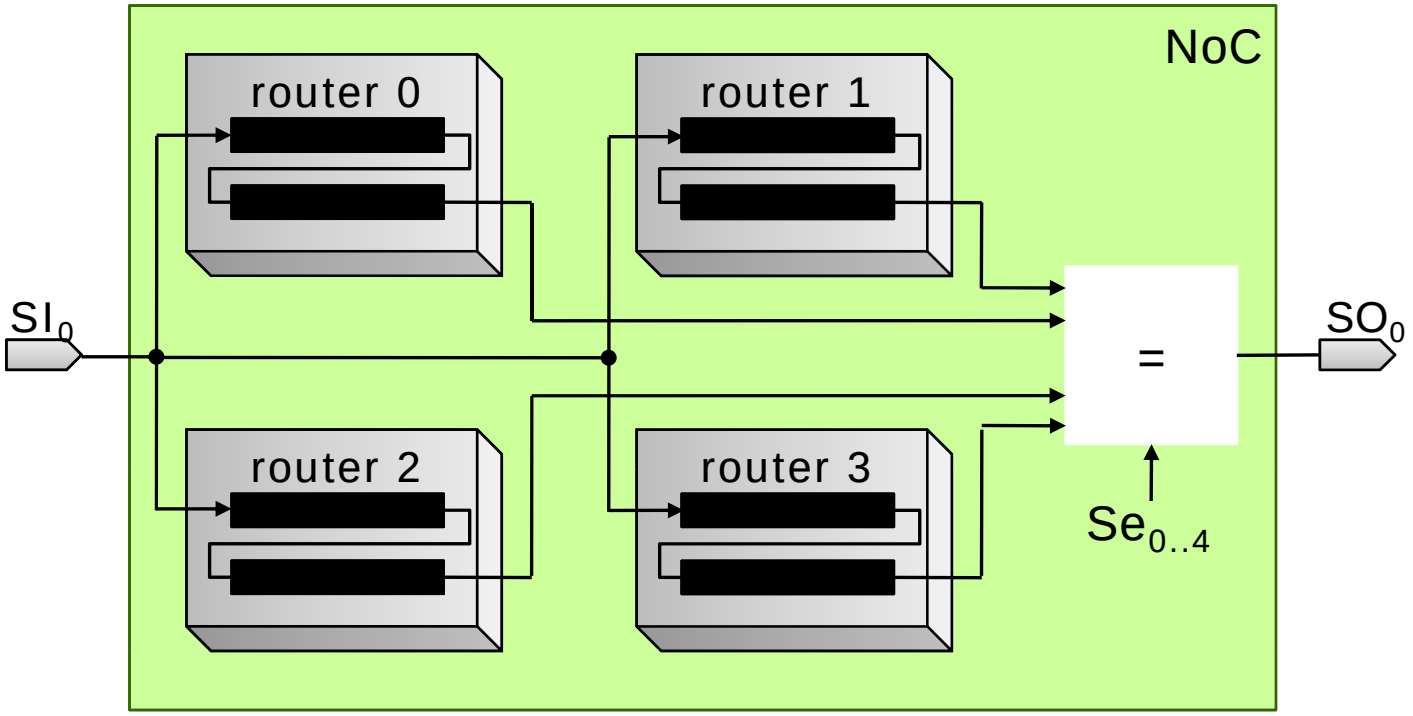


Testing of Routers

- Router testing has been dealt with in three parts
  - The testing of each router
  - The testing of all routers (without considering network interfaces and interconnects)
  - The testing of wrapper design
- Testing a router
  - Testing the control logic (routing, arbitration, and flow control modules)
  - Testing the FIFOs
- Testing the control logic can be done using traditional sequential circuit testing methods
- One approach to test FIFO
  - Configure the first register of the FIFO as part of a scan chain, and other registers can be tested through this scan chain

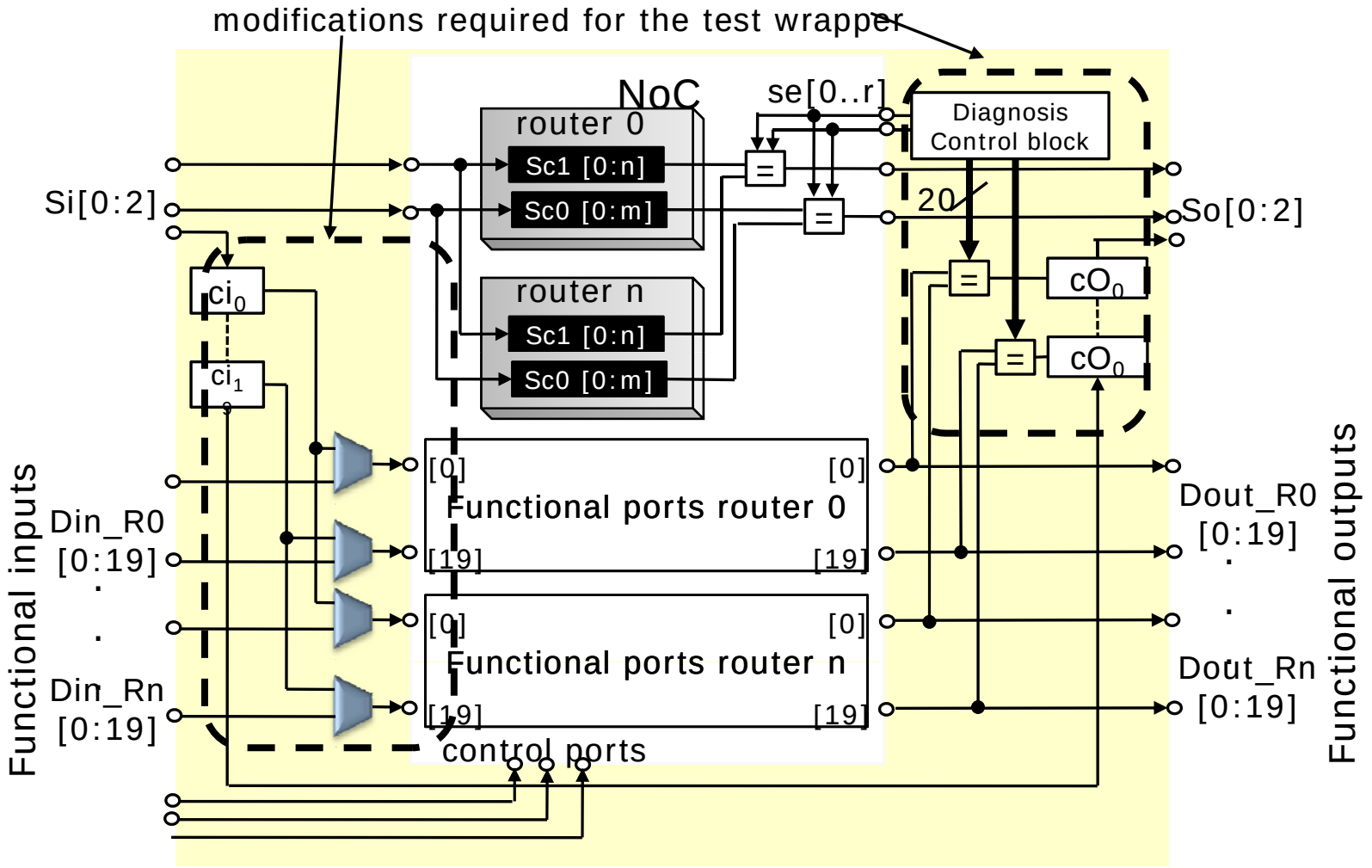
Testing multiple identical Routers

- The FIFOs in a router is configured as a scan chain
  - Multiple routers can be tested in parallel



Test Wrapper Design for Routers

- An IEEE-1500 compliant test wrapper should be designed to support test pattern broadcasting and test response comparison

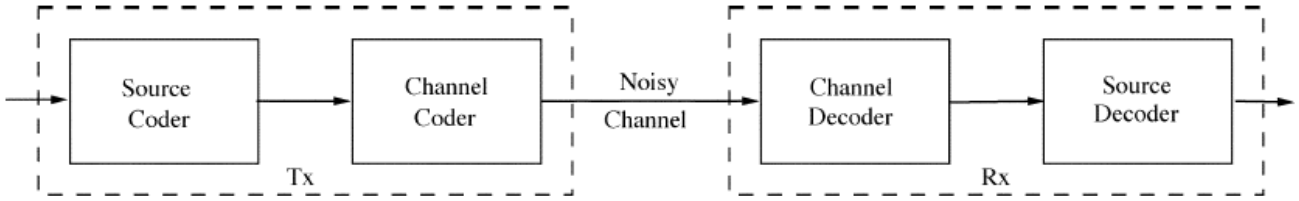


special in test wrapper

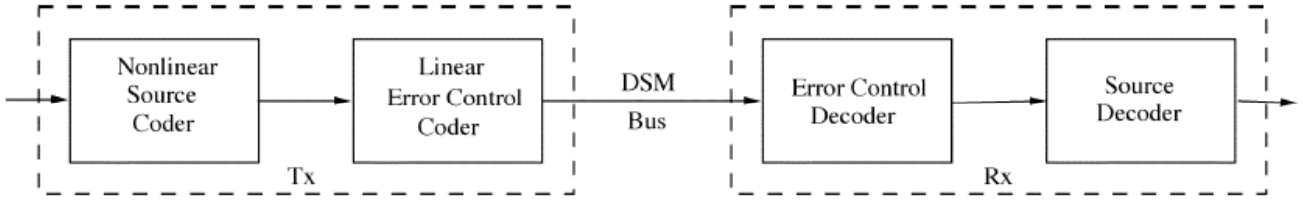
Design of Reliable On-Chip Networks

[Source: pp. 655-667, June, 2005, TVLSI]

- Generic communication system



- Generic coding system for an on-chip bus



Design of Reliable On-Chip Networks

[Source: pp. 655-667, June, 2005, TVLSI]

- An unified coding framework for on-chip networks