System-in-Package (SiP) Testing

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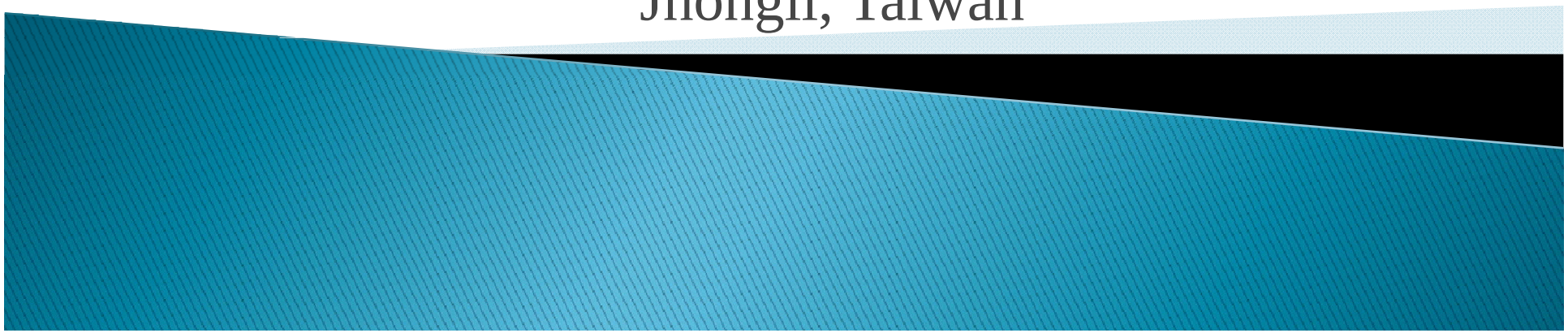
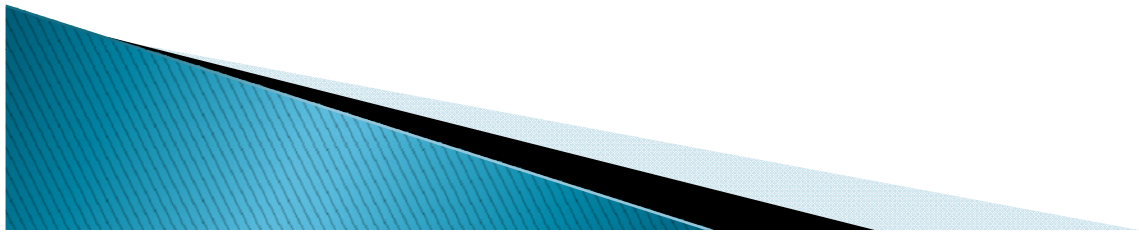
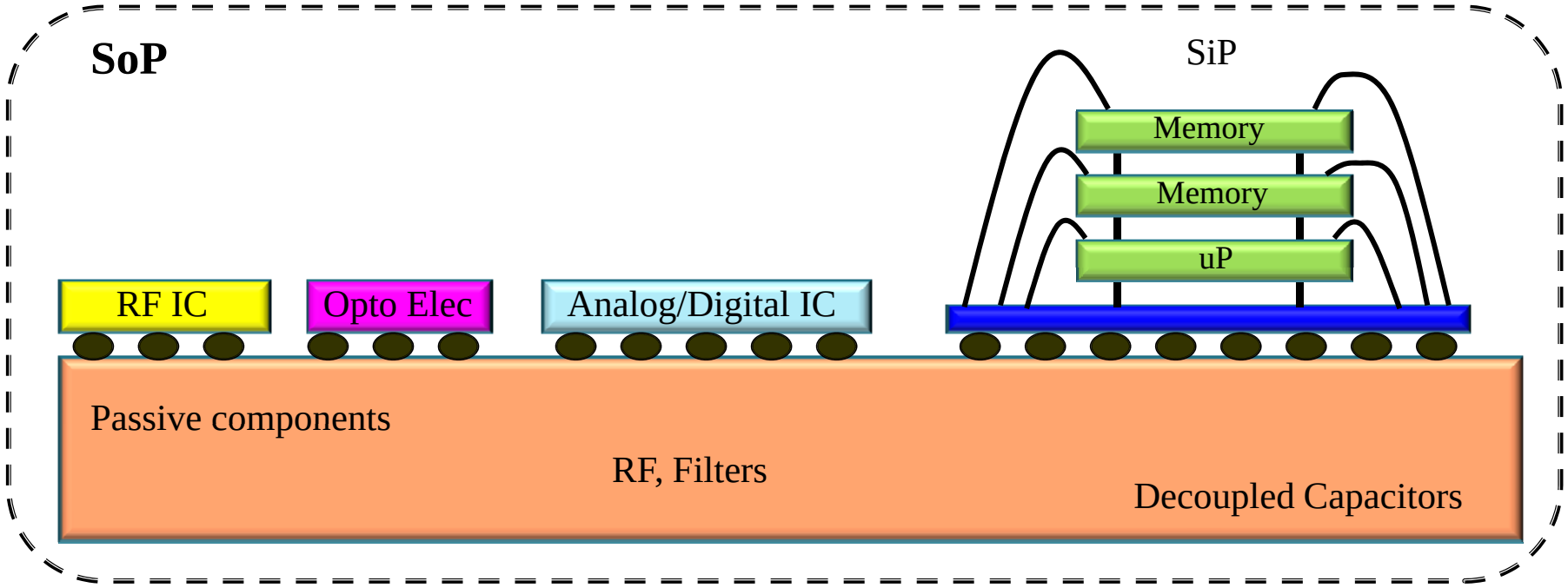


Outline

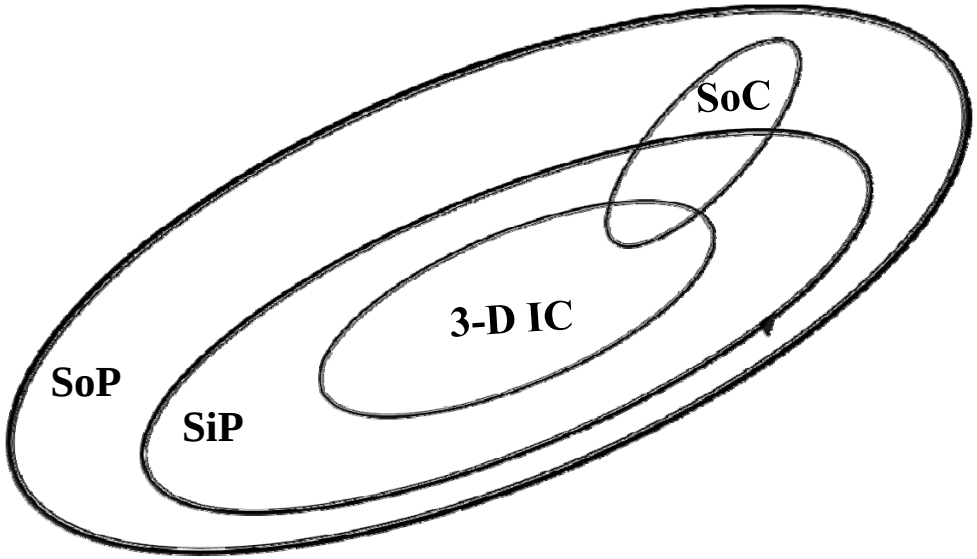
- Introduction
- System-on-Chip (SoC), Multichip Module(MCM), and System-in-Package (SiP)
- Testing of Bare Dies
- System-in-Package Testing



System-on-Package



Relation of SoP, SiP, 3-D IC, and SoC

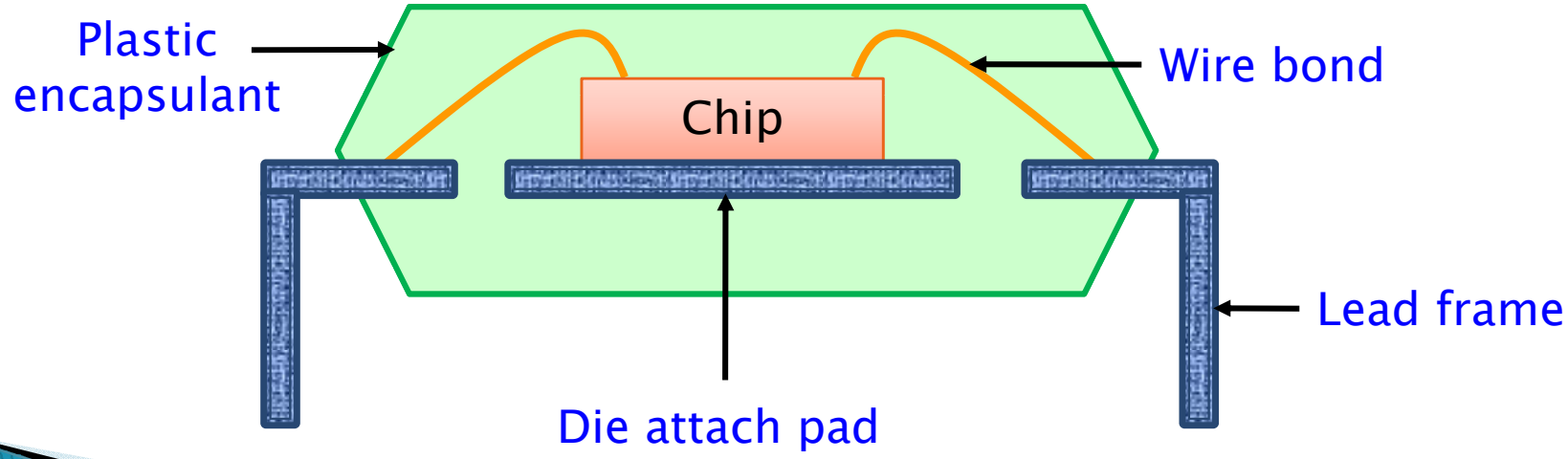


System-in-Package

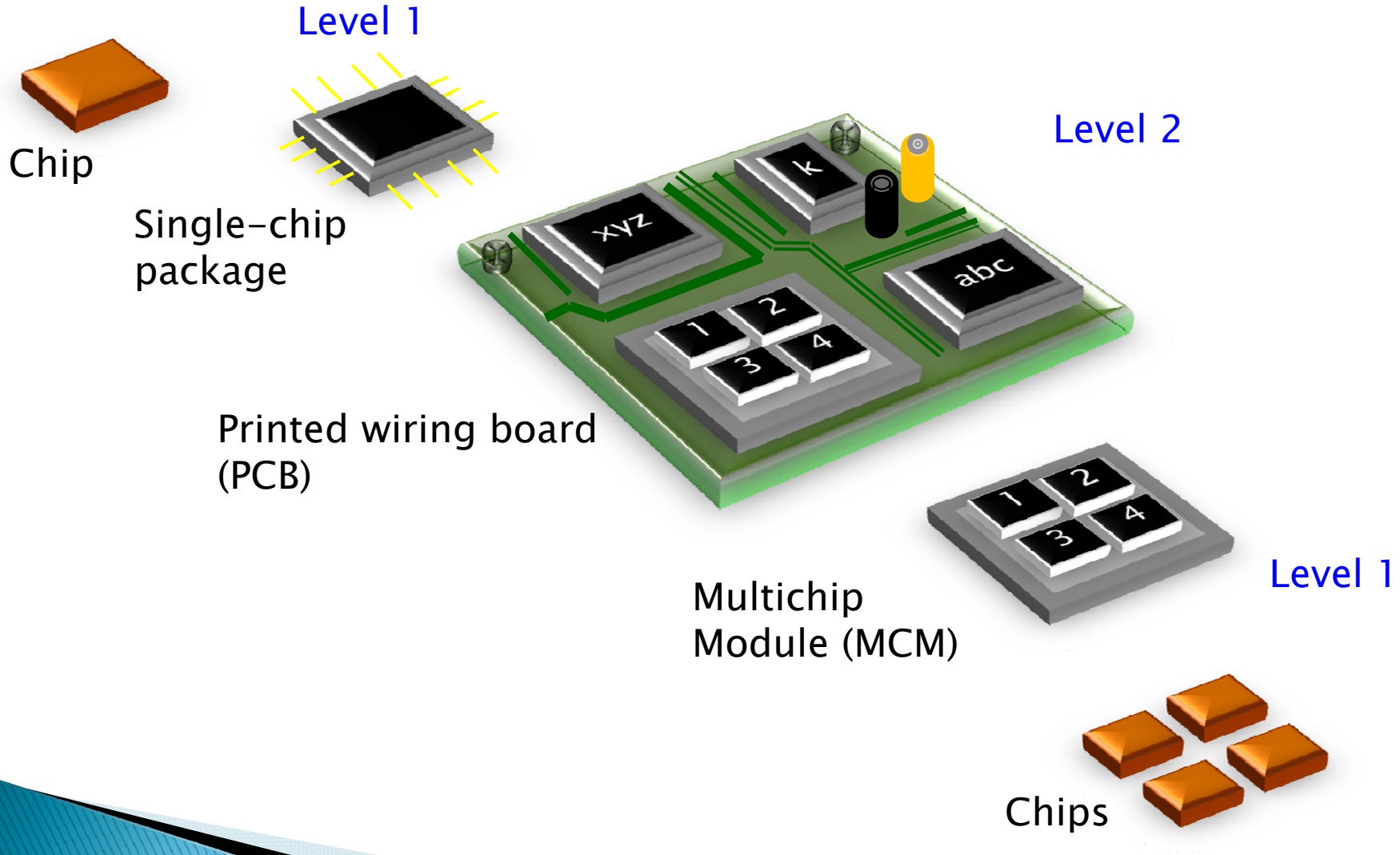
- The system-in-package (SiP) is a single miniaturized functional module realized by vertical stacking of two or more similar or dissimilar bare or packaged chips
- Bringing the chips closer together enables the highest level of silicon integration and are efficiency at the lowest cost, compared to mounting them separately in traditional was
- SiP technology allows the integration of heterogeneous IC technologoies
- Therefore, SiP technology is emerging as a strong contender in a variety of applications that include cell phones, digital camera, PDAs, etc.

Chip Package

- Basic requirements of chip package
  - Signal distribution
  - Heat dissipation
  - Power distribution
  - Circuit support and protection

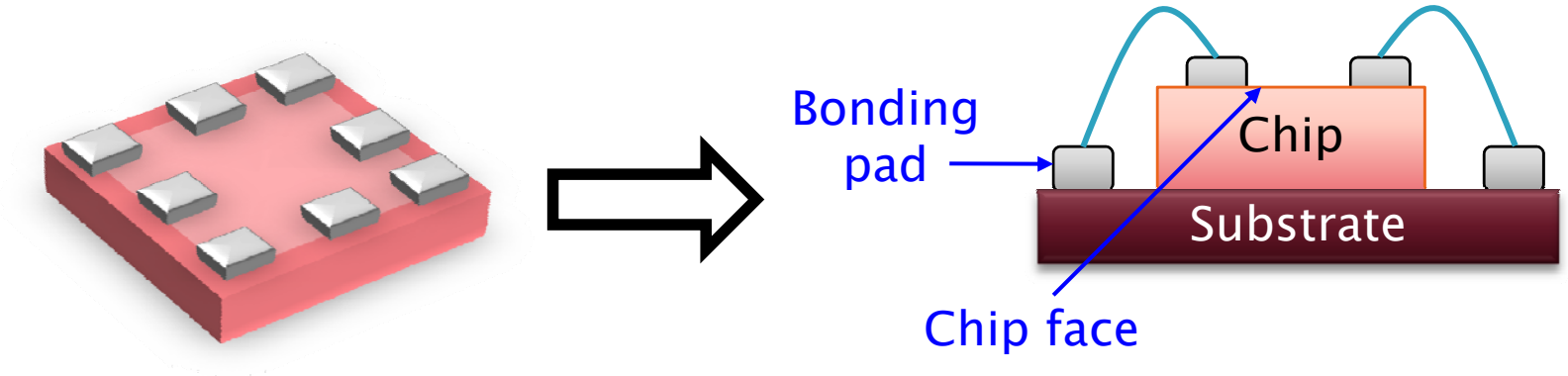


Packaging Hierarchy



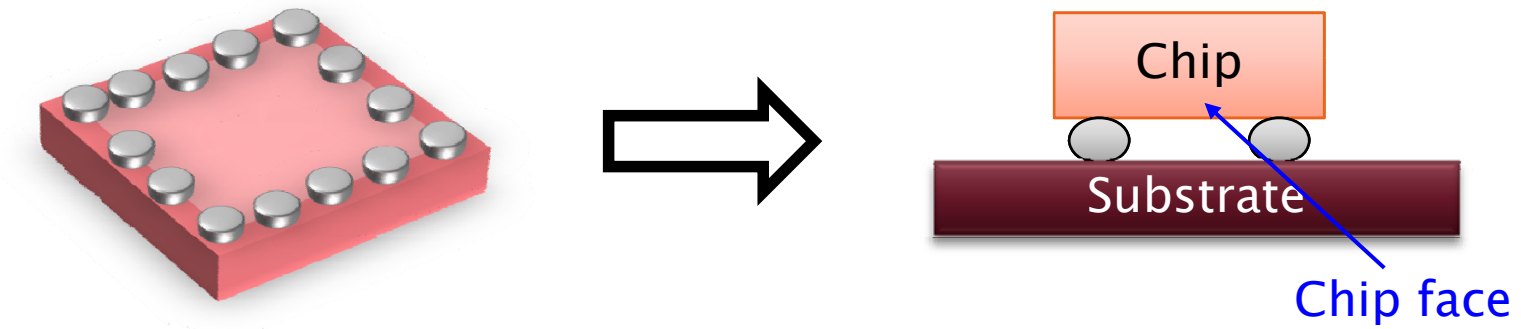
Wire Bonding

- Pitch=75-130 um, Leads=1.5mm
- I/O density=400/cm^2



Flip-Chip Bonding

- The flip chip assembly is much smaller than a traditional carrier-based system
- No leads are needed
- Pitch=75-250 um
- I/O density=1600/cm^2



Flip-Chip Bonding

- Advantages
  - The flip chip assembly is much smaller than a traditional carrier-based system
  - The chip sits directly on the circuit board, and is much smaller than the carrier both in area and height
- Disadvantages
  - Not suitable for easy replacement, or manual installation
  - Require very flat surfaces to mount to
  - Sometimes difficult to maintain as the boards heat and cool

Outline

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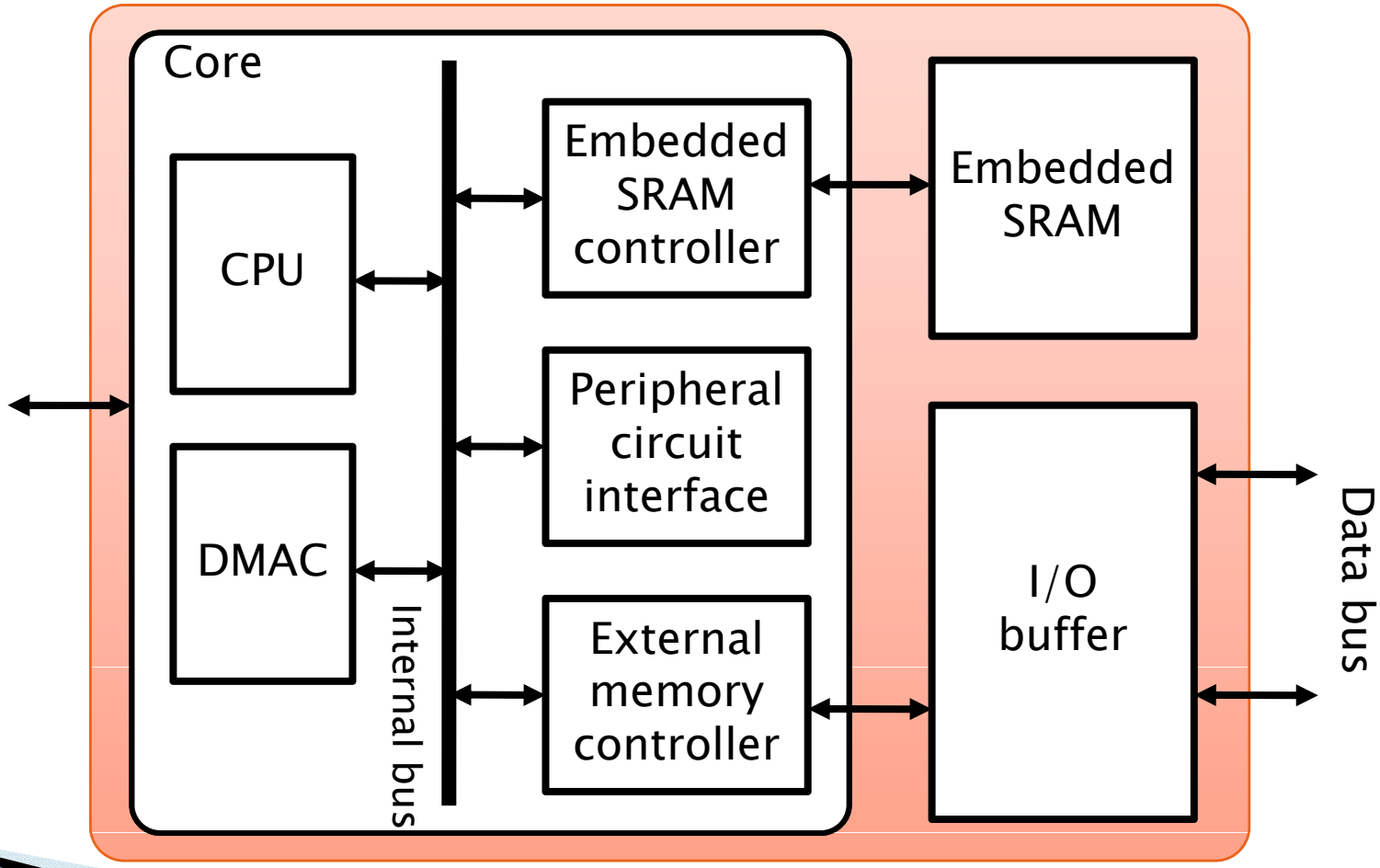
- Interconnection and Package
- System on Chip (SoC), Multichip Module(MCM), and System in Package (SiP)
- Bare Dies Testing
- System in Package Testing

SOC, MCM, and SIP

- Mainframe computers drove MCMs in 1980s
- High-end networking, signal processing, and digital communication demands drive SoC
- Cell phones and handsets are driving SiPs solutions
- Some view SiP as a vertical MCM
- SoC: a packaged chip with only one die
- SiP: an assembled system composed of a number of individual dies on a packaged chip

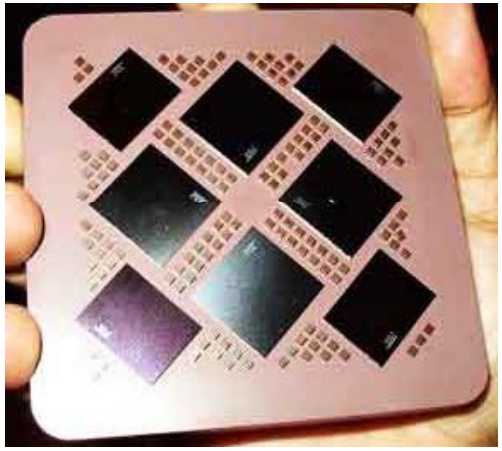
System on Chip

- Several components are integrated into a chip



MCM

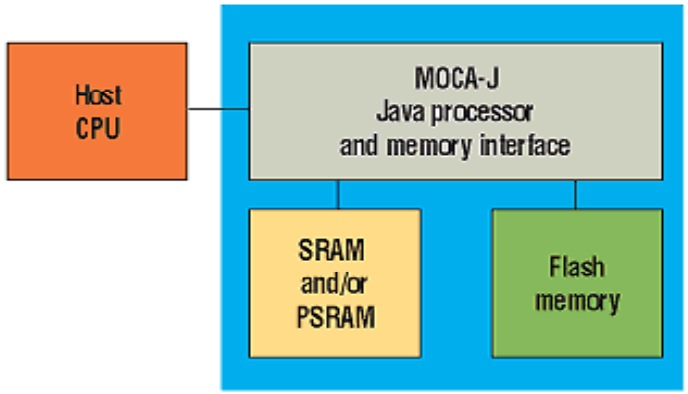
- Multi-chip module package
  - Several specialized chips are also assembled in a single ceramic package as a system solution using traditional assembly processes
  - The chips in an MCM are mounted on the same plane (the cavity substrate), whereas SiP employs die stacking as its natural configuration

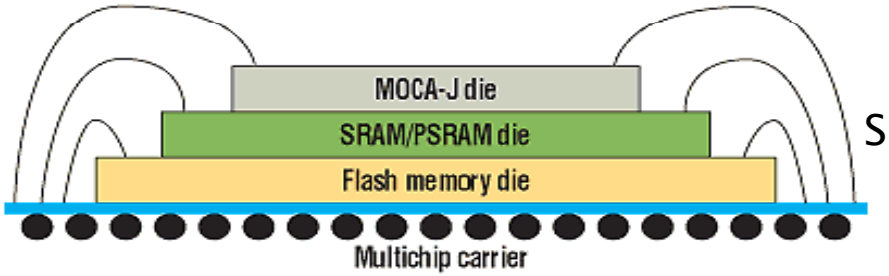


Source: IBM Power5

System-in-Package

- SiP design and test is a viable, rapid, and cost-effective solution to high-density system integration
- SiP is more than an IC package containing multiple die
- SiP helps exceed the limits of the SoC designs

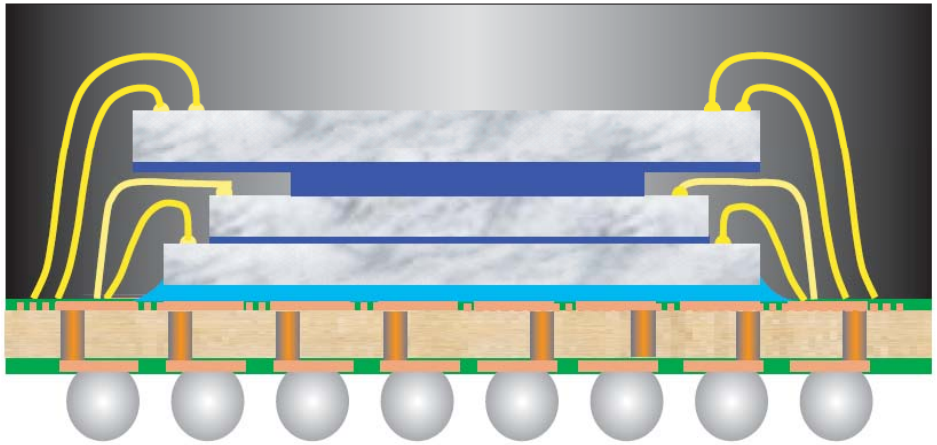




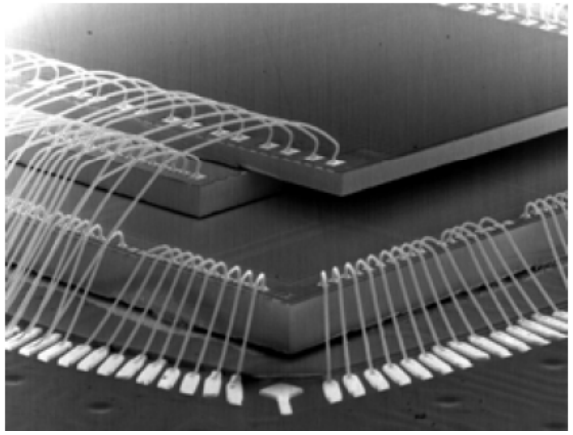
Source: nanoamp

Three-Dimensional Packaging

- 3D packaging is critical to integrating the multi-media features consumers demand in smaller, lighter products
- It can deliver the highest level of silicon integration and area efficiency at the lowest cost



Source: Amkor



Source: ETS07

SiP Market

- Portable devices, cell phone
  - 70~80%
- Module integration
  - RF cellular, RF amplifier, switch, transceiver
  - Digital
  - Memory module, DRAM, Flash
  - WLAN, Bluetooth
- In 2008, 3.25 billion SiPs are expected to be assembled

Advantages of SiP

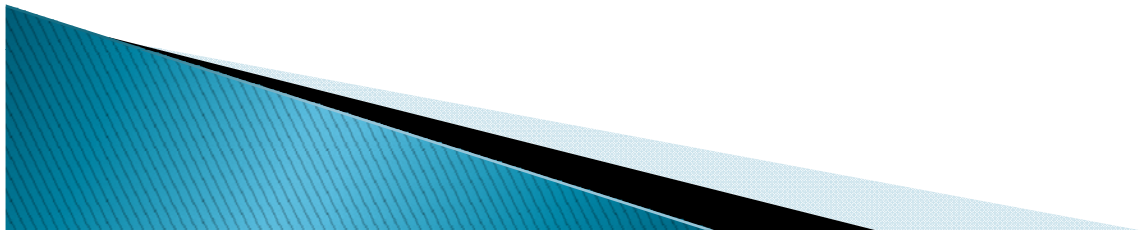
- Combining different die technologies (Si, GaAs, SiGe, etc.)
- Combining different die geometries (180nm, 90nm, 45nm, etc.)
- Including other technologies (MEMS, optical, vision, etc.)
- Including other components (antennas, resonators, connectors, etc.)
- Increasing circuit density and reducing PCB area
- Reducing design effort
- Improving performance

Challenges

- The most critical issues are design and test methods and solutions
  - Common EDA tools are necessary for integrating mixed-signal and RF blocks
  - KGD should be readily available for SiP designers
  - The proliferation of integrated passive devices (IPD) at the SiP substrate level is needed

Test Issues

- How to test chips and packages
  - DFT, package test, and KGD strategies
- How to integrate and test different types of memories
  - Alternative design and package options
  - Debug and yield enhancement



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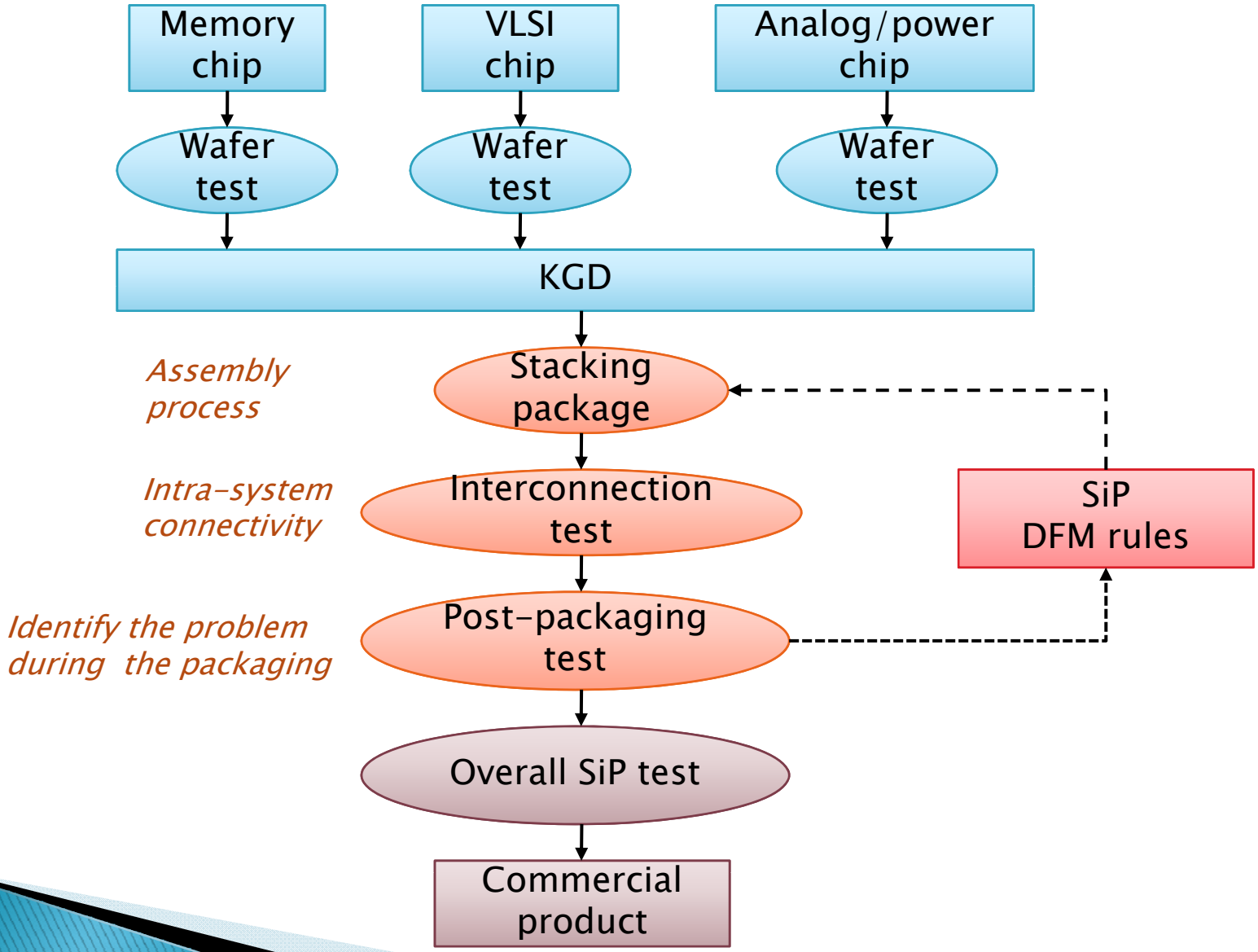
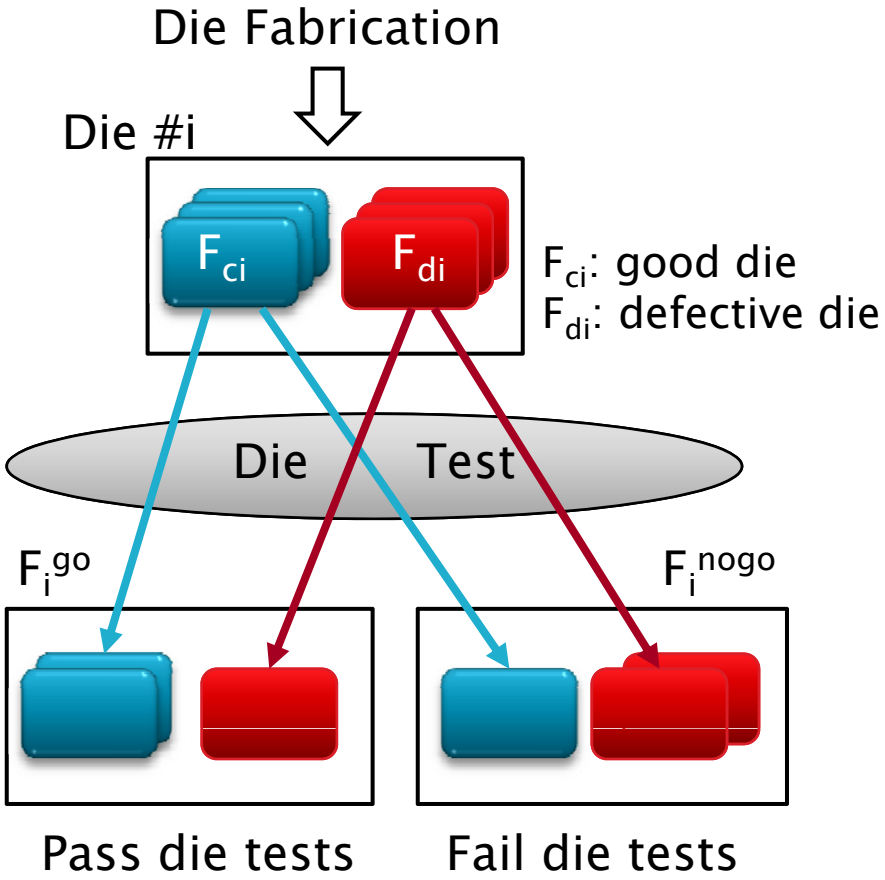
SiP Test Flow



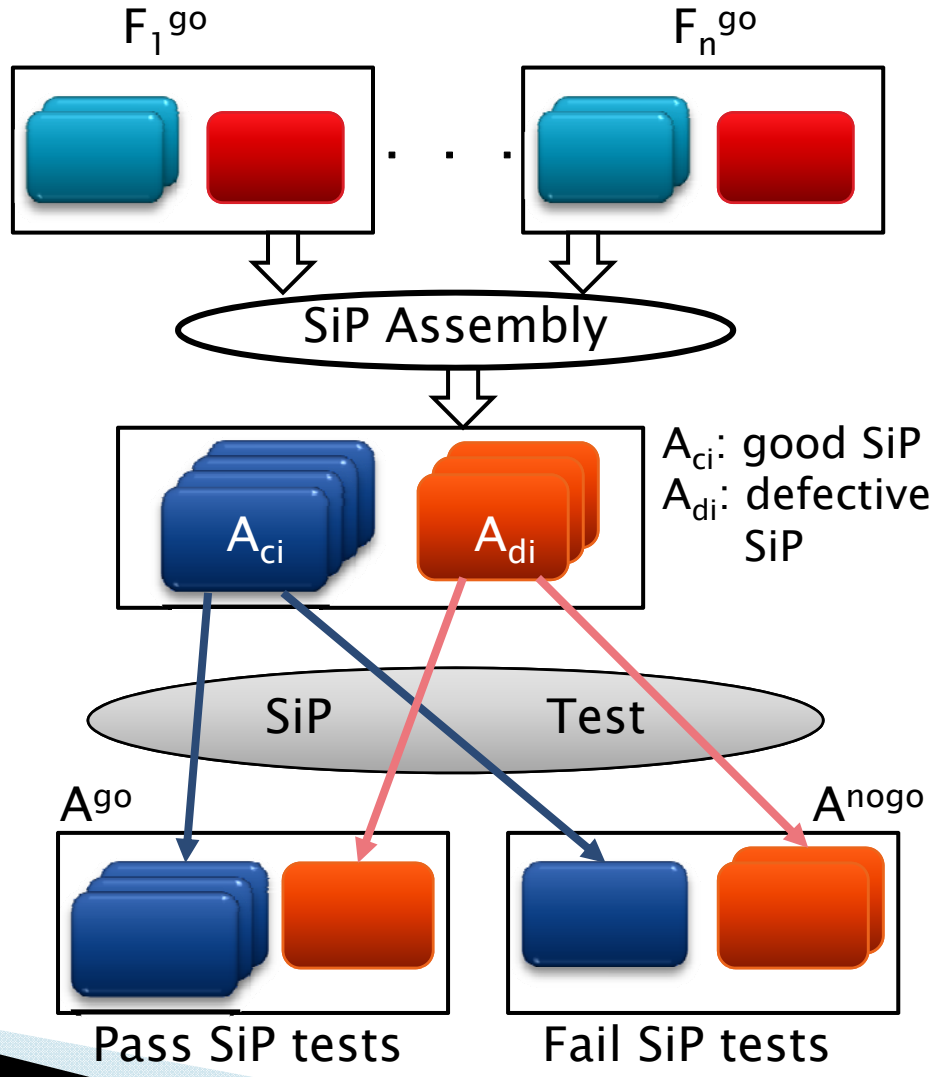
Quality

- Die process



Quality

- SiP Process



Yield of SiP

- If various chips are used in a chip
  - $Y_m=[(p1)^A(p2)^B(p3)^C\ldots]$
  - Y_m: yield probability for assembled chips
  - A, B, C: number of dice of each type
  - p1: probability of die 1 being good
- Yield of SiP is also dependent on
  - P_s: Know-good probability of substrate
  - P_i: Know-good probability of die interconnects
  - Q: number of interconnects
  - P_w: probability of assembly workmanship
  - $Y_{sip}=Y_m x P_s x (P_i)^Q x P_w$

SiP Defect Level

- Definition of defect level: percentage of SiPs shipped which passed the SiP test, but may be faulty
  - $DL=1-Y_{sip}^{(1-FC)}x100\%$
  - Y_{sip}: yield of SiP
  - FC: faulty coverage
- Defect level can be reduced by high quality bare dies and high FC

Example

- The assembly process accumulates all the problems of the individual dies

	DLi (ppm)	Pi (%)
Substrate	600	99.94
Die 1	4100	99.59
Die 2	35500	97.45
Die 3	1200	99.88
Y_{SIP}		96.87

Bare Dies Testing

- To test an SiP, each bare die must be tested first before packaged in the SiP
  - To eliminate compound yield loss
- It is performed at standard wafer sort
  - Manufacturing defects of silicon implementation
- Known Good Dies
  - Confidence level that bare dies are fully tested for performance over a temperature range
  - A bare die with the same quality after wafer test
- Mechanical probing techniques
- Electrical probing techniques

KGD Approaches

- Process control-based approach
  - Improve yield through six sigma and zero defect yield programs
- Testing-based approaches
  - Sampling approach
  - Full test and burn-in approaches
    - Temporary pressure contacts
      - Wafer-level
      - Die-level
    - Permanent contacts
    - Semi-permanent contacts
  - Design-based approaches

Testing-Based Approaches

- Require high quality functional test
- Require performance test
  - Performance driven application (at-speed)
- Require reliability screening
  - Wafer level burn-in
  - Tape automated bonding (TAB)
  - Temporary test packaging

Sampling Approach

- Based on statistical probability of KGD
  - Systematic defects- process or design-related problems
- Process
  - Package a sufficient sample of dies in wafer lot
  - Perform exhaustive test and burn-in
  - Certify entire lot if meets requires criteria
  - Perform binning each die based on tests of nearest neighbors

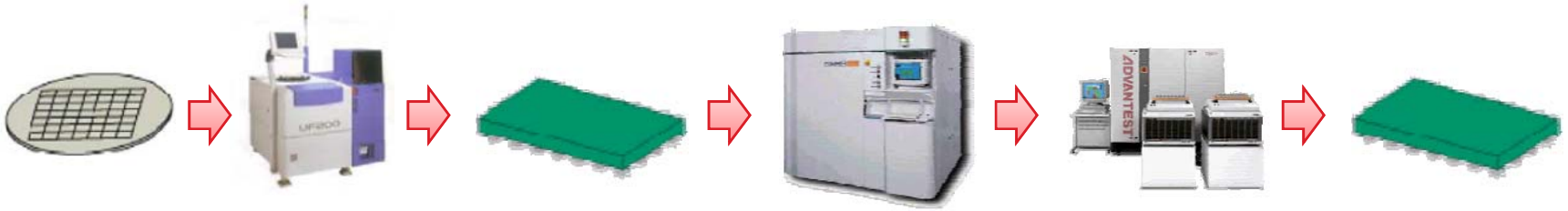
Full Test and Burn-In Approaches

- A: Temporary pressure contacts
  - Wafer level
    - Reliability screens
    - Burn-in
  - Die level
    - Temporary packages, carrier
    - Probe cards and techniques
    - Membrane pressure
- B: Permanent contacts
- C: Semi-permanent contacts

Wafer-Level Burn-In

- Full wafer contactor
- Applied High voltage and temperature
- Long term solution for KDG

Traditional back-end



Wafer → Wafer probe → Package → Burn-in → Final Test → Know-Good-Package

Wafer-level Burn-in and Test

Wafer → Wafer-level burn-in and test → Wafer final test → KGD wafer

Wafer-Level DC Stress

- Used for many years by DRAM vendors to reduce burn-in time
- Often referred to as wafer-level BI
- Provides external control of array voltages
- Stresses most defects

Die-Level Burn-In Methods

Method	Pitch Limit	Process complexity	Parallelism	Initial $	Operating $	Optimal Value
Carrier	>120um	Med High	Low-Same as PLBI	Low	Medium	Low
Sac Metal WLBI	>120um	High	High-full Wafer	Medium	Medium High	High
Direct Contact WLBI	<100um	Low	High-full wafer	High-Contactor tooling and NRE	Low	High

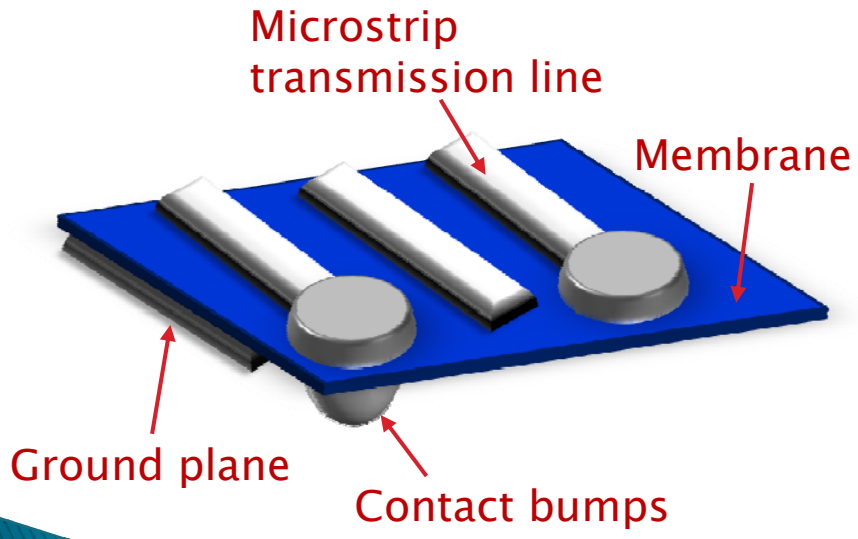
Source: freescale

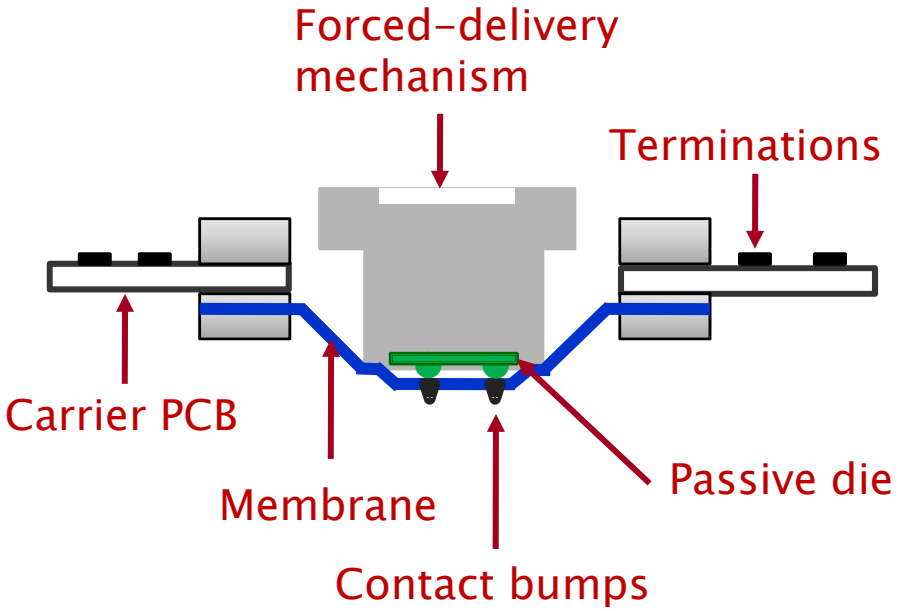
Probe Cards

- Wafer sort using probe card is a traditional technique
- New probe cards are required for new die
- High performance operations depends on probe pin
- ATE Limitations
  - High I/O counts
  - High performance devices
- For bare dies, probing technology is crucial

Membrane Contact

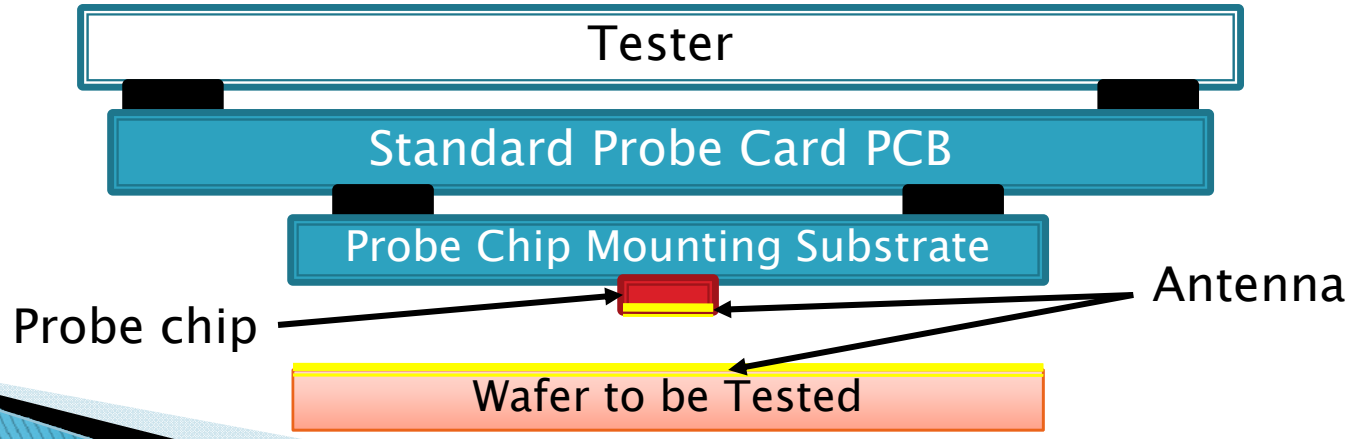
- The distance between the pads and the tuning components is reduced
- The membrane offers significant advantages for high-performance wafer test





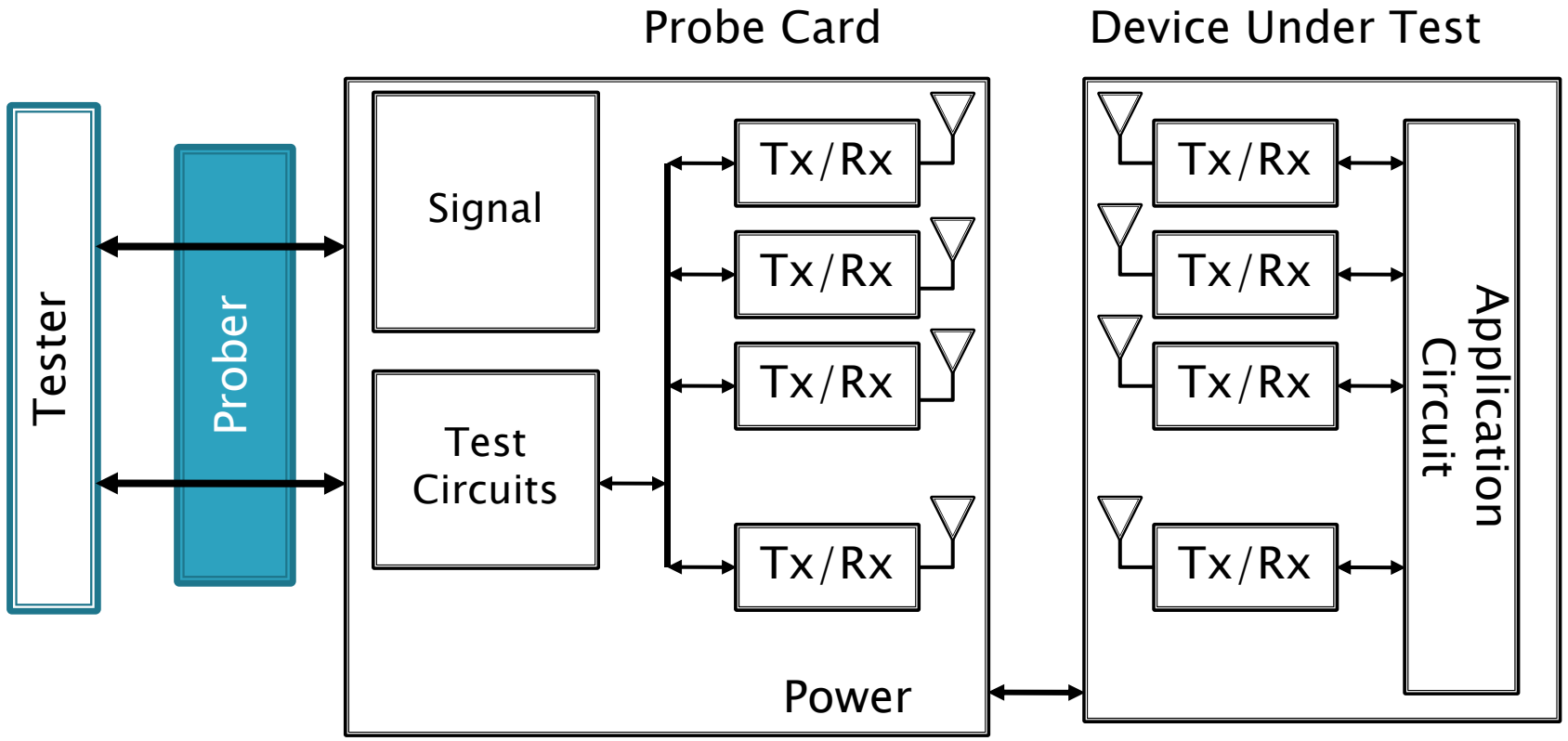
Mechanical Probing Techniques

- Vertical probe was developed to fulfill the requirement for array configurations
  - Co-planarity
  - The demand on novel and expensive probe techniques is increased
- Solutions
  - MEMS-based implementations of probe cards
  - Noncontact testing



Noncontact Testing

- Each antenna and transceiver probes one I/O on the DUT with each I/O site on the DUT



Electrical Probing Techniques

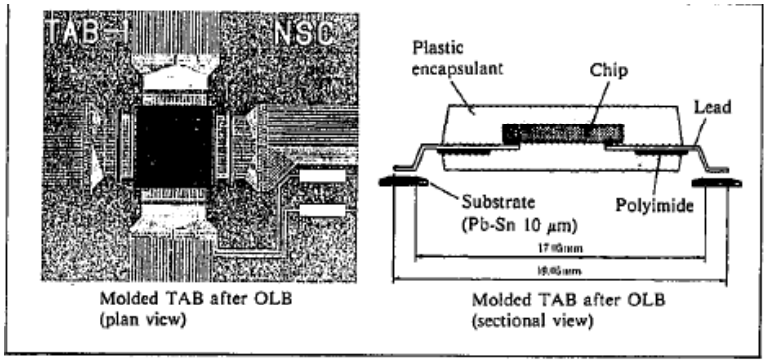
- Testing RF and mix-signal ICs represents a big challenge due to the propagation of disturbed signal
- Wideband protocols add many constraints to the wafer probing
  - Membrane

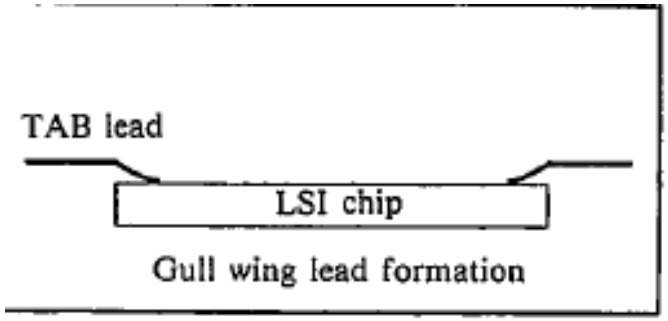
Full Test and Burn-In Approaches

- A: Temporary pressure contacts
- B: Permanent contacts
  - TAB (Tape Automated Bonding) lead frame bonded
  - Testable ribbon bonding
  - Bare die carrier
- C: Semi-permanent contacts

Permanent Contacts

- Minimal package permanently assembled with die
- Die bounded into low cost carrier or tape
- TAB lead frame bonded to IC
  - Full test and burn-in is possible
  - TAB technology is expensive
- Testable ribbon bonding
  - Die ribbon bounded to low cost carrier
  - After test and burn-in ribbon cut, leaving TAB like die
- Bare Die carrier
  - No performance penalties
  - Easy carrier replacement





Design-Based Approaches

- DFT
- Yield optimization loop
  - Yield learning; detection, analysis, and correction
- Architecture of IIP
  - Ensures manufacturability and lifetime reliability of SiP
- Embedding process monitoring IP
  - Test vehicle or test die
- Embedded test & repair IP
  - Embedded memory with redundancy
- Embedded debug & diagnosis IP
  - Collect failure data and analyze obtained data by off chip

Bare Substrate Testing

- Test for electrical integrity before attachment
  - Mechanical probing
  - Contactless electron-beam probing
- Prevent population of defective substrates
  - No possible to repair substrate
  - Dies damaged during removal
  - High cost
- Failure mechanisms
  - Short and open

Substrate Testing

- Known good substrate is required prior to bonding
- In-Process Testing
  - Intermediate tests during fabrication to access every wiring layer
  - Mainly contactless probing techniques
  - Helps process improvement and process control
- Final Testing
  - Before populating expensive bare dies

Substrate Testing Techniques

- Mechanical probing – slow
  - Bed of nails – traditional PCB testing
  - Moving test head
  - Single/double point flying probes – capacitance and resistive, open, and short testing
  - Glow discharge – optically detect opens and shorts
- Contactless probing - fast
  - Automatic optical testing – image analysis
  - Electron beam testing – charge and read each pad

Bed-of-nails probing

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SiP Assembly Process

- Incoming bare die test
- Mounting process
  - Mechanical placement
- SiP assembly test
  - Parametric test
  - Functional test
- Encapsulation
  - Molding a plastic body around substrate
- Burn-in
- Retest
- Rework

SiP Testing

- Die-to-die interconnection
  - Delay marginalities
- Die-to-die bonding
  - Electromechanical marginalities
- Marginal pad or die placement on the substrate can affect the yield
  - Electrical effects, such as crosstalk or bonding violation
- Need microprobing and traceability

System Test of SiP

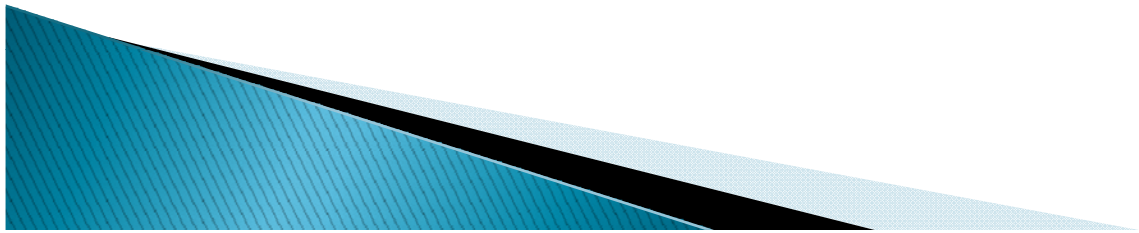
- Functional test
  - Structural and performance test
  - Check application specifications and functionality
  - Require a complex test setup with expensive instruments
  - Long test times
  - Testing full paths makes diagnostics difficult
- Access methods

Test Challenges for SiP

- Accessibility
- Controllability
- Observability
- Failure localization
- Failure analysis
- Deep memory and mixed signal
- Design for test (DFT)

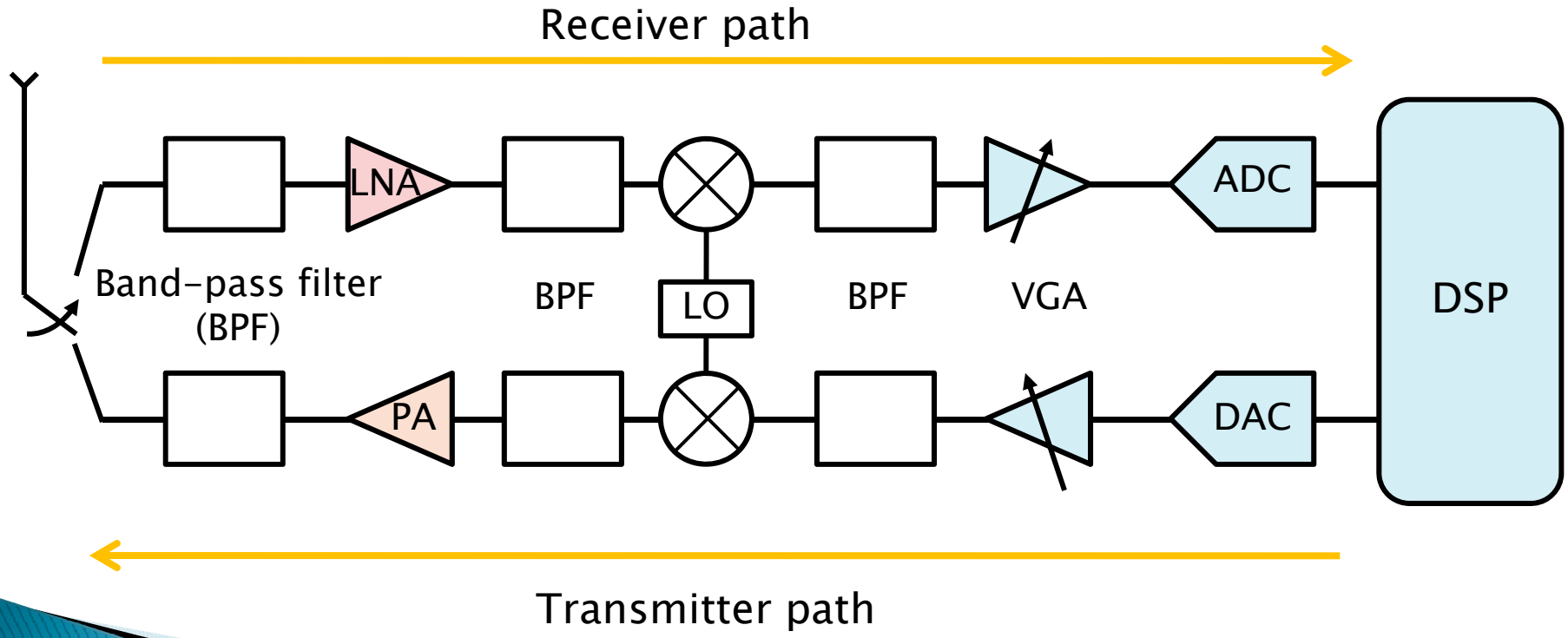
Functional System Test

- Advantage of functional test
  - Good correlation at the system lelvel
- Disadvantages
  - Complex test setup with expensive instruments
  - Long test times
  - Diagnostic difficulty
- Example:
  - Path-Based testing
  - Lookback techniques



Path-Based Testing

- Consider a system with a digital plus mixed-signal circuitry, an RF transceiver , and a power amplifier dies



Receiver Test

- The quality of a receiver is given by its bit error rate (BER)
- The BER test requires a lot of data to achieve the target accuracy
- A bit-error, p_e

$$p_e = 0.5 \cdot erfc\left(\sqrt{E_b / N_o}\right)$$

$$E_b = C / f_b$$

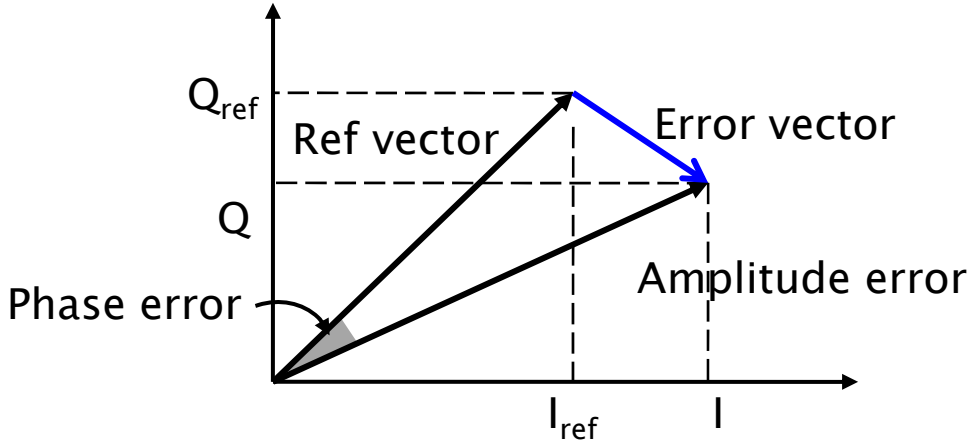
N_o : the noise power spectral density
E_b : the energy of the received bit
C : the power of the carrier
f_b : the data rate

Transmitter Test

- The transmitter channel is usually tested by measuring the error vector magnitude (EVM)
  - V(t) represents the transmitted signal, where I(t) and Q(t) are the data signals

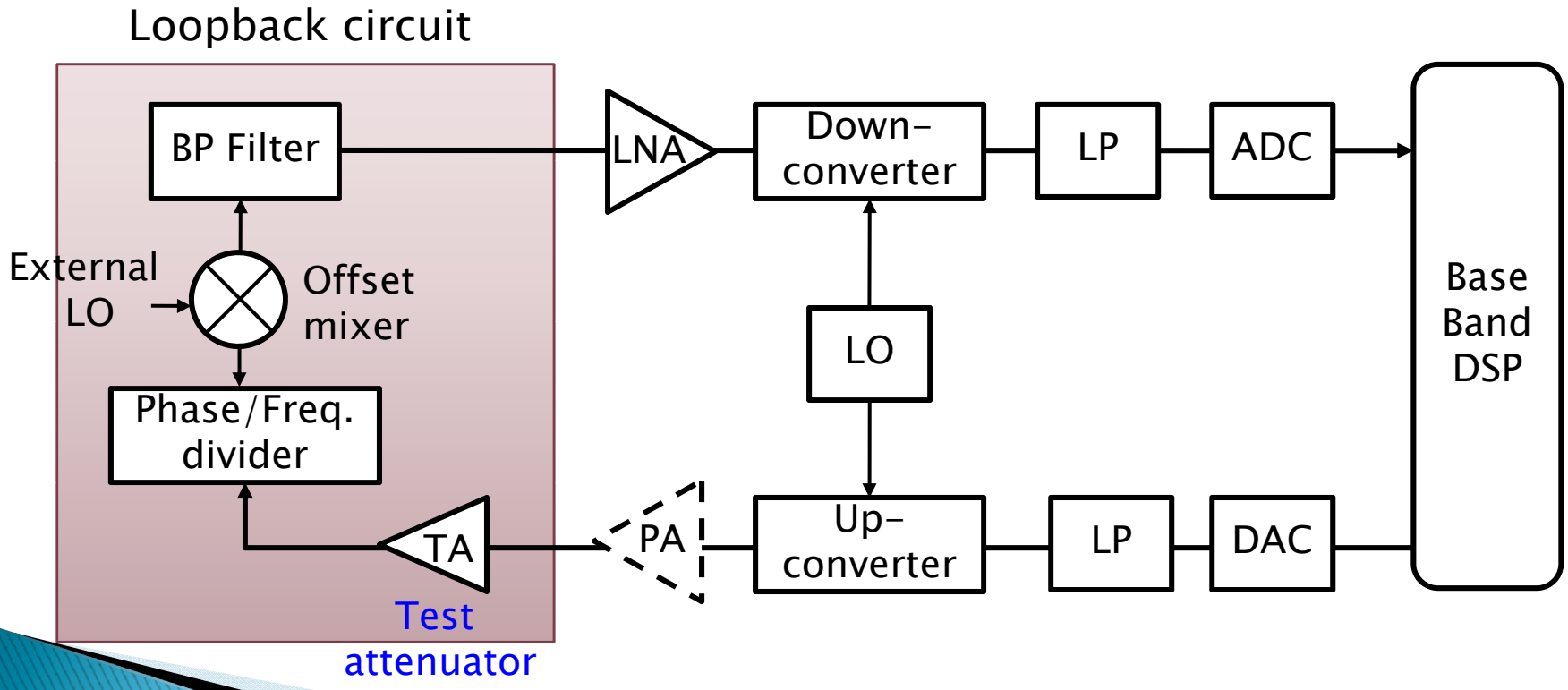
$$v(t) = I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t)$$

$$EVM = \sqrt{\left(I - I_{ref}\right)^2 + \left(Q - Q_{ref}\right)^2}$$



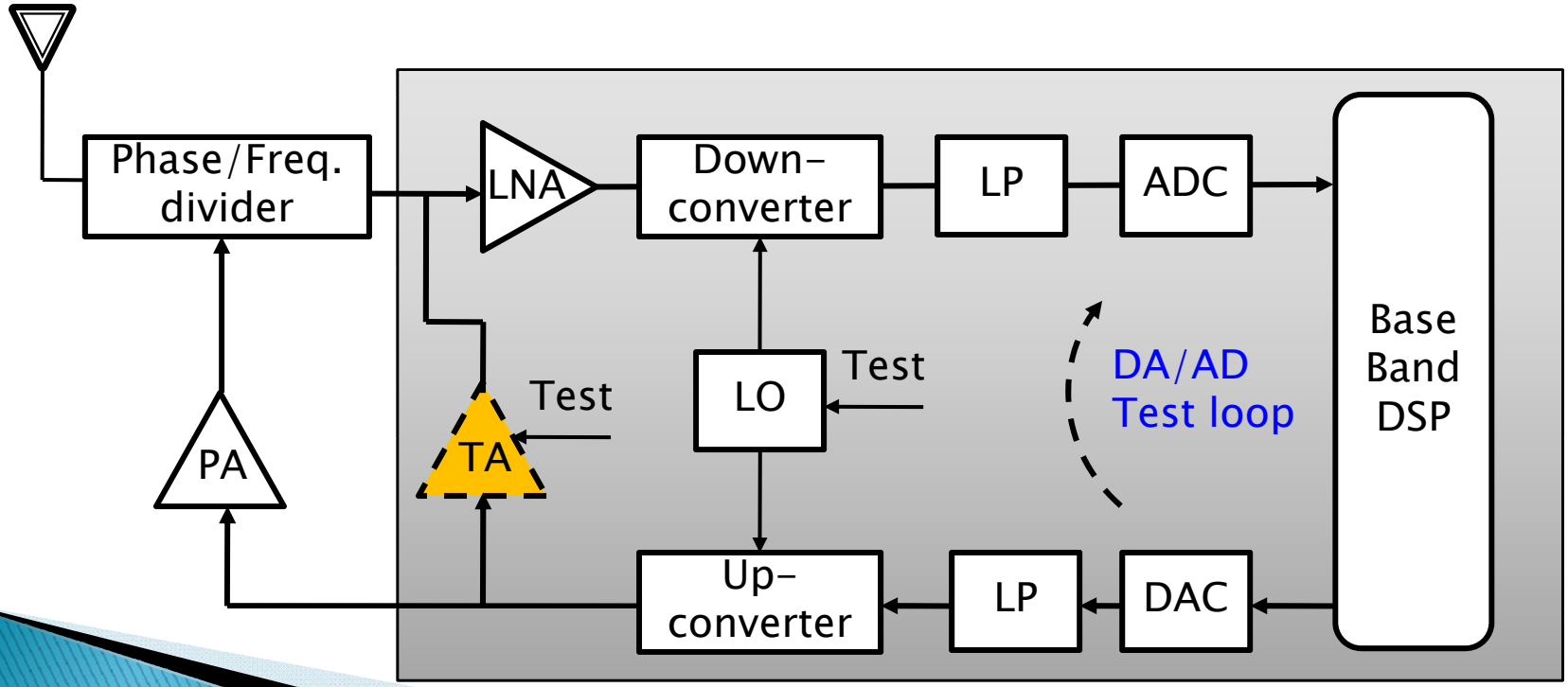
Loopback Techniques-External

- External
  - Creating the loop between the output of PA and the input of LNA



Loopback techniques-Internal

- Internal
  - Creating the loop in the front-end IC
  - Connecting the up-converter to LNA through TA, a complementary BIST sharing the circuitry with on-chip resources



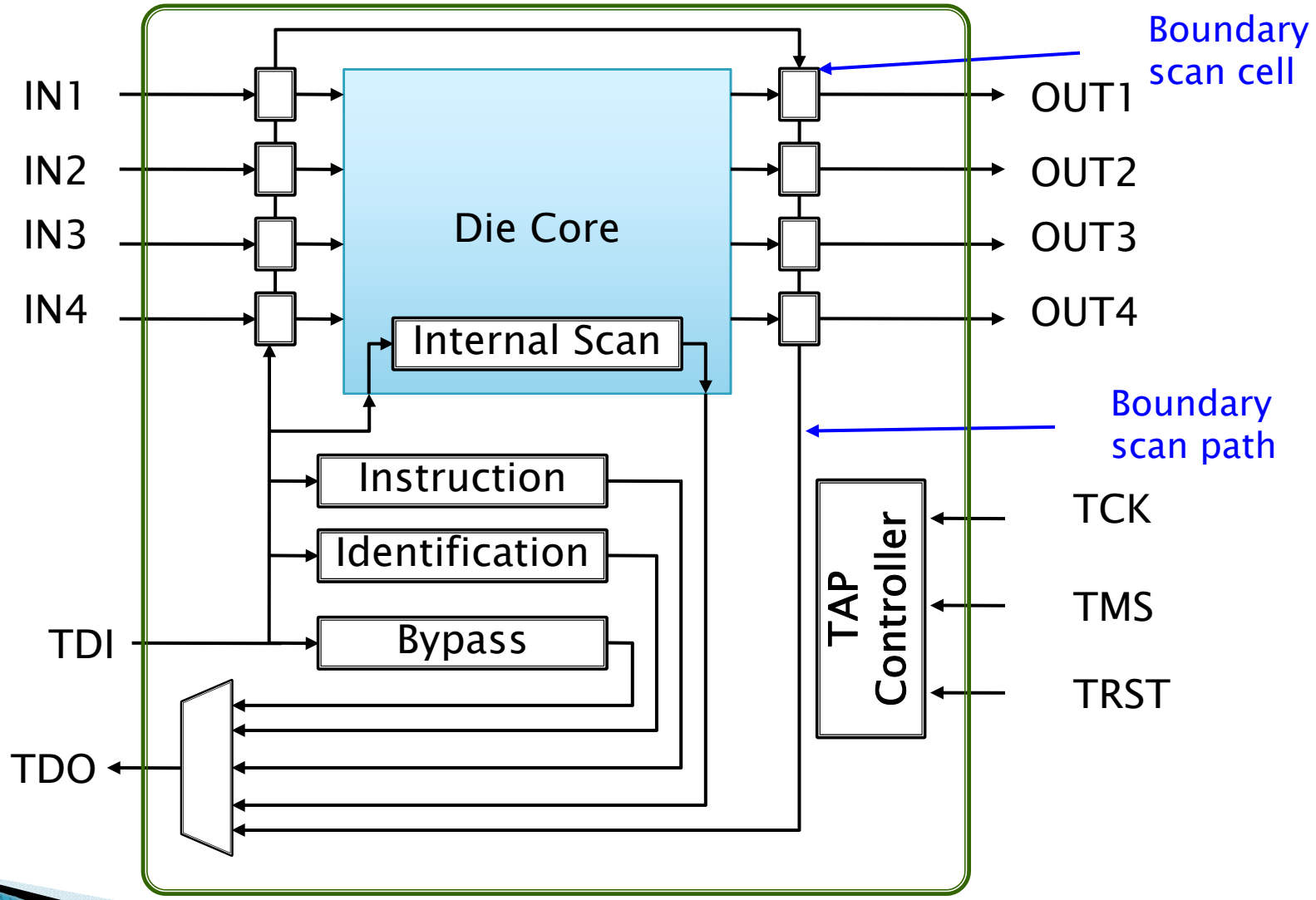
Test Embedded Components

- Structural testing of interconnections between dies
- Structural or functional testing of dies themselves
- Challenge
  - Hard to access the dies from the I/Os of the SiP
- To improve the testability, SIP test access port (TAP) is placed on the bare dies
- To provide high quality structural test and failed element identification capability, BIST and boundary-scan are used

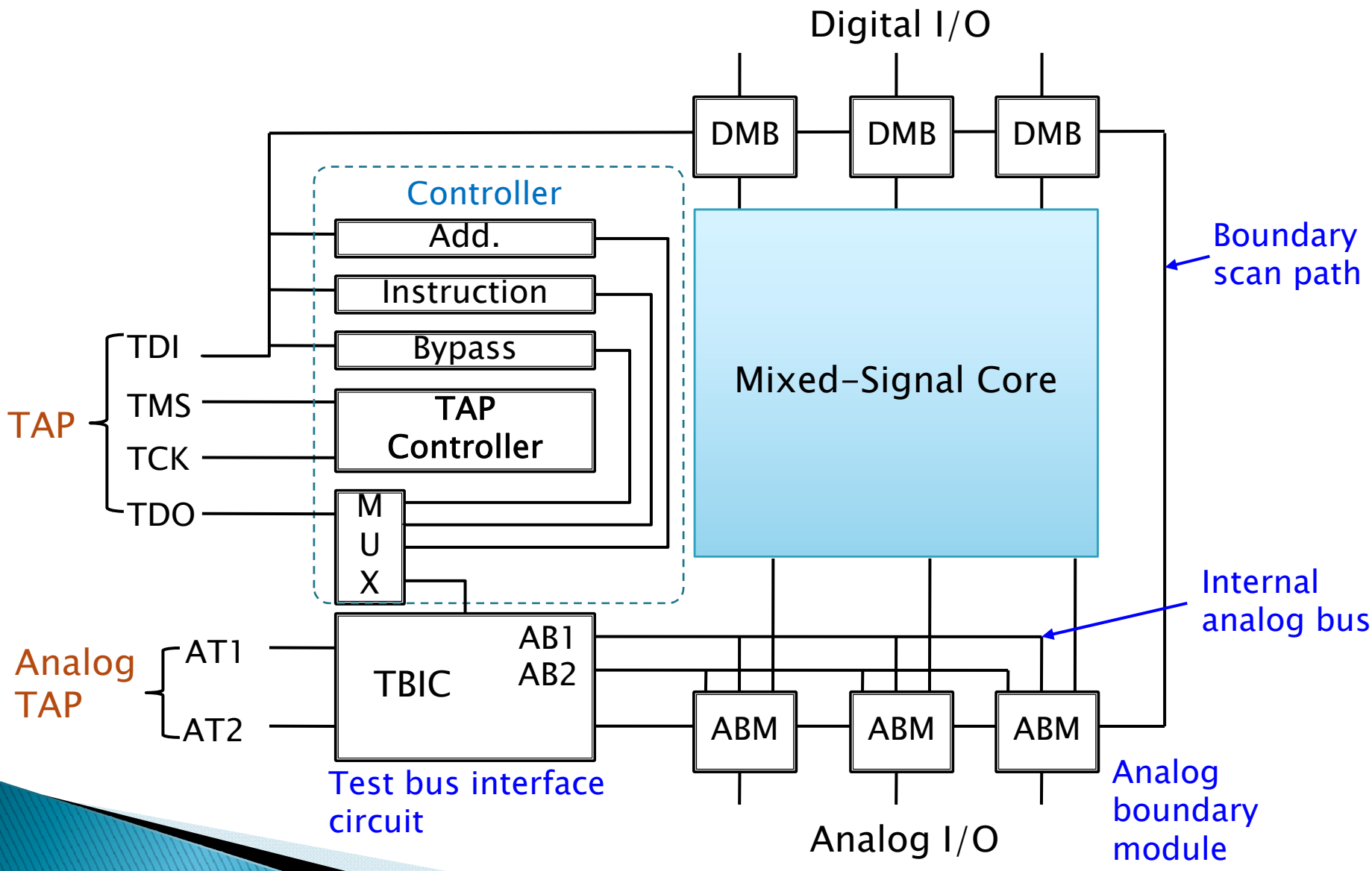
SiP Test Access Port

- Features
  - Access for die and interconnection tests
  - SIP test enabling at system level
  - Additional recursive test procedures during assembly
- IEEE 1149.1 and 1149.4
  - Boundary scans are used in bare dies
  - 1149.1 for digital dies and 1149.4 for mixed-signal or analog dies
- IEEE 1500
  - Designed for SoC test at system level

1149.1 Test Solution



1149.4 Test Solution



Ordered Assembly Strategy

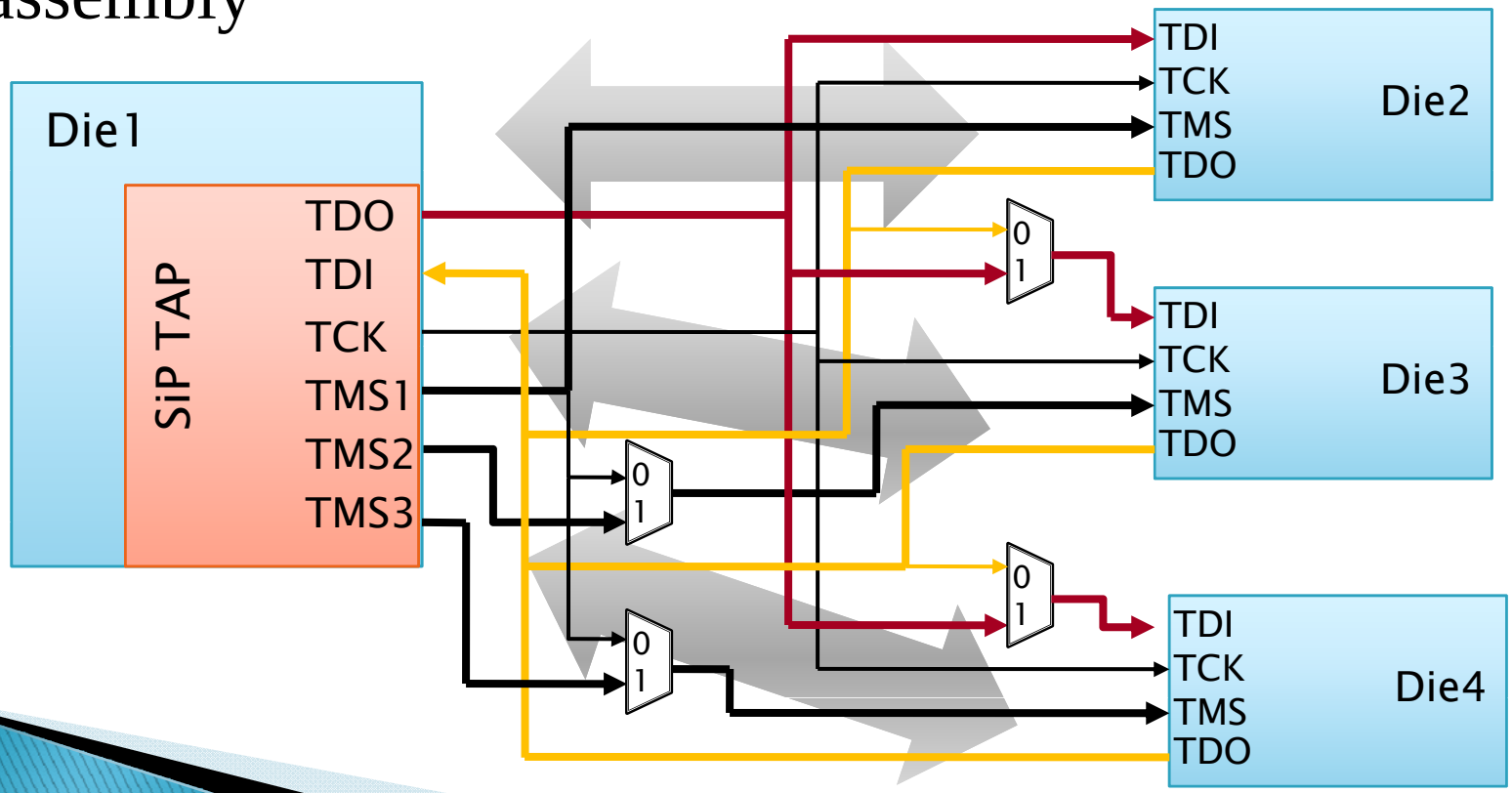
- The assembly process may introduce additional failures
- Intermediate tests after every die soldering may be required
- Dies are assembled from the least to the most expensive dies to optimize the overall SiP cost

TAP Controller

- TAP must manage boundary scan resources during the incremental tests even while some dies are missing
- Two configurations are required
  - One is for the incremental test - star
  - One is for the end-user test - ring

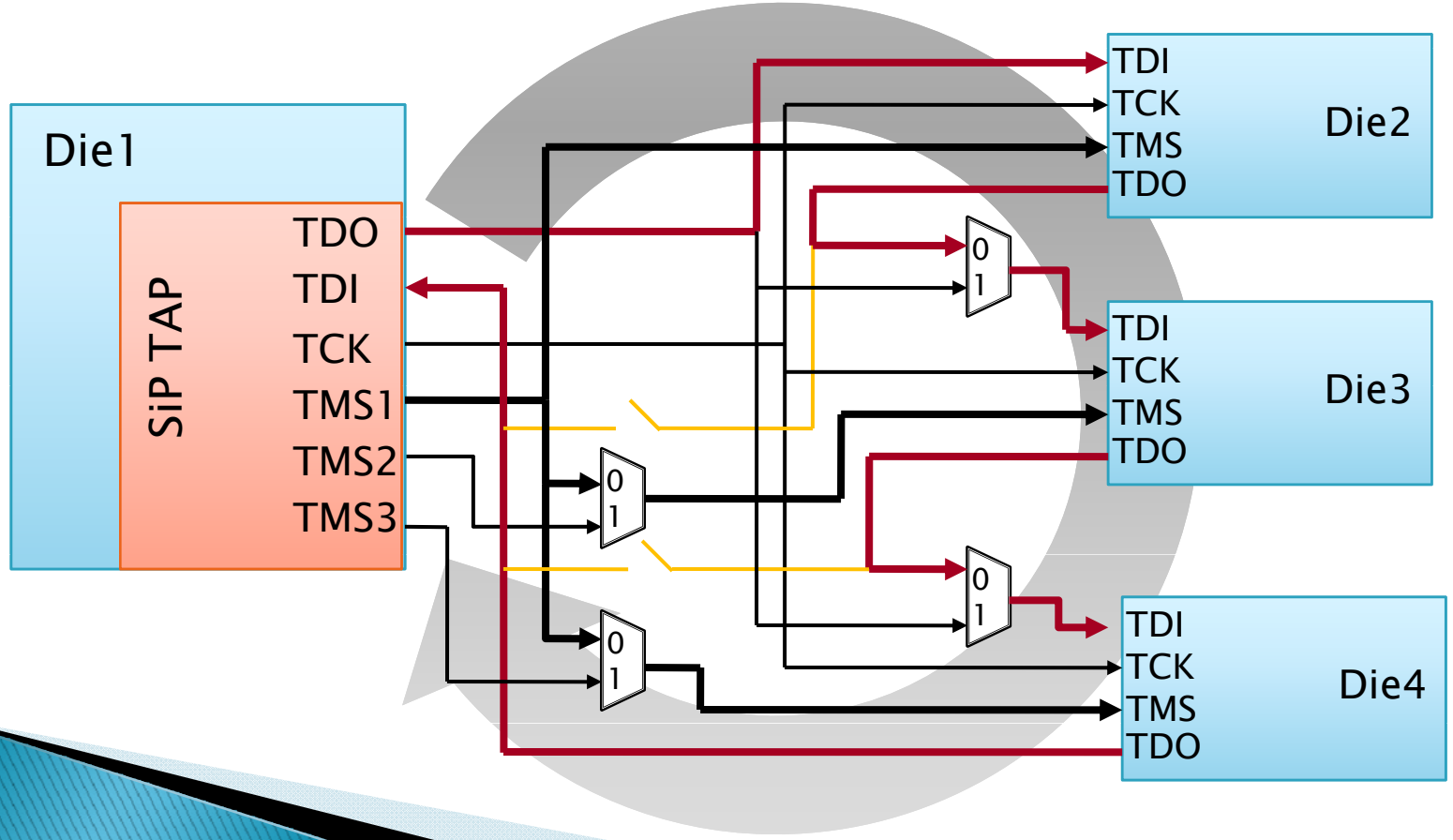
Star TAP Controller

- The star configuration attempts to facilitate incremental testing during the assembly
  - The link between the dies is broken during the assembly



Ring TAP Controller

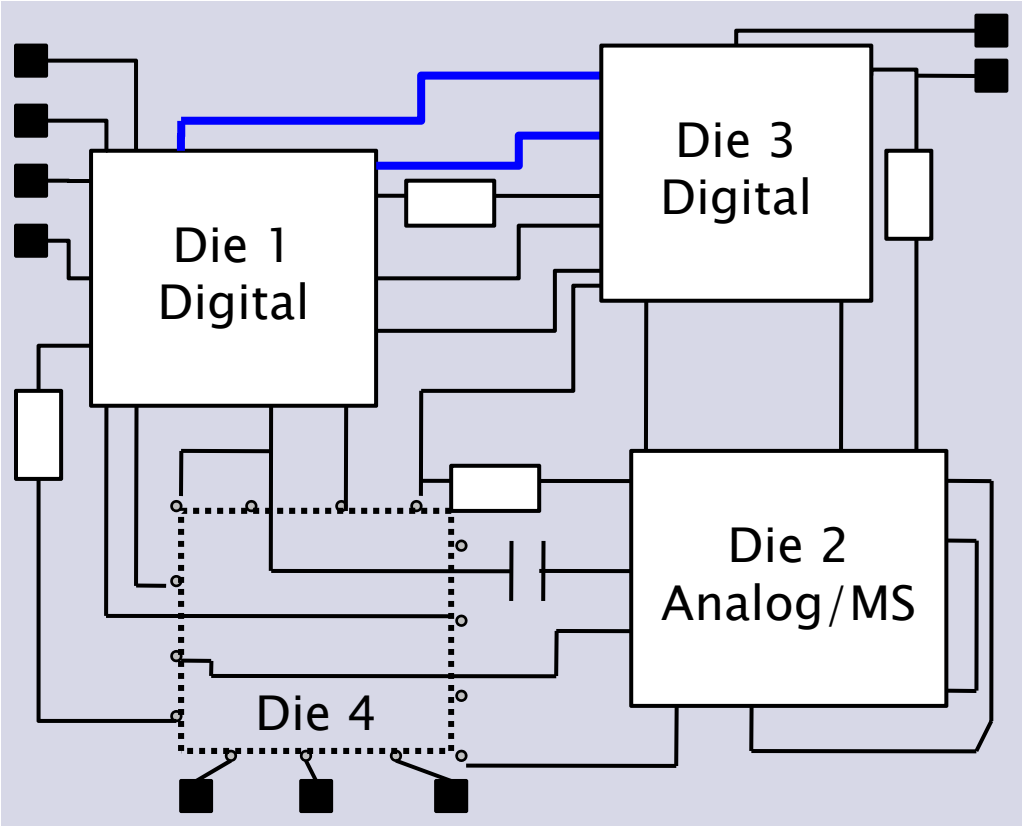
- The end-user cannot detect the presence of several dies in the ring configuration
  - Only one TMS control signal is required



Interconnection

- The interconnection test is performed through boundary scan in *external test mode*
  - For k wire, $\log_2(2k+2)$ vectors are required to test bridging faults

Step	Die 1	Die3	
1	Reset	Reset	
2	PRELOAD	PRELOAD	
3	EXTEST	EXTEST	Vector #1
4	EXTEST	EXTEST	Vector #2
5	Reset	Reset	

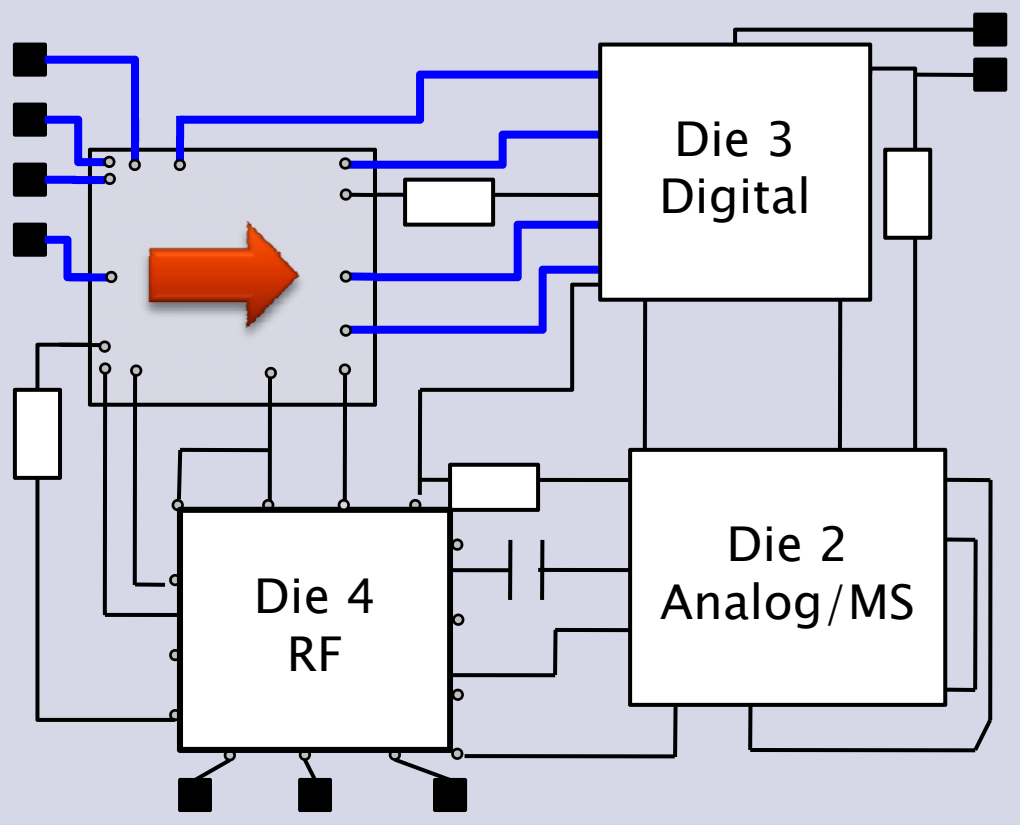


Digital and Memory Dies

- External pads of an SiP are less
  - Integrate additional DFT for testing specific dies on another die
  - Implement a configurable DFT with software or programmable capabilities on another die
  - Use the transparent mode of other dies to directly control and observe from the primary I/O
- Example
  - The embedded memories are usually packaged without BIST circuit
  - The BIST circuit has to be implemented in another digital core
  - Dies without boundary scan

Transparent Mode

- Use a transparent mode of the other dies to control and observe from the I/O of the package

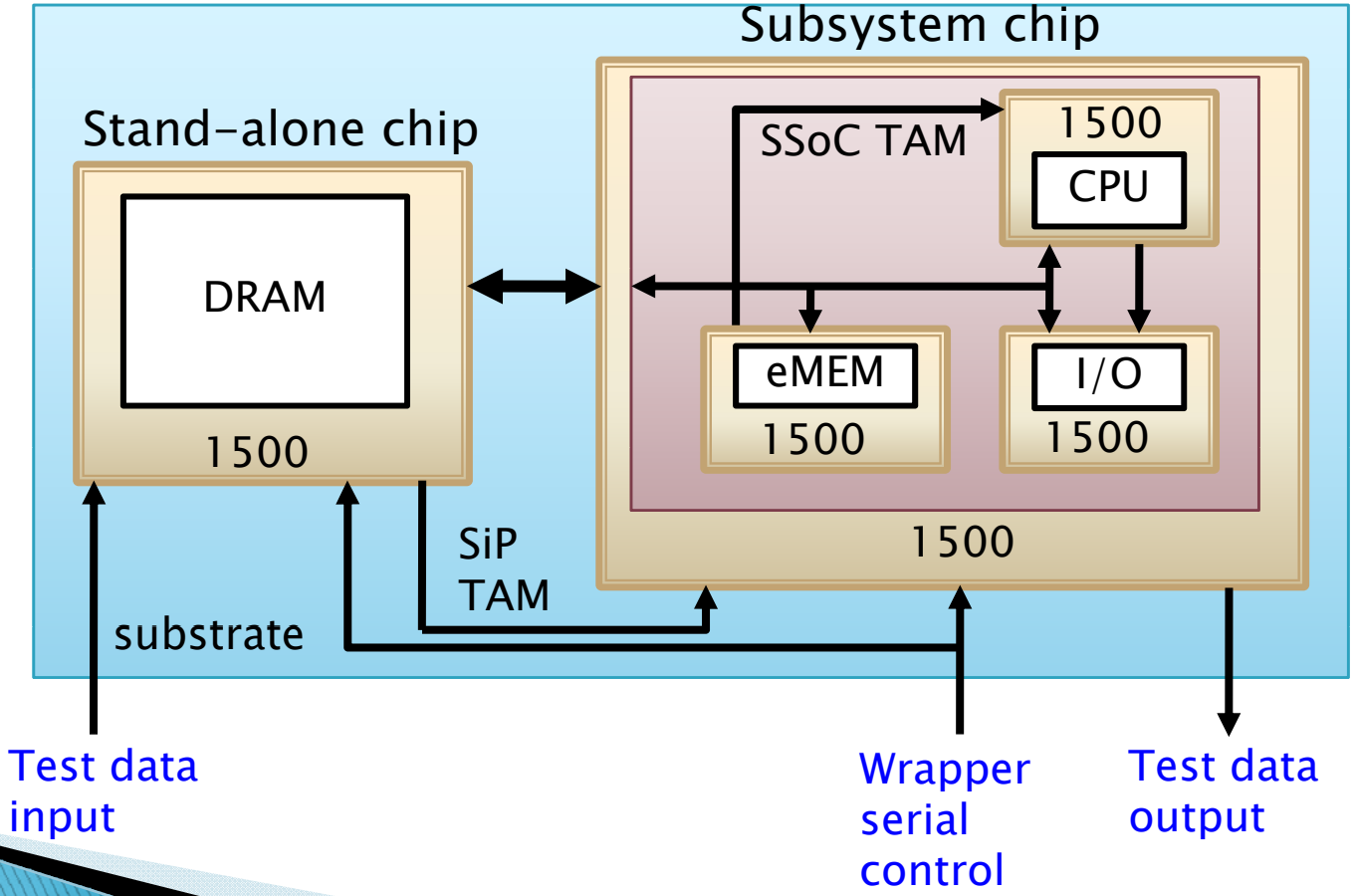


Hierarchical 1500 Test Solution

- Features
  - Easy and fast test interoperability at the core and subsystem layers
  - Effective support for chip-to-chip interconnection test
  - Definition of a standard approach for generating the chip-level and SiP-level test program

SiP with 1500

- A single serial line is used as the TAM
- It is useful for both chip-level and SiP-level test



SiP-Oriented Wrapper

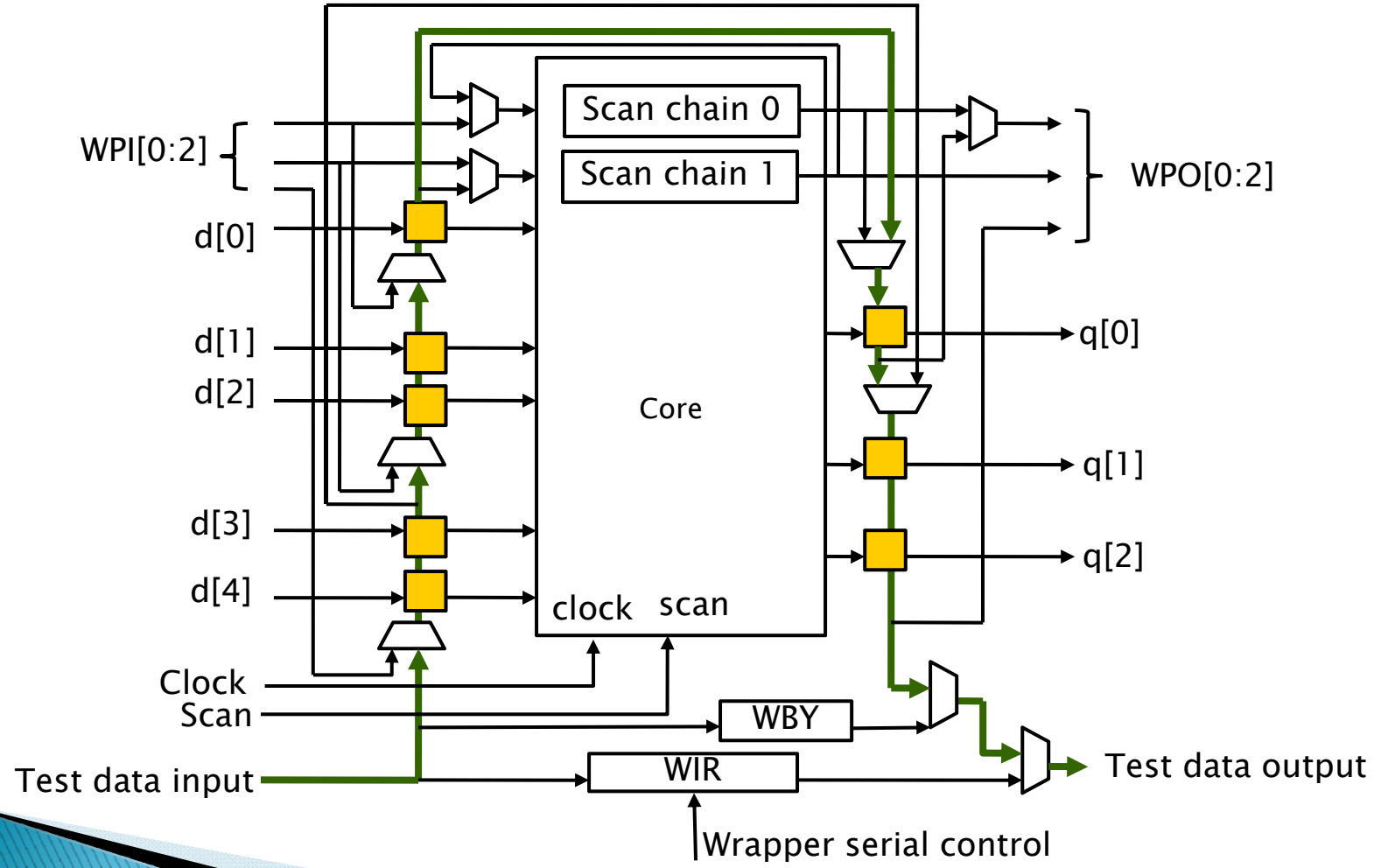
- The wrapper is to provide test data to each core and capture results and to perform data conversion for transmission on the selected TAM
- A six-signal bus allows management of the wrapper serial structures by controlling data transfers to and form each core

Registers in a Wrapper

- The wrapper boundary register (WBR) is used as a boundary scan chain at core level
- The wrapper bypass register (WBY) has a single flip-flop to bypass test data to other cores
- The wrapper instruction register (WIR) receives the instruction and controls the multiplexers

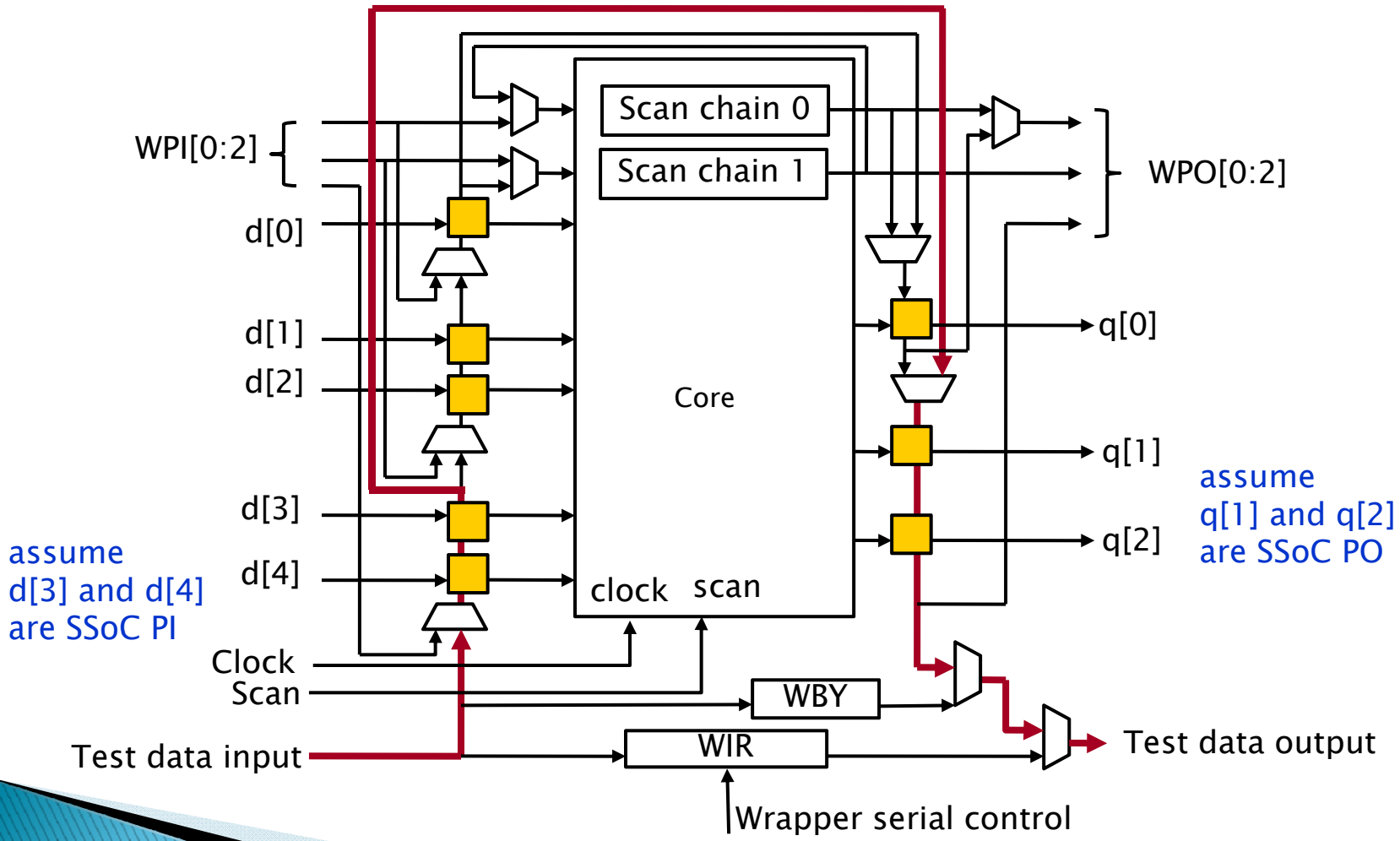
1500 Wrapper

- Core-to-core interconnection testing



1500 Wrapper

- Chip-to-chip interconnection testing

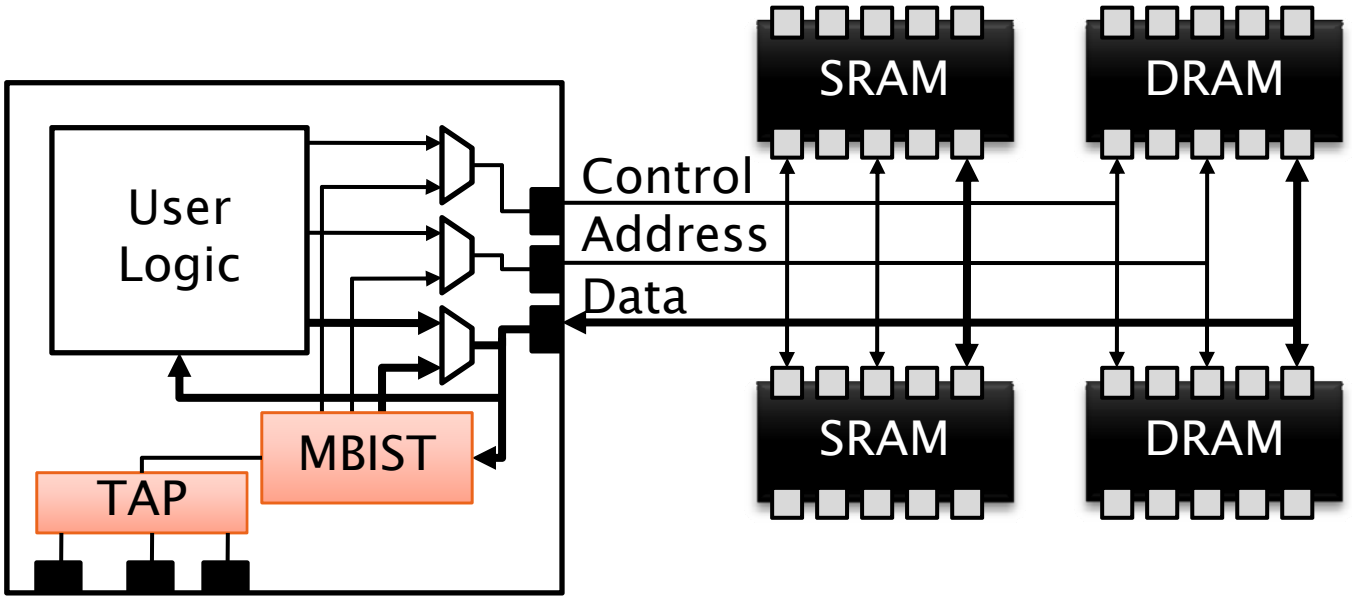


SiP Memory Test

- Memory test time dominates product test flow and test platform choice
  - SoC tester and memory tester
- DFT for mixed-signal and memory is the better solution

Test of Memories without BIST

- Use dedicated chip with BIST
- Include BIST facilities in neighboring dice



Test of Die without Boundary Scan

- Use boundary scan chain of neighboring ASIC
  - Memory arrays, glue logic, etc.
- Use dedicated boundary scan parts to create virtual boundary scan
  - Probe chip, octals, etc.

SiP Level BIST

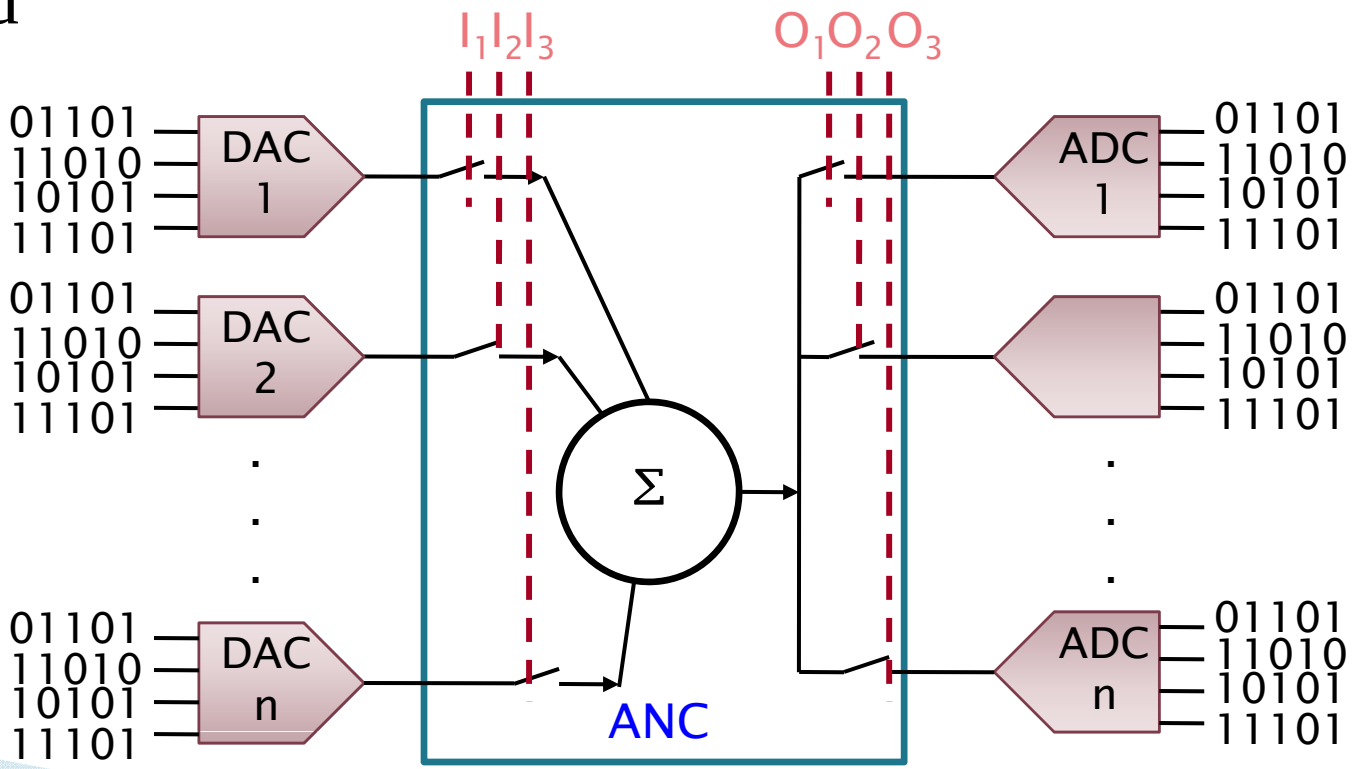
- Effective self-test in autonomous manner
- Test controller embedded in SiP, instead of external test processor
- Embedded ASIC block or dedicated chip
- SiP technology drivers
  - High quality test
    - BIST can provide high test coverage
  - Performance test
    - BIST runs at system speed
  - Reliability test
    - BIST runs during burn-in

Analog and RF Components

- Challenges
  - Cost reduction of the required test equipment
  - Difficult to access the dies after assembly process
- Analog, mixed signals, and RF circuits require long functional test time
- Approaches
  - Move tester functions onto the chip itself - BIST
  - Convert analog signals on-chip to timing delay information for ATE measurement
  - Use DFT techniques to internally transform the analog signals to digital signals
- Only digital signals are externally observed by less-expensive digital tester

Analog Network of Converters

- Assume that DACs and ADCs are available
- Input and output signals are fully digital
- Both DAC-to-ADC and analog blocks paths can be tested

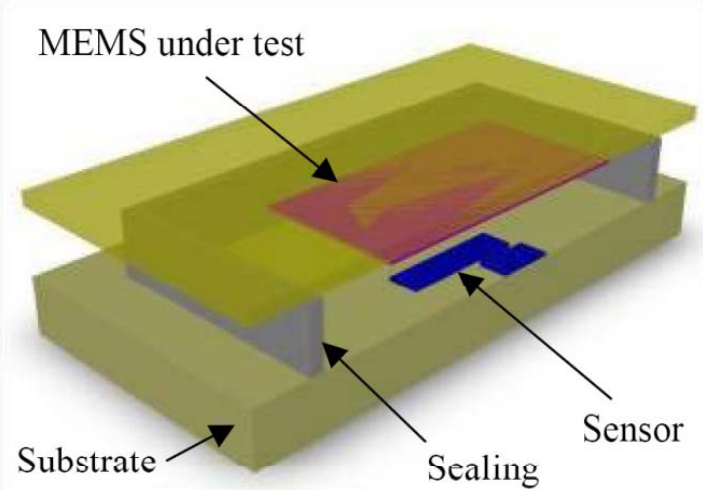


MEMS

- Test equipment is a problem for MEMS testing
- Two approaches
  - Perform an indirect structural or functional test
  - Implement DFT circuitry to convert the physical signal to an electrical signal
- Significant package influence is another challenge for MEMS testing
  - Hard to detect defective MEMS before packaging

MEMS Testing in SiP

- The classical problems are more serious
  - Adjacent dies might disturb and modify the MEMS quality
  - The test needs to generate and observe various nonelectrical signals for several MEMS in the same SiP
- The alternative techniques with only electrical signals are the only viable option



Source: ETS07