Chapter 0
Introduction

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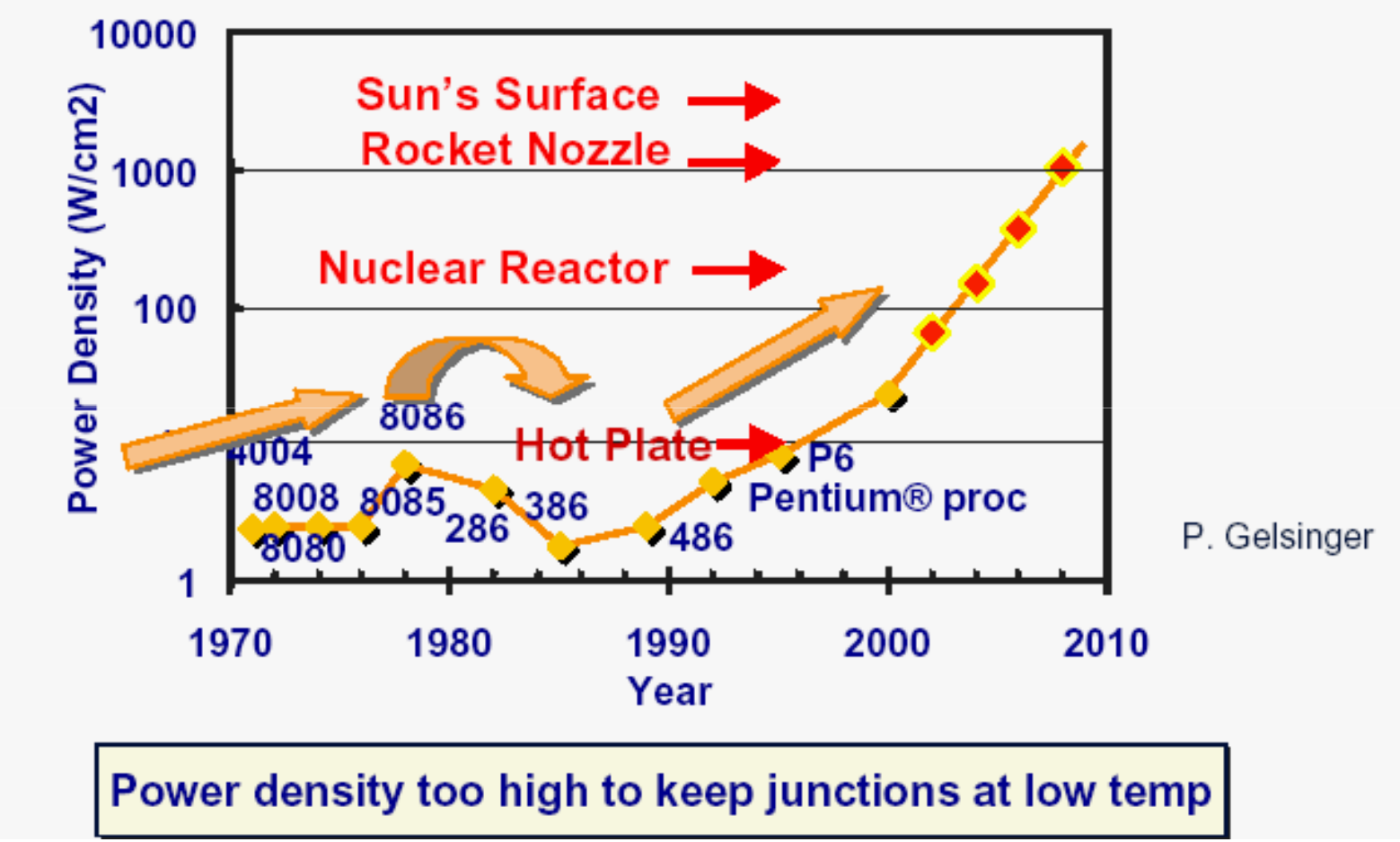
Nano-Scale VLSI Design Challenges

- Power issue:
  - Energy consumption, power dissipation, power delivery
- Reliability issue
  - Variability
  - Soft error (single-event upset)
  - Device degradation
- Yield issue
  - $Y=e^{-AD}$
- ….

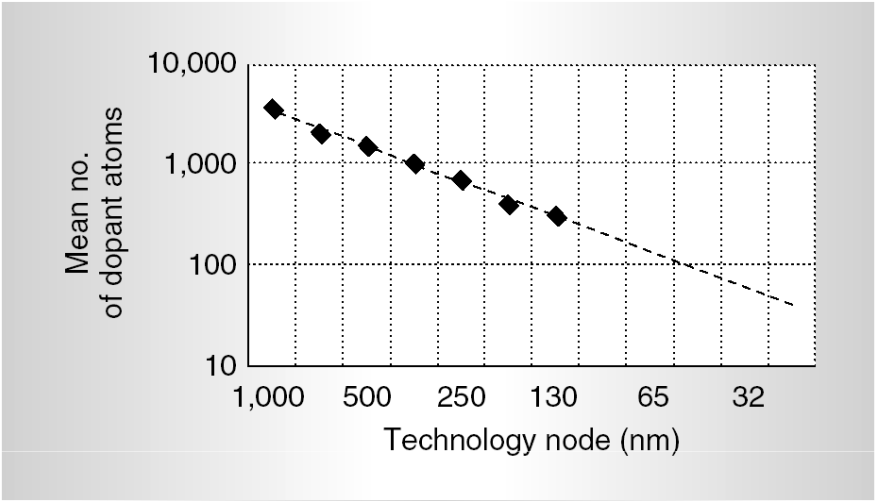
Power Will be Problem



Source: J. Rabaey, 2004

Source of Variations

- The first source is random dopant fluctuations



Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

- In the 1-micron technology generation there were thousands of dopant atoms, whereas in a 32- to 16-nm generation there are only tens of dopant atoms left in the channel
- Therefore, two transistors sitting side by side will have different electrical characteristics because of randomness in a few dopant atoms, resulting in variability

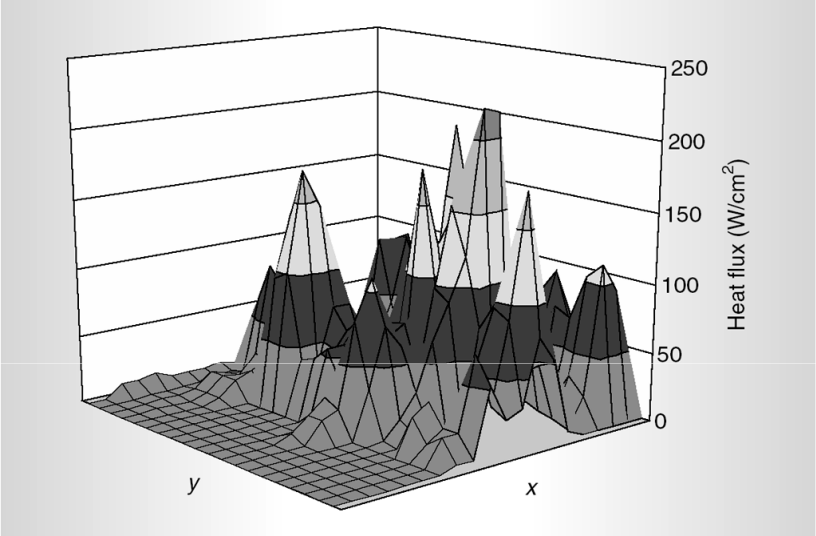
Source of Variations

- The second source of variability is because sub-wavelength lithography
  - 248-nm wavelength of light to pattern 0.25um & 0.18um transistors
  - 193-nm wavelength of light to pattern 130nm & 65nm transistors
  - The difference in the wavelength of light and the patterning width will continue to widen until extreme ultra-violet technology (13nm) becomes available
- The first two sources are static; that is, they occur during fabrication
- But the third source of variations is dynamic, that is it is time and context variant

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Source of Variations

- An example of heat flux (power density) in Watts per square centimeter across a microprocessor die

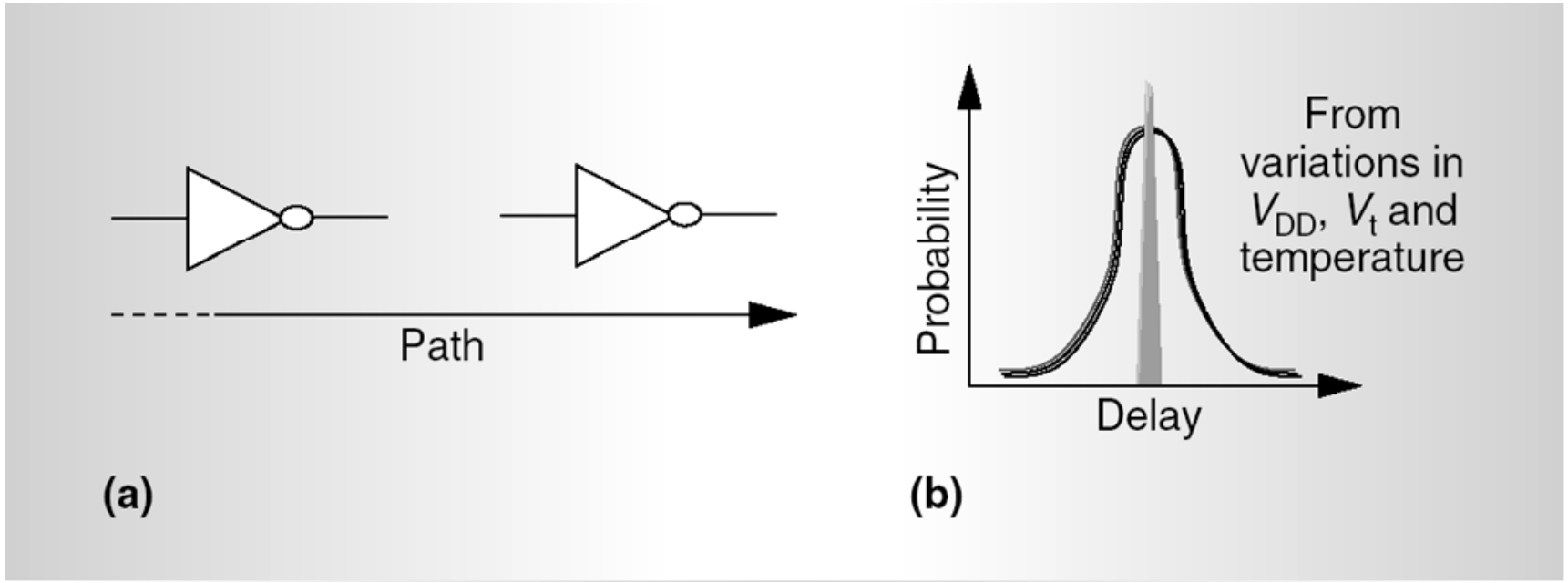


  - The heat flux across the die varies depending on the functionality of the circuit block
  - Higher heat flux puts more demand on the power distribution grid, resulting in resistive and inductive voltage drops, and creating time-dependant, dynamic, supply voltage variations

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Impact of Variations

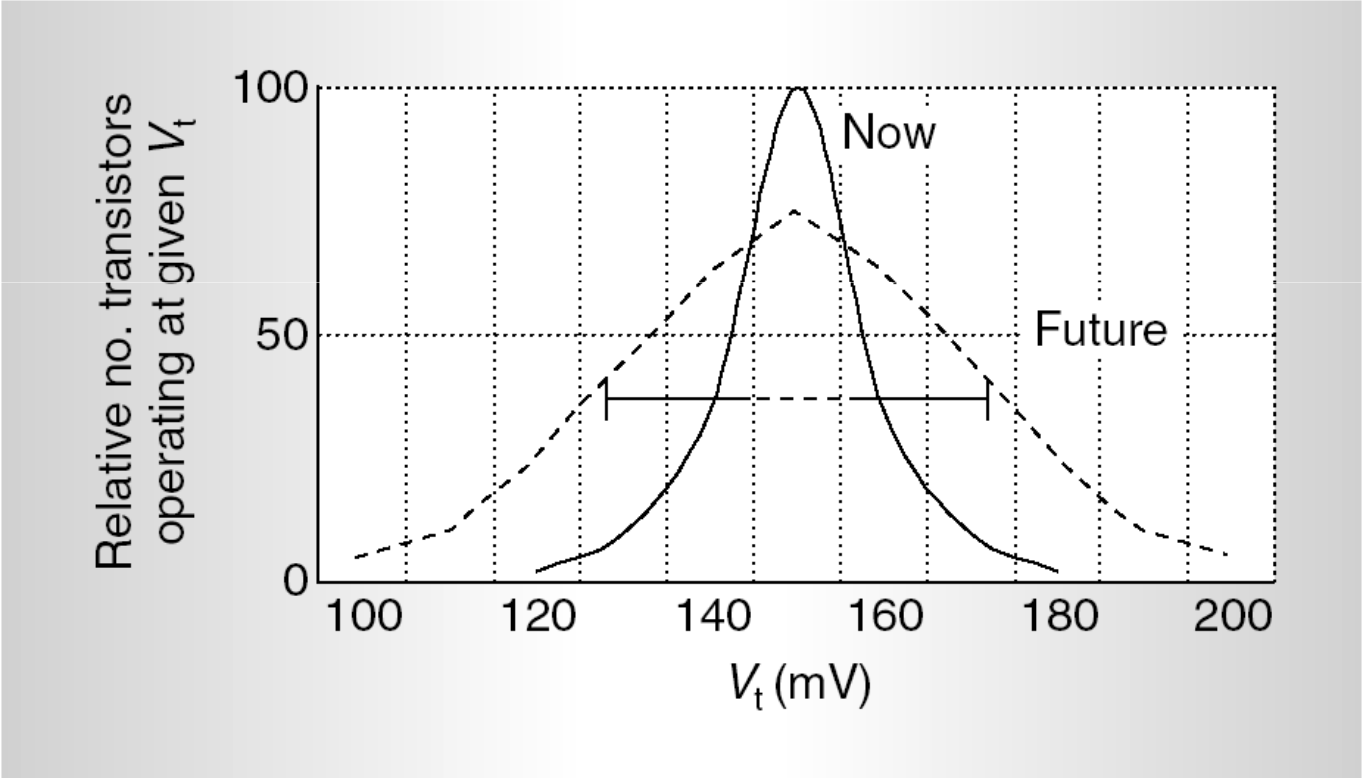
- Deterministic path delay & probabilistic path delay



Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Impact of Variations

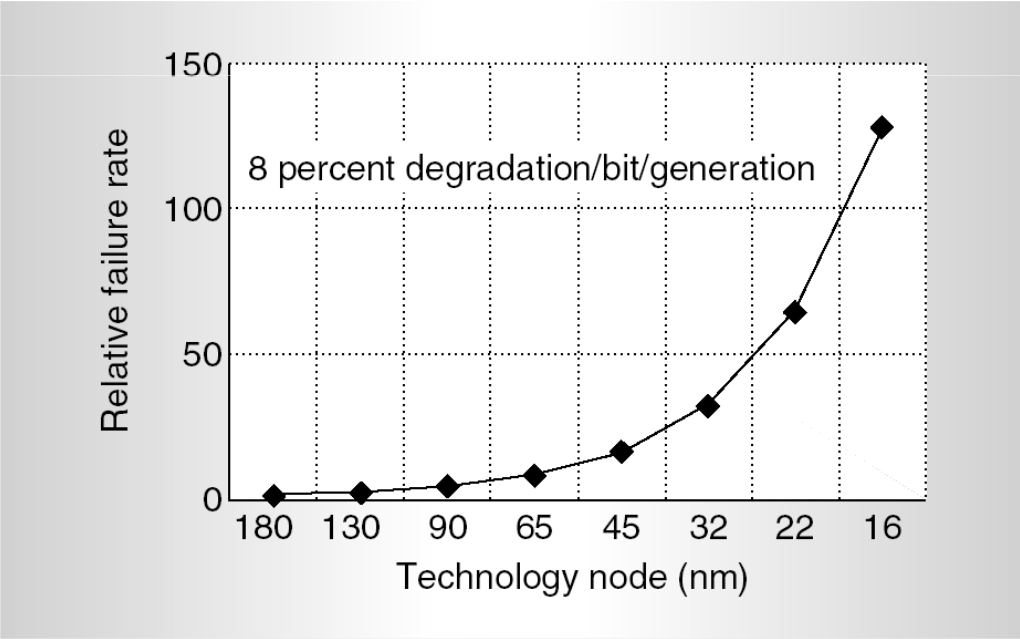
- Extreme device variations will become more typical in the future



Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Soft Error

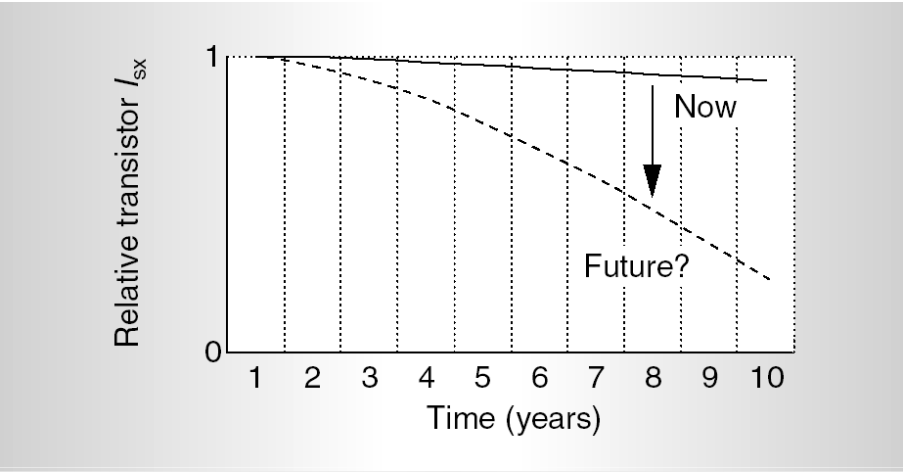
- Researcher expect about an 8 percent increase in soft-error rate per logic state bit each technology generation
- For example, soft-error failure-in-time of a chip (logic and memory)



Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Device Degradation

- Time-dependent device degradation



- Studies have shown that a transistor's saturation current degrades over years because of oxide wear out and hot-carrier degradation effects
- Researchers expect this degradation to become worse as we continue to scale transistor geometries beyond the 32-nm node. It might become so bad that it would be impractical to absorb degradation effects upfront in a system design

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

As Technology Scales Continuously

- Die size, chip yield, and design productivity have so far limited transistor integration in a VLSI design
- Now the focus has shifted to energy consumption, power dissipation, and power delivery
- As technology scales further we will face new challenges, such as variability, single-event upsets (soft errors), and device (transistor performance) degradation– these effects manifesting as inherent ***unreliability*** of the components, posing design and test challenges

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Possible Solution to Conquer Unreliability

- *The key to the reliability problem might be to exploit the abundance of transistors−use Moore's low to advantage. Instead of relying on higher and higher frequency of operation to deliver higher performance, a shift toward **parallelism** to deliver higher performance is in order, and thus **multi** might be the solution at all levels−from multiplicity of functional blocks to multiple processor cores in a system*

Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Possible Solution to Conquer Unreliability

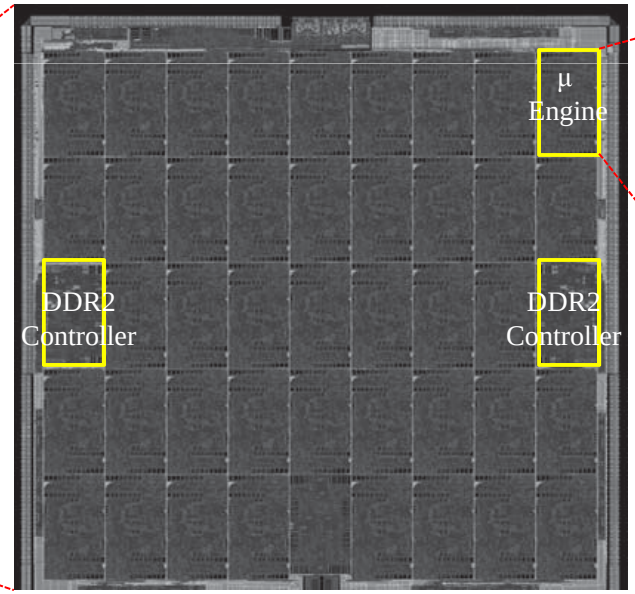
- *We could distribute test functionality as a part of the hardware to dynamically detect errors, or to correct and isolate aging and faulty hardware. Or a subset of cores in the multicore design could perform this work. This microarchitecture strategy, with multicores to assist in redundancy, is called* ***resilient microarchitecture****. It continuously detects errors, isolates faults, confines faults, reconfigures the hardware, and thus adapts. If we can make such a strategy work, there is no need for on-time factory testing, burn in, since the system is capable of testing and reconfiguring itself to make itself work reliably throughout its lifetime.*

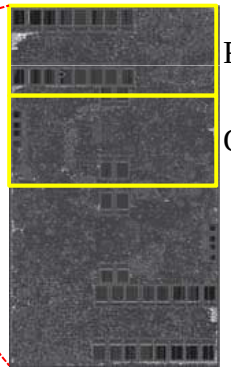
Source: S. Borkar (Intel Corp.), *IEEE Micro*, 2005

Architecture of Current SOC Chips

- Multi-core chip architecture
  - Use multiple identical cores to design a chip
- Network-on-chip communication infrastructure
  - Multiple point-to-point data links interconnected by switches (i.e., routers)

Source: IEEE Computer, 2005.

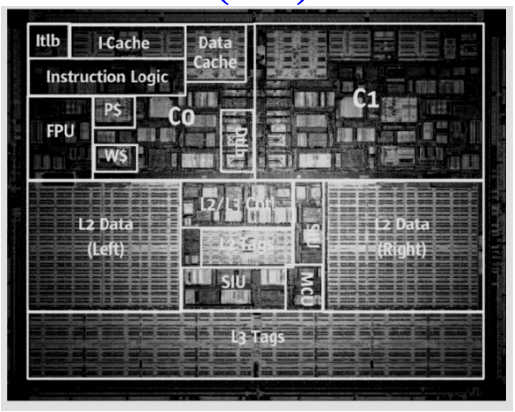




Source: IEEE Micro, 2007.

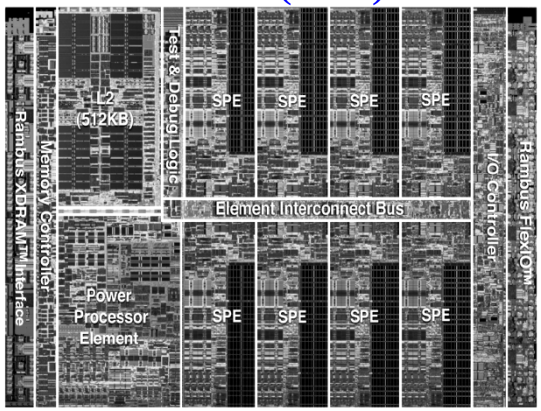
Examples

SPARC V9 (Sun)



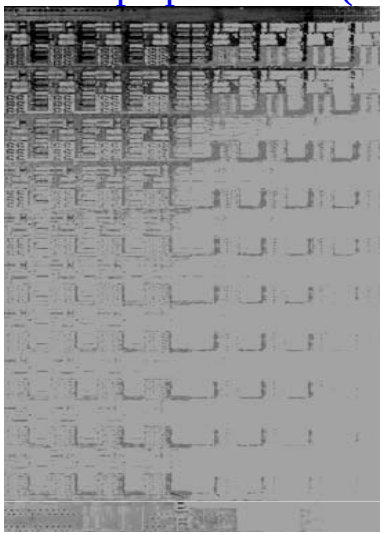
Source: IEEE JSSC, 2006.

Cell Processor (IBM)



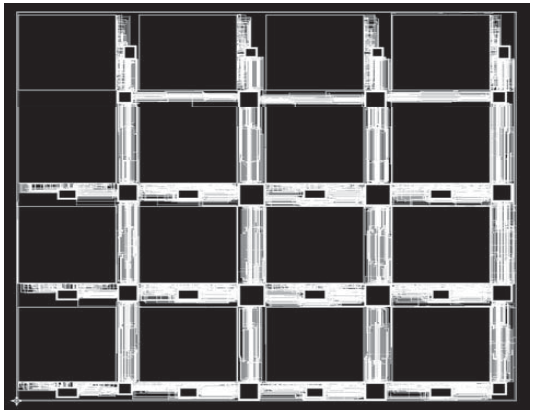
Source: IEEE JSSC, 2006.

Teraflops processor (Intel)



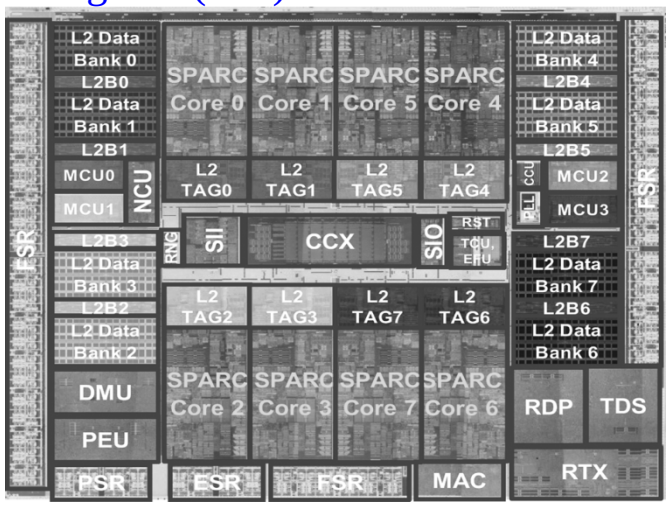
Source: IEEE Micro, 2007.

4x4 mesh built with Xpipes library components



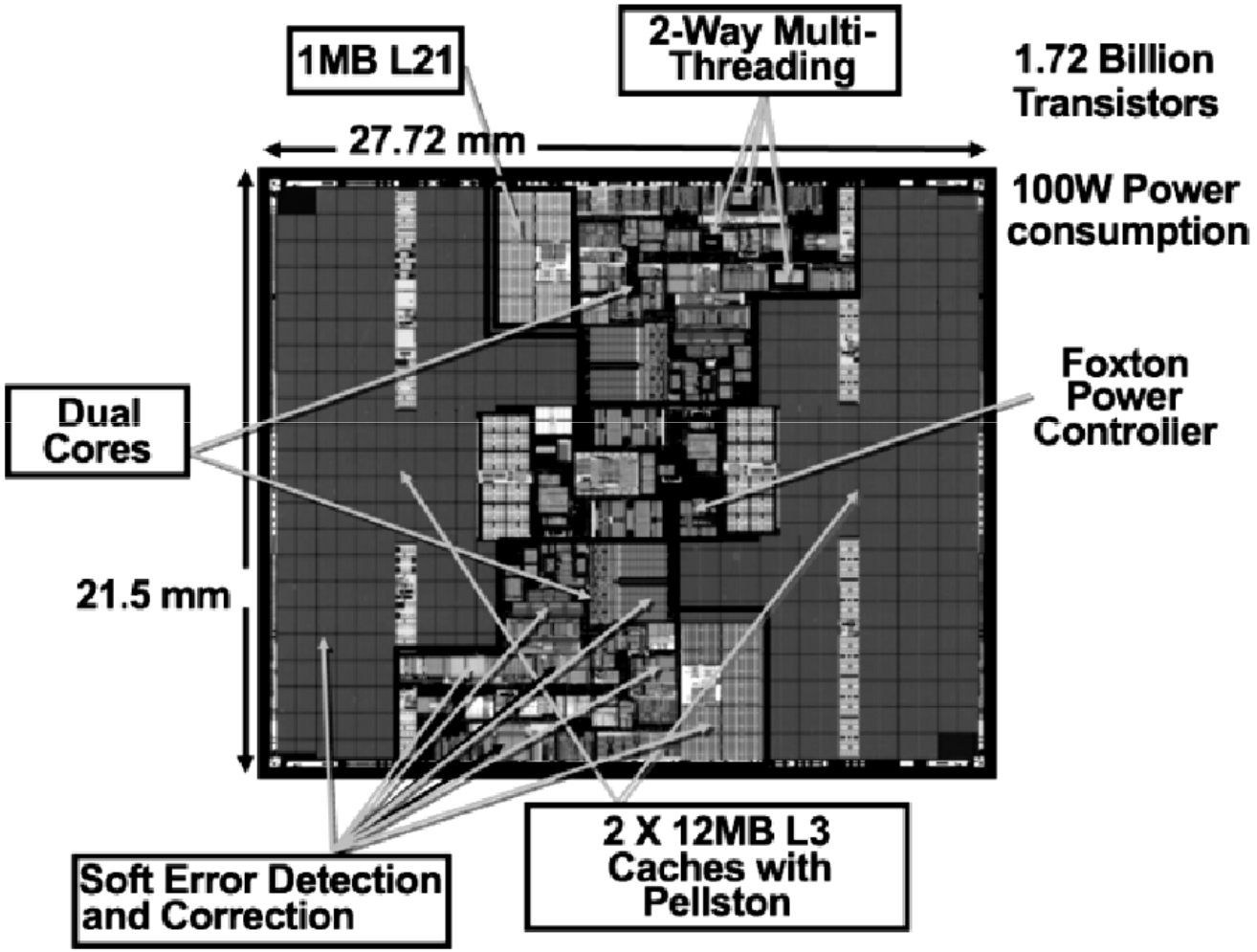
Source: IEEE Micro, 2007.

Niagara2 (Sun)

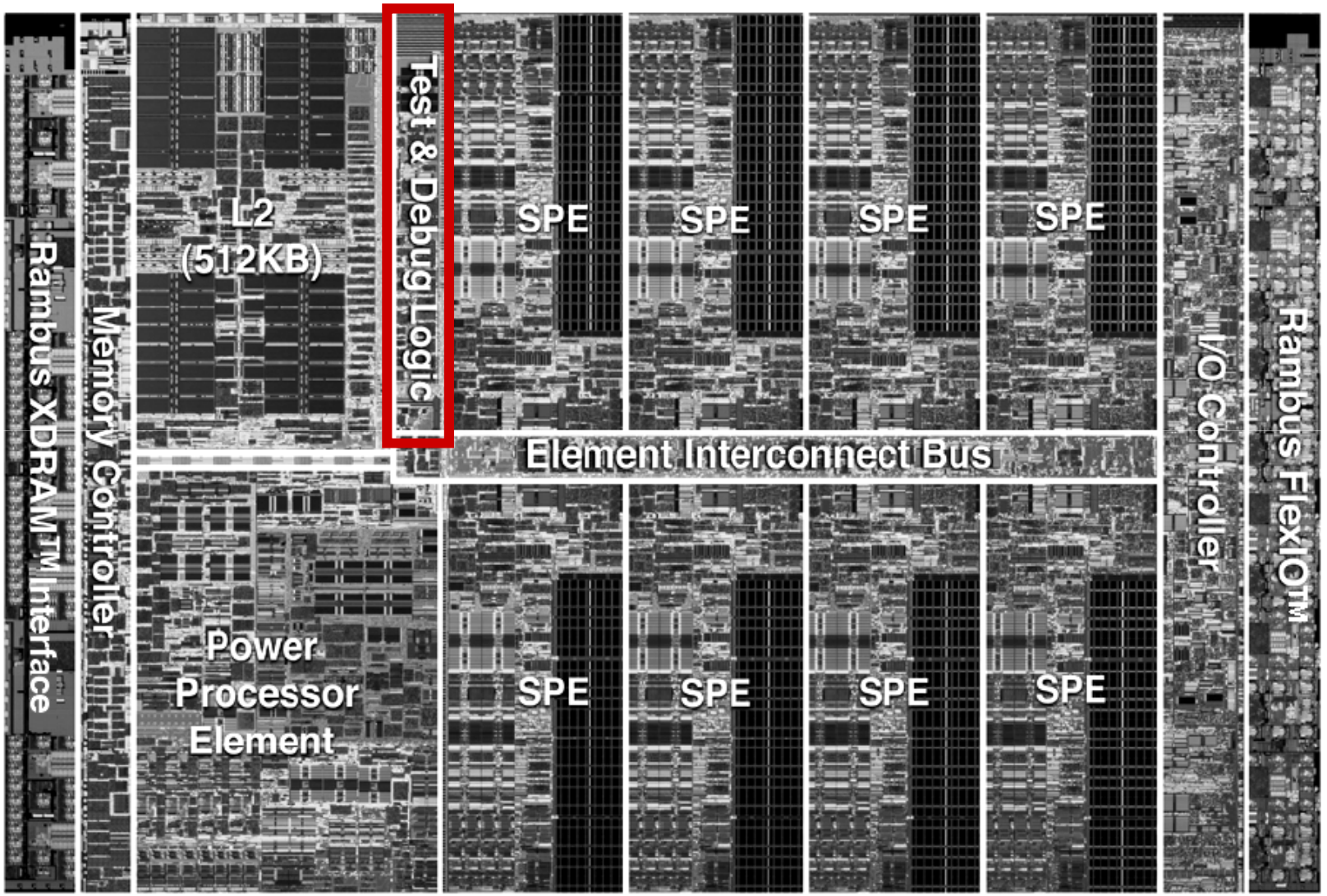


Source: IEEE JSSC, 2008.

Example: Itanium (JSSC, Jan. 2006)

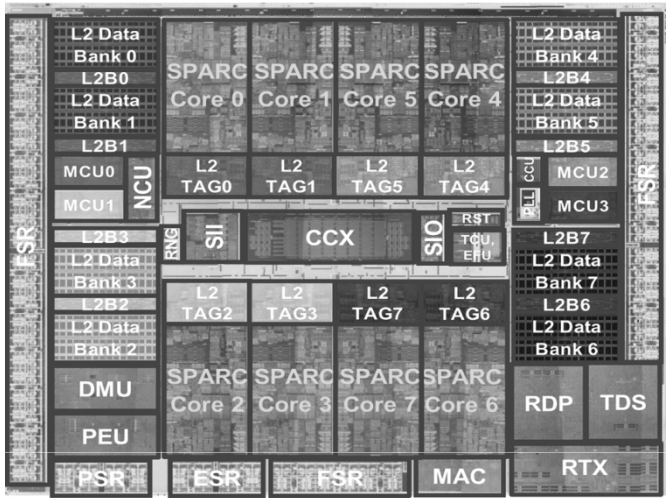


Cell Processor (JSSC, Jan. 2006)



Example: Niagara2 & POWER6 (JSSC, 2008)

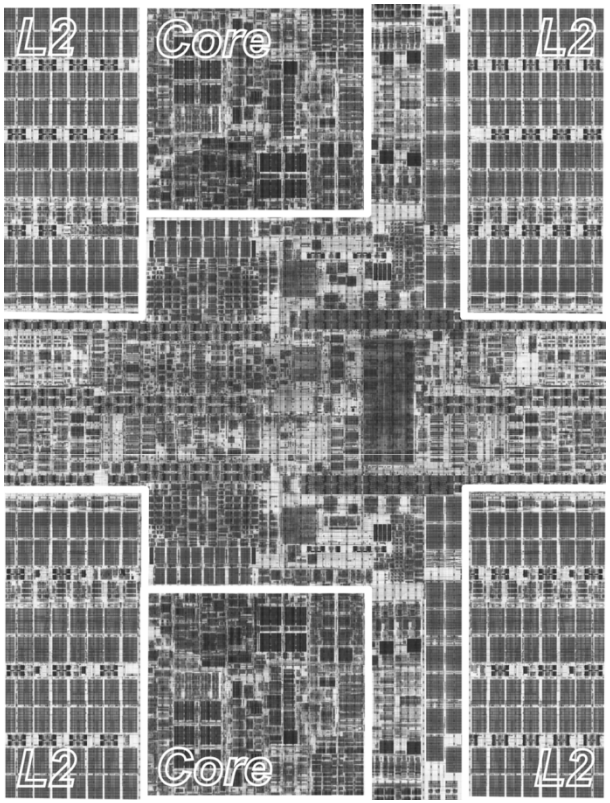
Niagara2 (Sun)



Design-for-Testability Features:

1. 32 Scans + ATPG
2. BIST for arrays
3. ….

POWER6 (IBM)

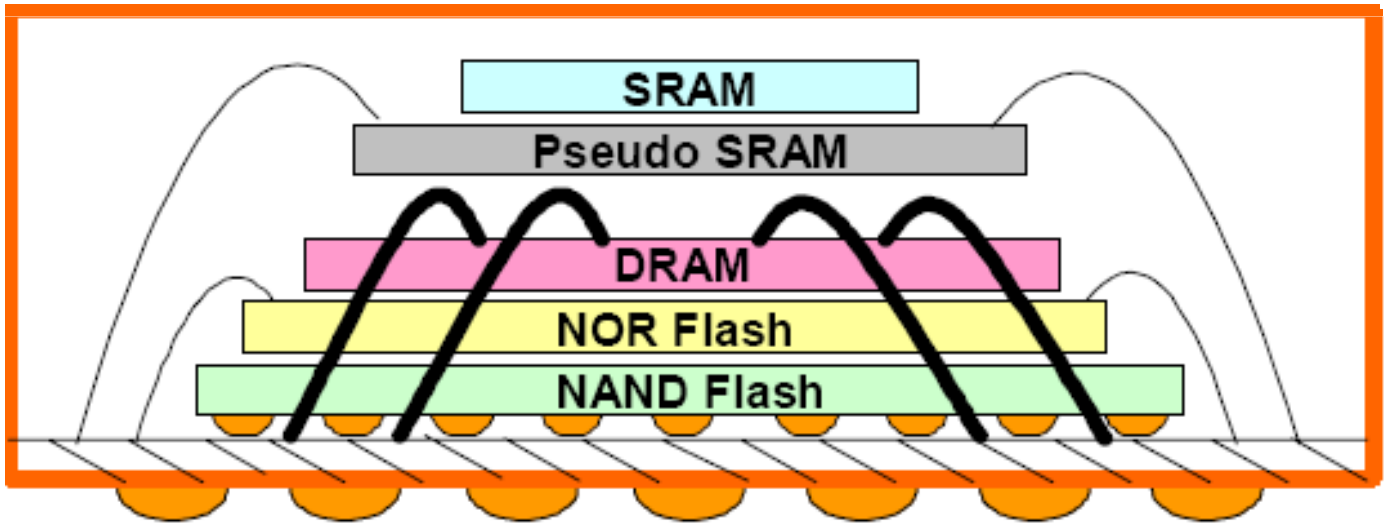


Design-for-Testability Features:

1. Logic BIST
2. BIST for arrays
3. BISR for arrays
4. …

3D-SiP: Next Technology/Architecture Transition?

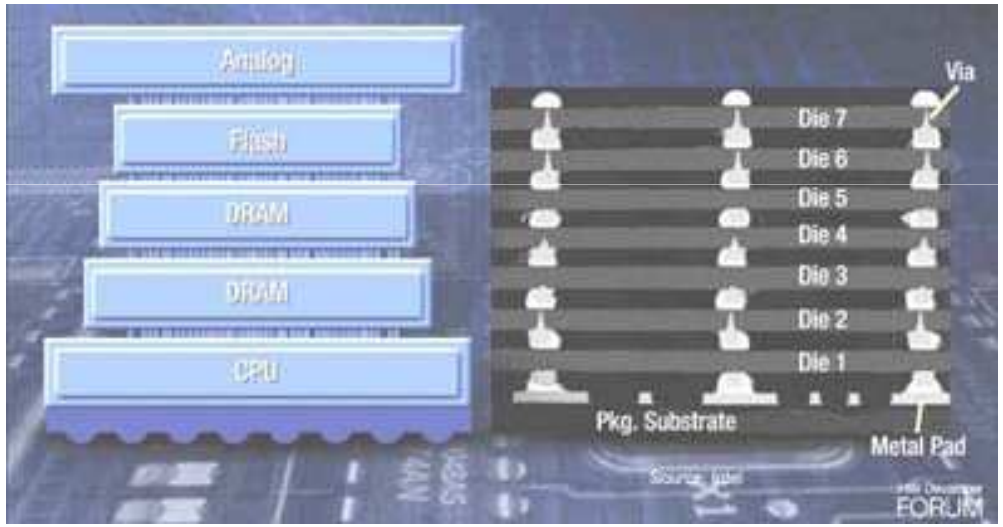
- Technology evolution
  - Bipolar → CMOS → Multicore → 3D integration + System-in-package (3D-SiP)
- System-in-package
  - stacking dies using bonding wires



Source: ISQED, 2008.

3D-SiP: Next Technology/Architecture Transition?

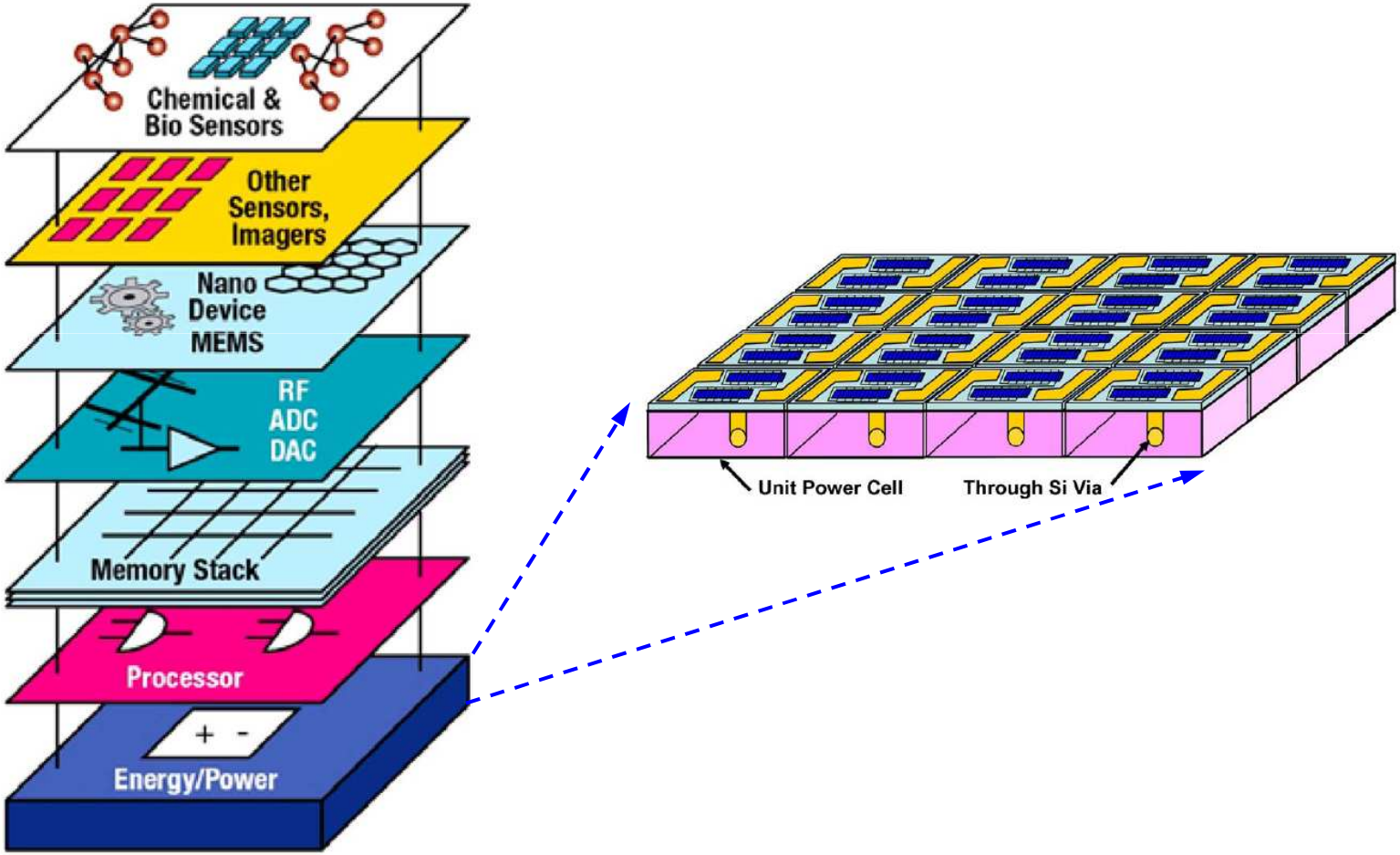
- 3D integration
  - stacking dies using through silicon via (TSV)



Source: IBM, 2008.

A New Paradigm for Future Technologies

- A vision of future 3-D hyperintegration of InfoTech, NanoTech, and BioTech systems



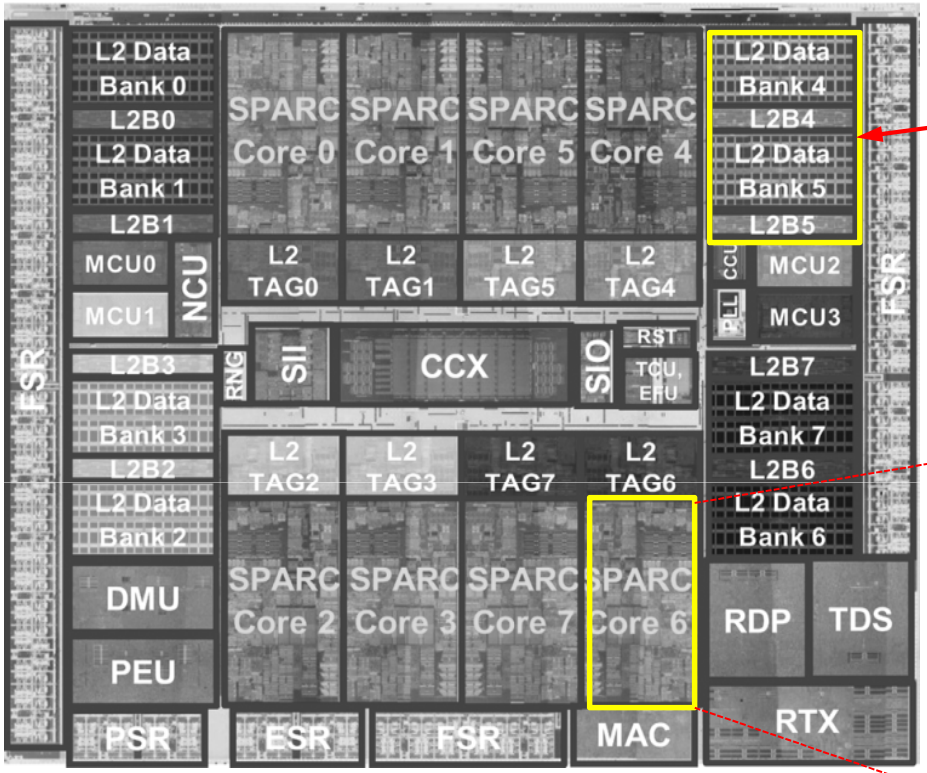
Source: Proceedings of IEEE, Jan. 2009

Challenges of 3D Implementations

- Yield
  - Design for resiliency
- Thermal
  - Can we overcome it?
- Test
- Reliability
- …

Source: IBM, 2008.

What will You Learn from This Course?



Source: IEEE JSSC, 2008.

Memory array

1. Controller
2. Datapath
3. Register File
4. Cache
5. …

Testing