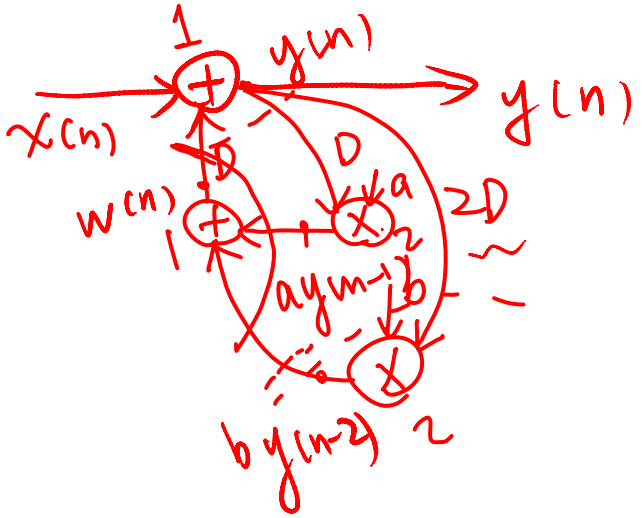
VLSI System Design

Jin-Fu Li
Advanced Reliable Systems (ARES) Laboratory
Department of Electrical Engineering
National Central University
Jhongli, Taiwan

Data flow graph (DFG)



3 time units

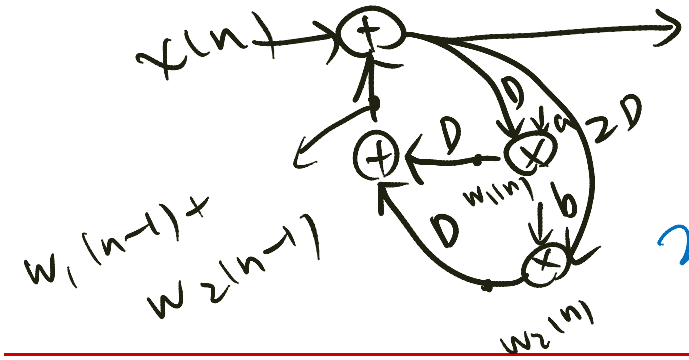
$y(n) = w(n-1) + x(n)$

$w(n) = a\,y(n-1) + b\,y(n-2)$

$y(n) = a\,y(n-2) + b\,y(n-3) + x(n)$

cutset ~~retiming~~

cutset



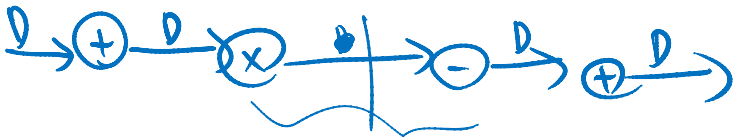
2 time units

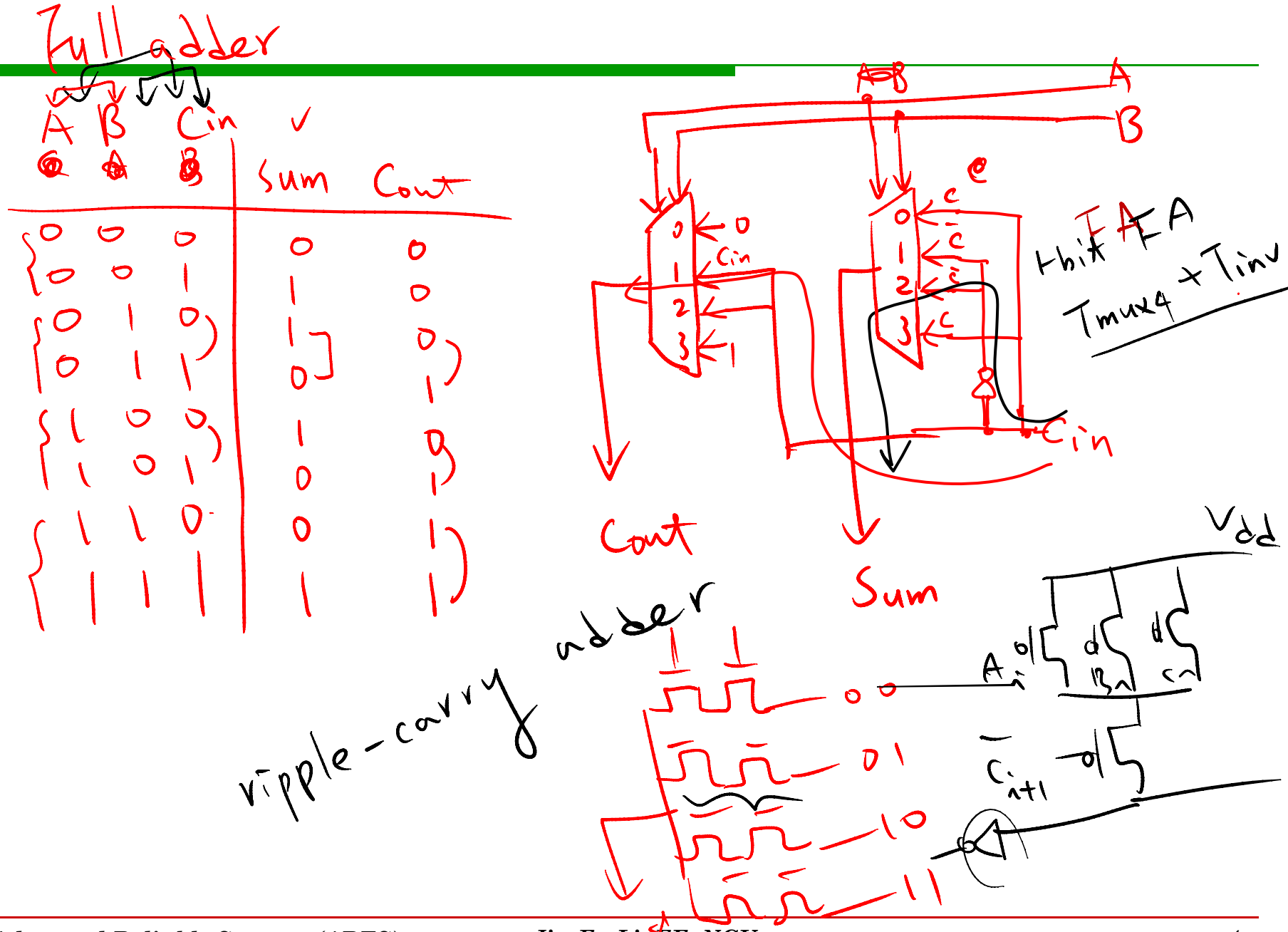
$w_1(n) = a\,y(n-1)$

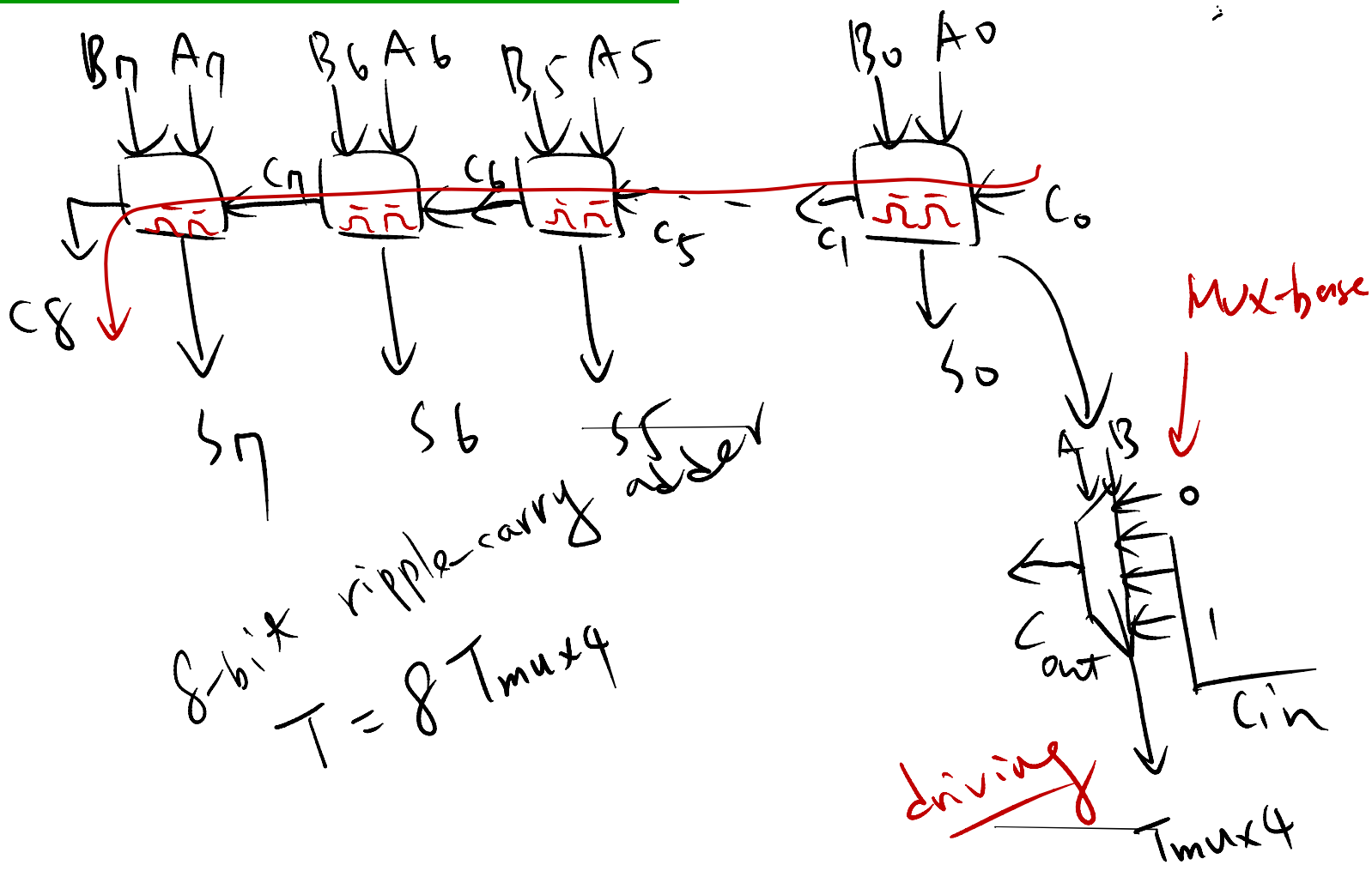
$w_2(n) = b\,y(n-2)$

$y(n) = w_1(n-1) + w_2(n-1) + x(n)$

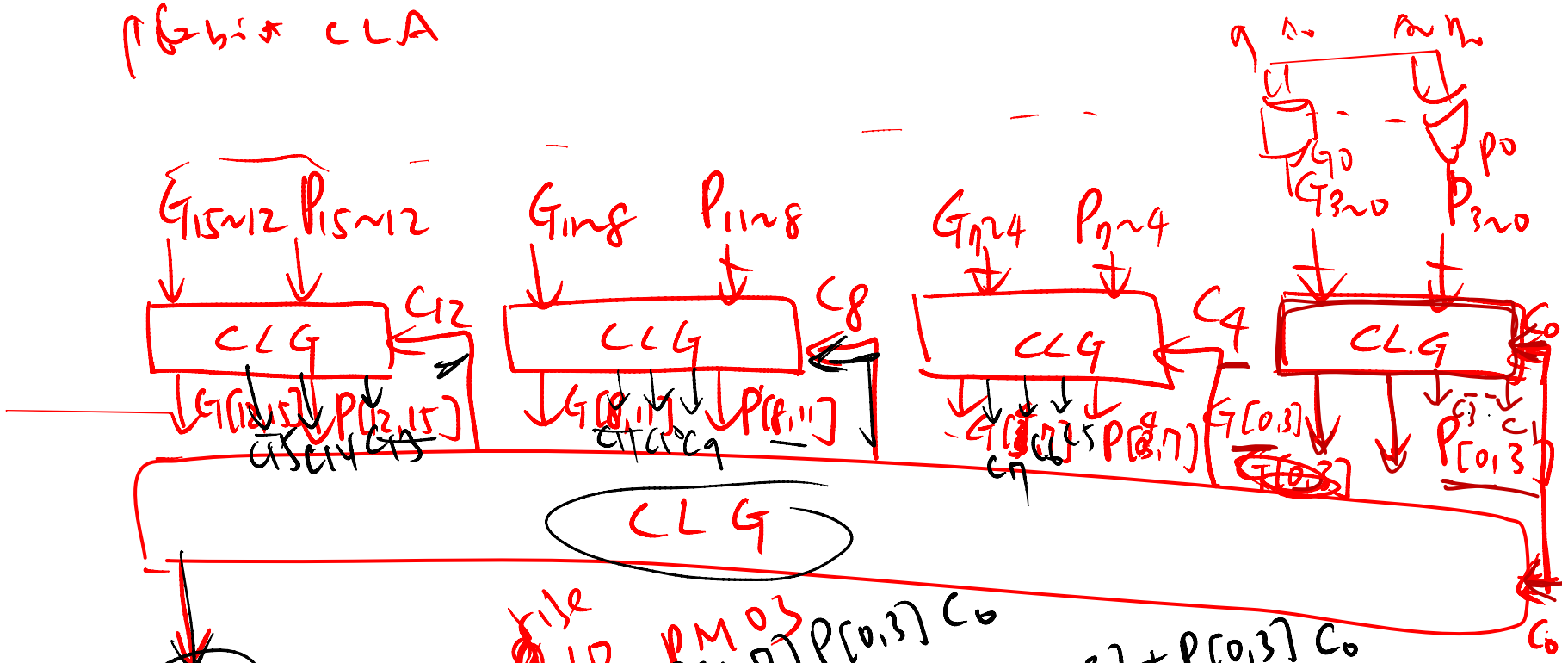
$= a\,y(n-2) + b\,y(n-3) + x(n)$


D
+
D
x
D
-
D
+
D


Full adder
A B Cin
Sum Cout
Cout
Sum
Cin
Vdd
Ai
Ci+1
ripple-carry adder
00
01
10
11
Thit FA
Tmux4 + Tinv


B7 A7
B6 A6
B5 A5
B0 A0
C7
C6
C5
C1
C0
C8
S7
S6
S0
8-bit ripple-carry adder
T = 8 Tmux4
Mux-base
A
B
0
1
Cout
Cin
driving
Tmux4

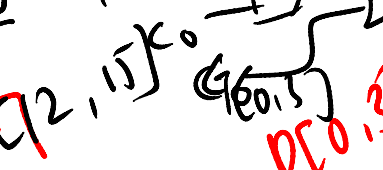
16-bit CLA



$C_8 = G[4,7] + G[0,3]P[4,7] + P[4,7]P[0,3]C_0$

$C_{16} = G[12,15] + G[8,11]P[12,15] + G[4,7]P[8,11]P[12,15] + G[0,3]P[4,7]P[8,11]P[12,15] + P[0,3]P[4,7]P[8,11]P[12,15]C_0$

$C_4 = G[0,3] + P[0,3]C_0$



16-bit CLA

$C_{i+1} = g_i + p_i C_i$ $\quad G(i, i+7)$ $\quad C_4 = G(0,7) + P(0,7) C_0$

$C_8 = G(4,7) + G(0,3) P(4,7) + P(4,7) P(0,3) C_0$

$= P_4 P_5 P_6 P_7$

$C_1 = g_0 + p_0 C_0$

$C_2 = g_1 + g_0 p_1 + p_0 p_1 C_0$

$C_3 = g_2 + g_1 p_2 + g_0 p_1 p_2 + p_0 p_1 p_2 C_0$

$C_4 = [g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3] + [p_0 p_1 p_2 p_3 C_0]$

$G(0,3)$ $\quad P(0,3)$

$C_5 = g_4 + g_3 p_4 + g_2 p_3 p_4 + g_1 p_2 p_3 p_4 + g_0 p_1 p_2 p_3 p_4 + p_0 p_1 p_2 p_4 C_0$

$C_6 = g_5 + g_4 p_5 + g_3 p_4 p_5 + g_2 p_3 p_4 p_5 + g_1 p_2 p_3 p_4 p_5 + g_0 p_1 p_2 \cdots p_5$

$+ p_0 p_1 \cdots p_5 C_0$

$C_7 = g_6 + g_5 p_6 + g_4 p_5 p_6 + g_3 p_4 p_5 p_6 + g_2 p_3 p_4 p_5 p_6 + g_1 p_2 p_6$

$+ g_0 p_1 p_2 p_6 + p_0 p_1 \cdots p_6 C_0$

$C_8 = [g_7 + g_6 p_7 + g_5 p_6 p_7 + g_4 p_5 p_6 p_7] + [g_3 p_4 p_5 p_6 p_7 + g_2 p_3 p_4 p_5 p_6 p_7$

$+ g_1 p_2 p_3 p_4 p_5 p_6 p_7 + g_0 p_1 p_2 \cdots p_7] + p_0 \cdots p_7 C_0$

$G(4,7)$ $\quad G(0,3) P(4,7)$

$$C_1 = g_0 + p_0 c_0$$

$$C_2 = g_1 + g_0 p_1 + p_0 p_1 c_0$$

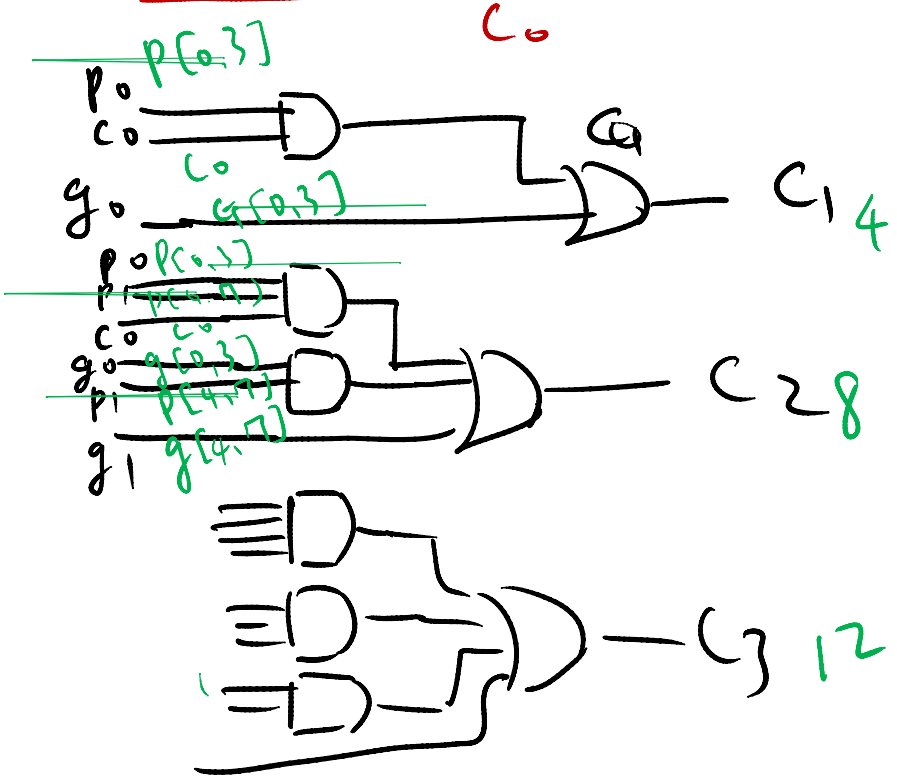
$$C_3 = g_2 + g_1 p_2 + g_0 p_1 p_2 + p_0 p_1 p_2 c_0$$

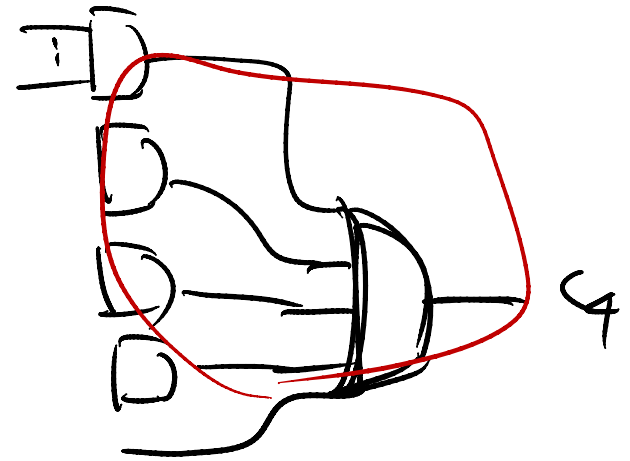
$$C_4 = [g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3] + [p_0 p_1 p_2 p_3] c_0$$

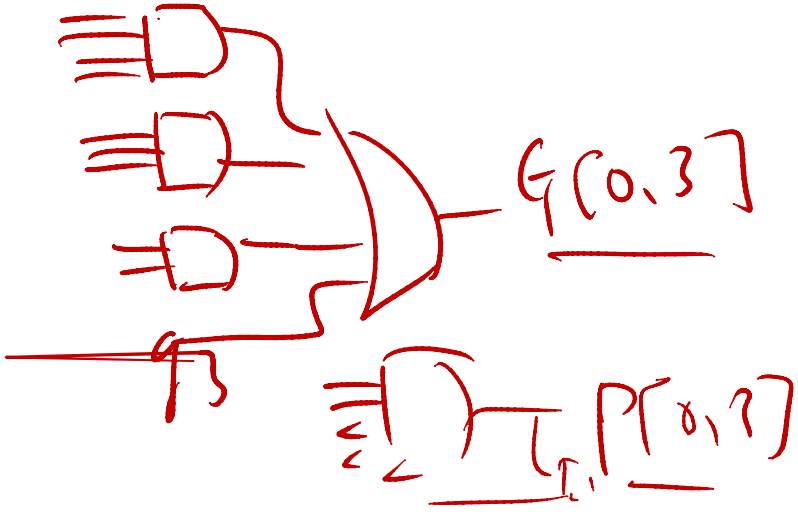
$G[0,3]$ $\quad P[0,3]$ $\quad C_0$

$p_i = A_i \oplus B_i$

$g_i = A_i B_i$



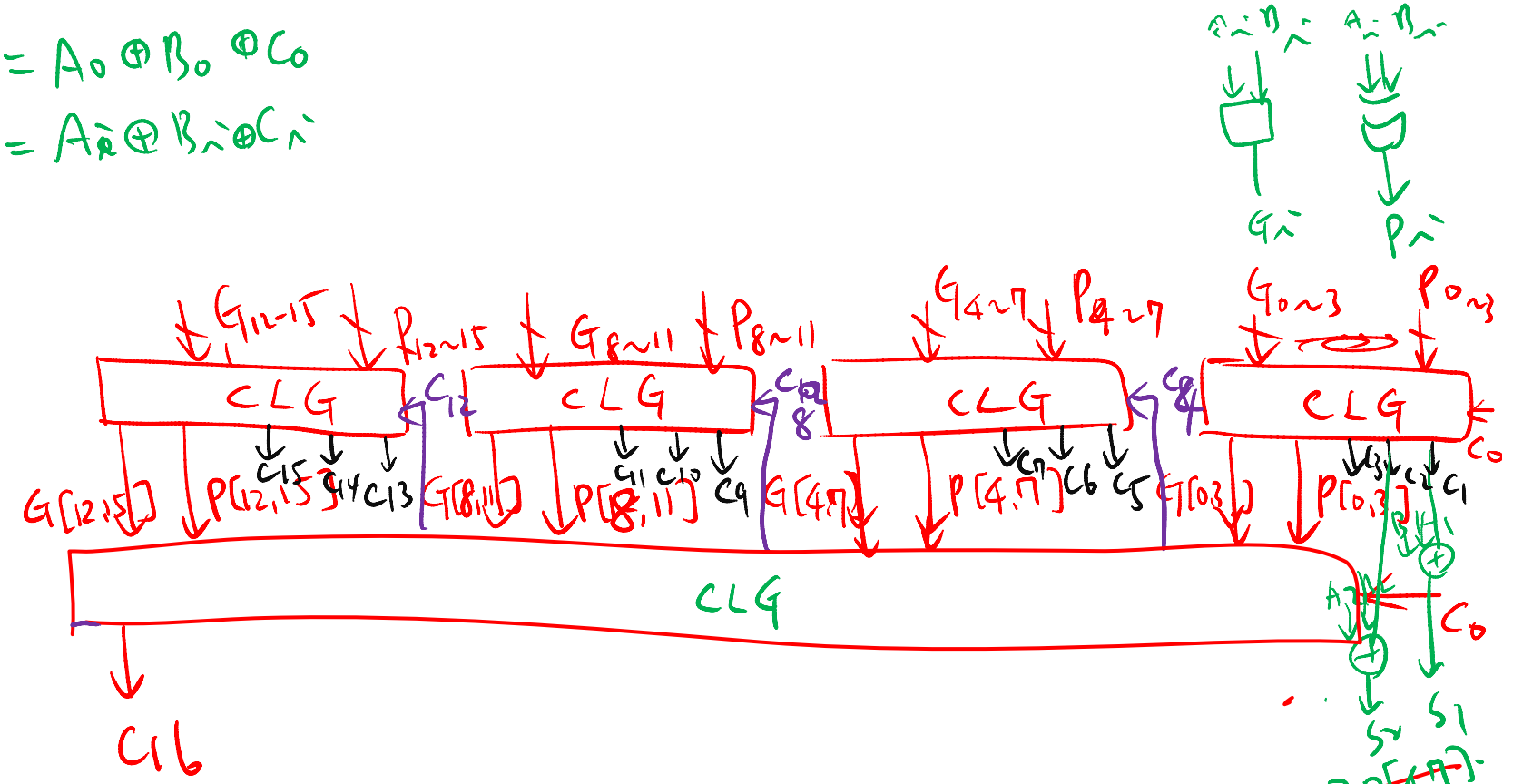




C16

$S_0 = A_0 \oplus B_0 \oplus C_0$

$S_i = A_i \oplus B_i \oplus C_i$



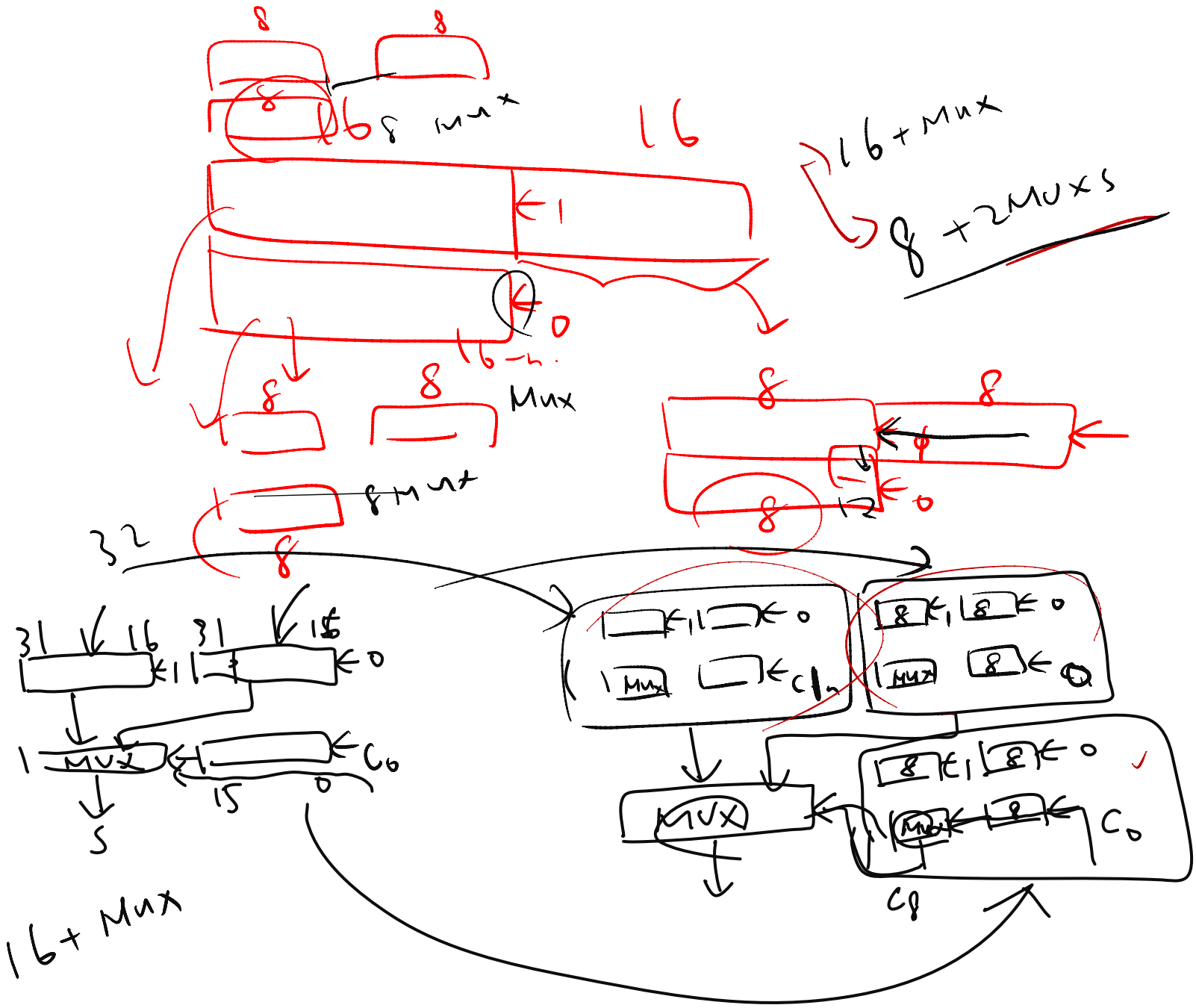
$G[0,3] = g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3$

$p[0,3] = p_0 p_1 p_2 p_3$

$C_{16} = G[12,15] + G[8,11]P[12,15] + G[4,7]P[8,11]P[12,15] + \cancel{G[0,3]P[4,7]}$

$+ G[0,3]P[4,7]P[8,11]P[12,15] + \cancel{\quad}$

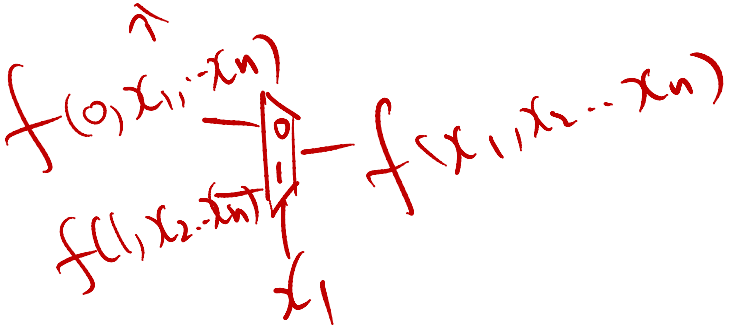
$P(0,3) \cdots P[12,15]C_0$


8
8
8 mux
16
1
0
16-n
Mux
16+Mux
8+2Muxs
8
8
8 mux
8
8
12
0
32
31
16
31
15
1
0
1
MUX
C0
15
0
S
16+Mux
MUX
Cn
MUX
C8
C0

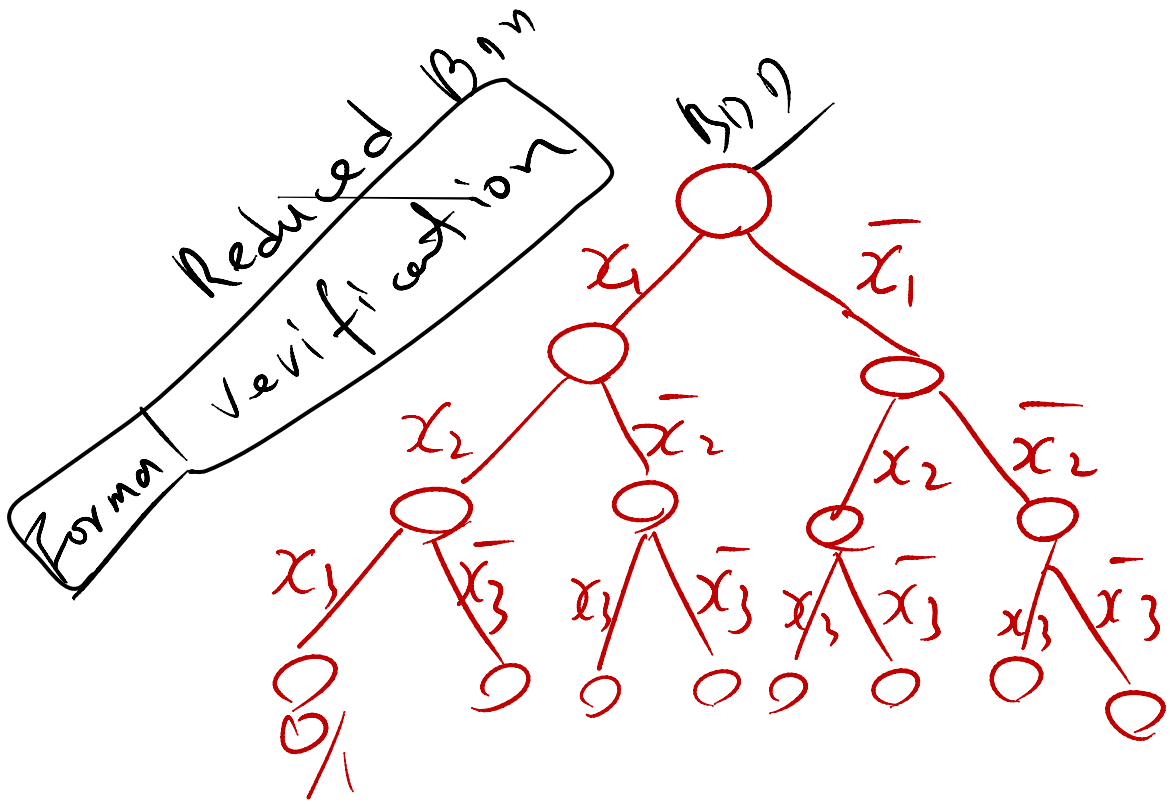
Shannon Expansion → BDD (Binary Decision Diagram)

$$f(x_1, x_2, \cdots x_n) = x_1 f(1, x_2, \cdots x_n) + \bar{x}_1 f(0, x_2, \cdots x_n)$$

$$= x_1 [x_2 f(1,1,\cdots x_n) + \bar{x}_2 f(1,0,\cdots x_n)] +$$
$$\bar{x}_1 [x_2 f(0,1,\cdots x_n) + \bar{x}_2 f(0,0,\cdots x_n)]$$

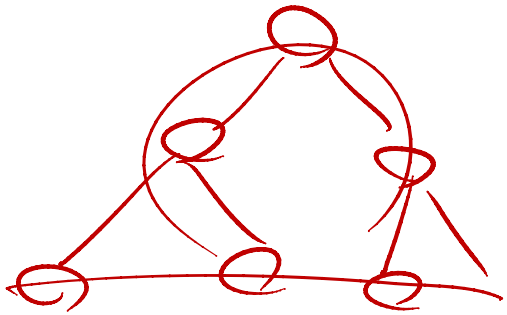


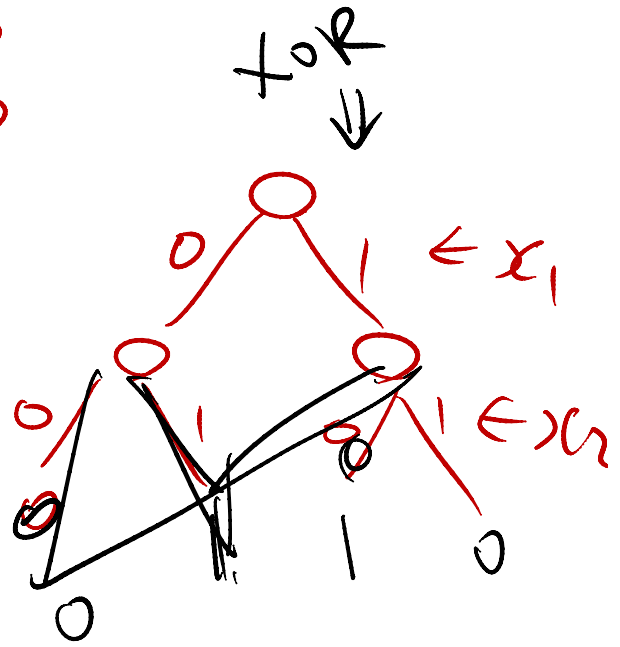
LUT + Mux + FFs



$$f(x_1, x_2) = x_1 \bar{x}_2 + \bar{x}_1 x_2$$

BDD

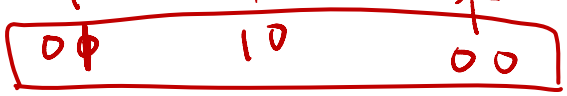




Ternary CAM cell

"0" or "1" or "X"

don't care



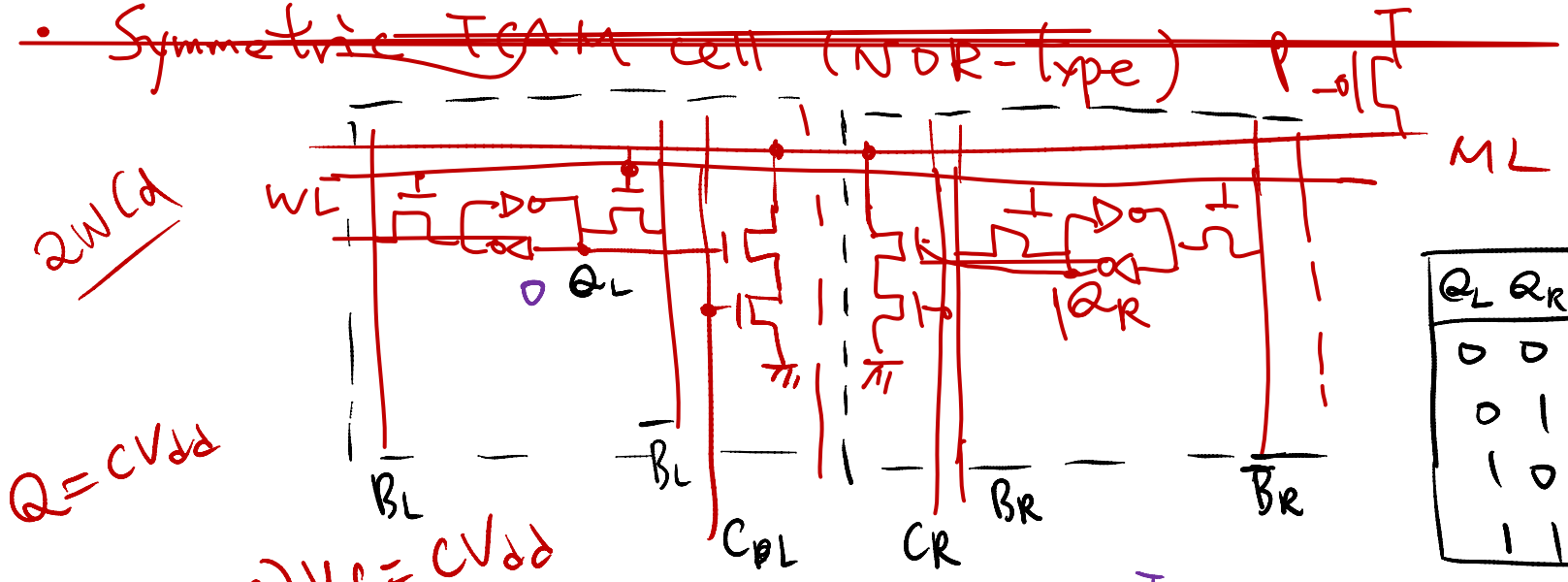
Binary CAM cell

"0" or "1"

TCAM cell depends on the cell structure

⇒ Symmetric TCAM cell ~~& Asymmetric~~ TCAM cell

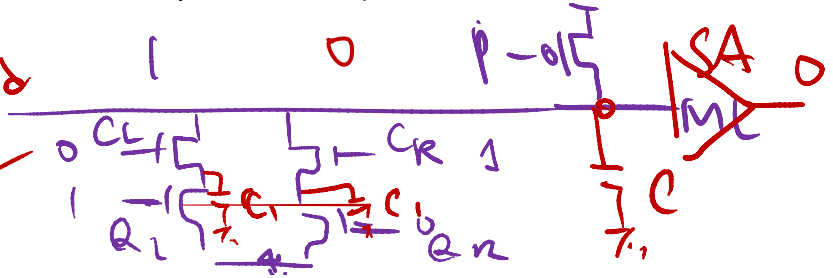
~~• Symmetric TCAM cell (NOR-type)~~



Q_L	Q_R	Ternary State
0	0	X
0	1	0
1	0	1
1	1	illegal

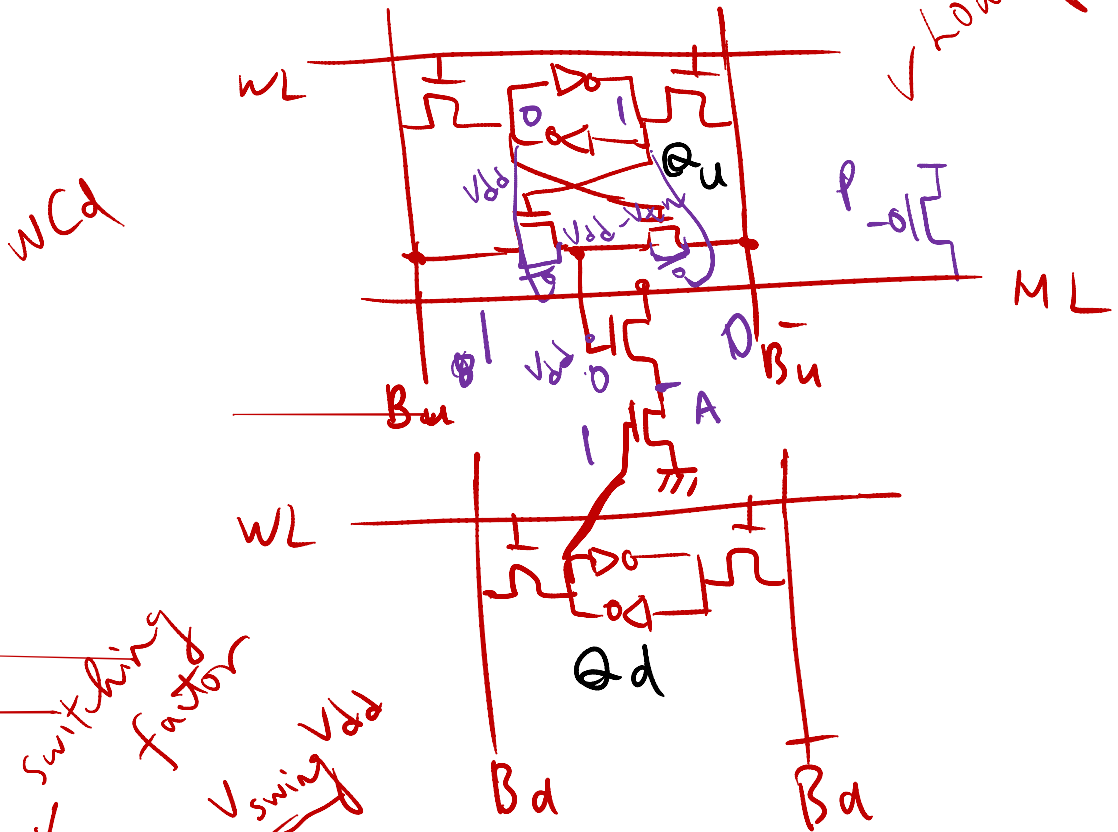
$(WC_1+C)V_f = CV_{dd}$

$V_f = \frac{C}{WC_1+C} V_{dd}$

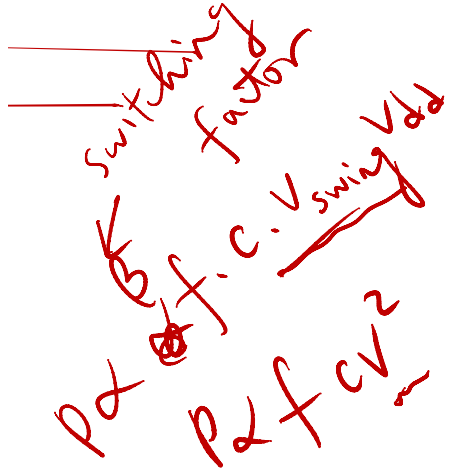


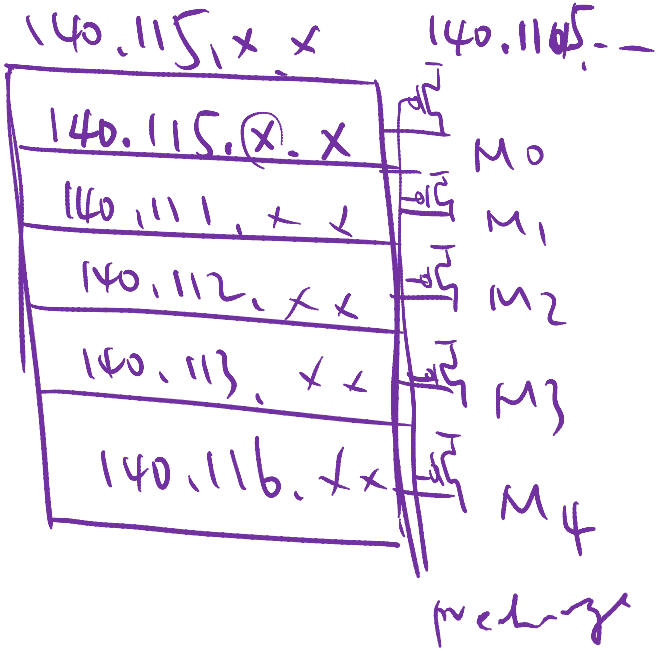
C_L	C_R	
0	0	X
0	1	1
1	0	0
1	1	illegal

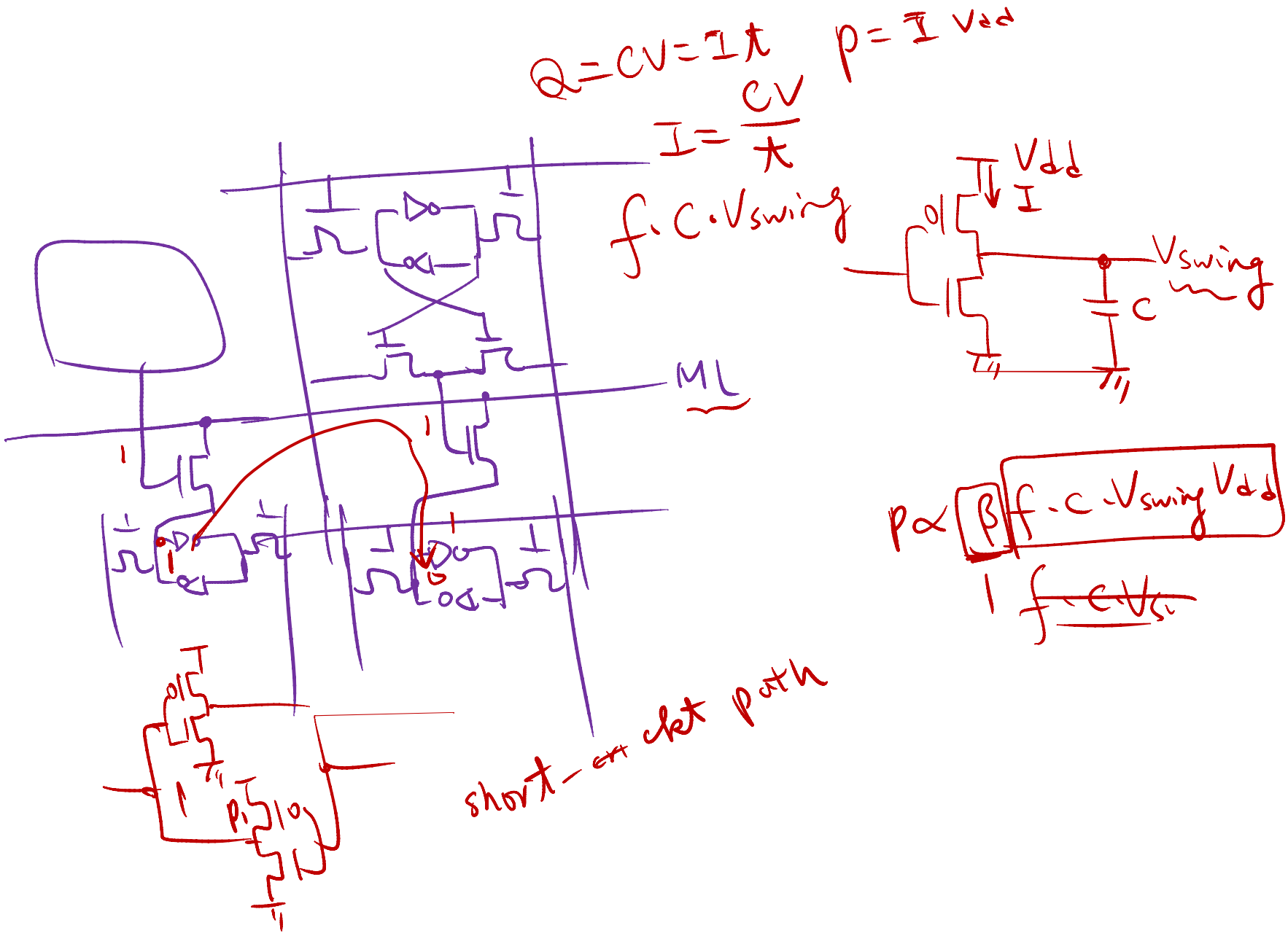
Asymmetric TCAM cell (NOR-type)

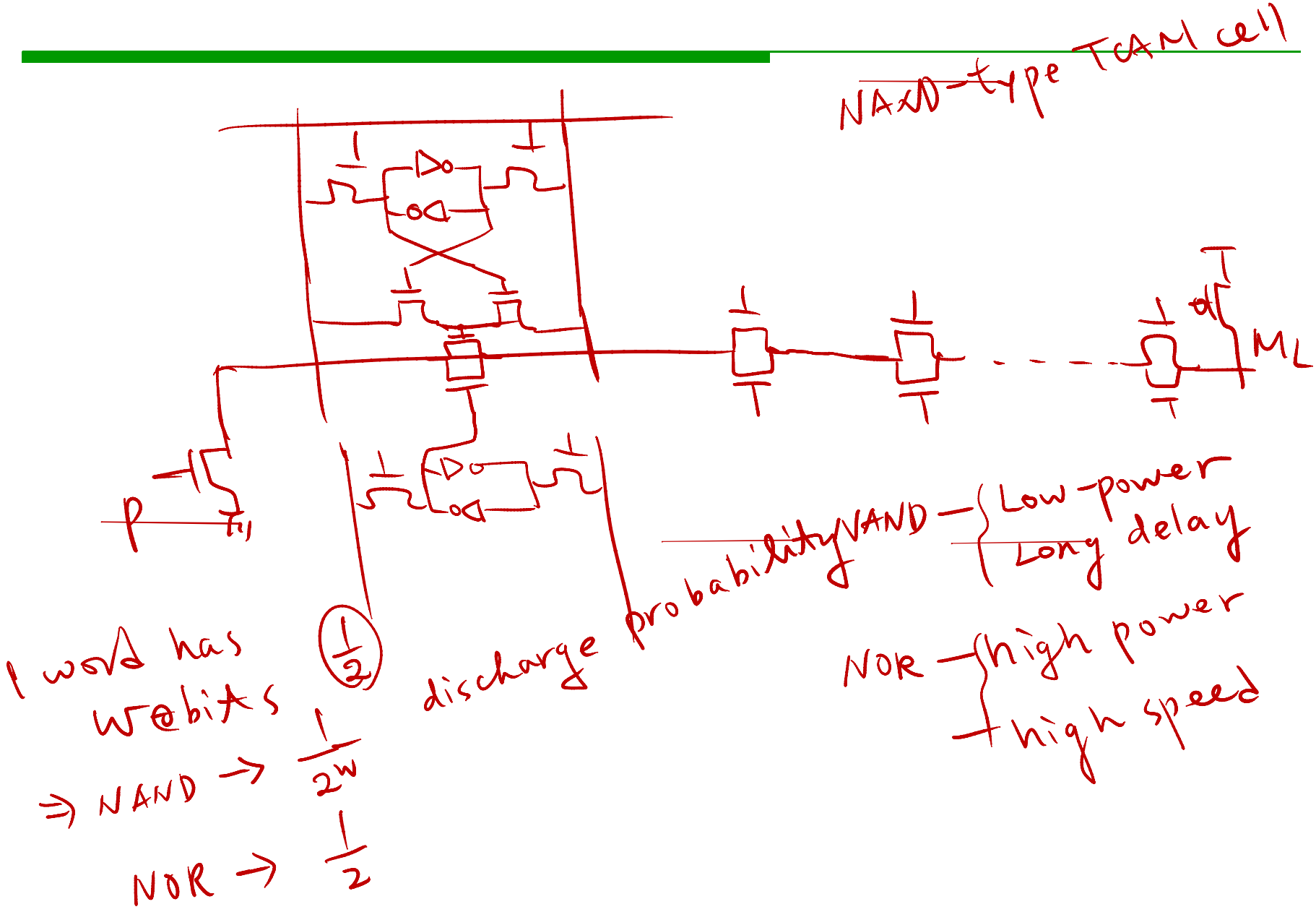


Qu	Qd	ternary state
0/1	0	X
0	1	0
1	1	1






Q=CV=It
I=CV/t
P=I Vdd
f.C.Vswing
Vdd
I
Vswing
C
ML
short-ckt path


NAND-type TCAM cell
ML
P
Fi
1 word has w@bits
⇒ NAND → 1/2w
NOR → 1/2
1/2
discharge probability
NAND → Low power
Long delay
NOR → high power
high speed

NOR/NAND Match Line Structure (BCAM)