Training Course of SOC Encounter

REF:

- CIC Training Manual Cell-Based IC Physical Design and Verification with SOC Encounter, July, 2006
- CIC Training Manual Mixed-Signal IC Design Concepts, July, 2007

Speaker: K. –T. Wu



Outline

- Basic Concept of the Placement & Routing
- Auto Place and Route Using SOC Encounter
- LAB

BASIC CONCEPT OF THE PLACEMENT & ROUTING

Cell-Based Design Flow



Advanced Reliable Systems (ARES) Lab.

SOC Encounter P&R Flow



IO, Power/Ground Placement



Specify Floorplan

- Determine the aspect ratio of the Core
- Determine the gap between the PAD and Core
 - The Core Utilization is determined in this step
 - The final CHIP area is almost determined in this step



Floorplan

- Determine the related positions of Hard Blocks
 - The performance is highly affected



Amoeba Placement

 Observe the result of cells and Hard Blocks placement



Power Planning



Clock Tree Synthesis



Power Analysis

IR-drop & electron migration



Power Route

Connect the power pins of standard cells to the global power lines



Add IO Filler

- Fill the gap betweenPADs
 - Connect the PAD power rings



Routing

Construct the final interconnections



Prepare Data

- Library
 - Physical Library (LEF)
 - Information of technology, standard cells, Hard Blocks, and APR
 - Timing Library (LIB)
 - Timing information of the standard cells and Hard Blocks
 - Capacitance Table
 - For more accurate RC analysis
 - Celtic Library
 - For crosstalk analysis
 - FireIce/Voltage Storm Library
 - For RC extraction and power analysis
- User Data
 - Gate-Level Netlist (Verilog)
 - SDC Constraint (*.sdc)
 - IO Constraint (*.ioc)

Not Necessary !

LEF Format – Process Technology

Layers
POLY
Contact
Metal 1

🔷 Via1

Metal 2

Design Rule

Net Width Net Spacing Area Enclosure Wide Metal Slot Antenna Current Density

Parasitic

Resistance Capacitance

LEF Format – Process Technology

Layer Define





- Unit
- □ Site
- Routing Pitch
- Default Direction
- Via Rule

□ Site

The placement site gives the placement grid of a family of macros







\backslash	$ \rangle$		$\left \right\rangle$	VDD
		-		
				VSS

- **D** Routing Pitch
- Default Direction



□ Via Generation

- To connect the wide metal, a via array is generated to reduce the via resistance
- Formulas for generating via arrays are defined



□ Same Net Spacing

SPACING

SAMENET Metal1 Metal1 0.23; SAMENET Metal2 Metal2 0.28 STACK; SAMENET Metal3 Metal3 0.28; SAMENET VIA12 VIA12 0.26; SAMENET VIA23 VIA23 0.26; SAMENET VIA12 VIA23 0.0 STACK; END SPACING



VIA12 and VIA23 allow stack



Physical Macros

- Define physical data for
 - Standard cells
 - I/O pads
 - Memories
 - Other hard macros
- Describe abstract shape
 - Size
 - Class
 - Pins
 - Obstructions



MACRO ADD1 CLASS CORE; **FOREIGN ADD1 0.0 0.0; ORIGEN** 0.0 0.0; LEQ ADD; SIZE 19.8 BY 6.4; SYMMETRY x y; SITE coresite; **PIN A DIRECTION INPUT;** PORT LAYER Metal1; RECT 19.2 8.2 19.5 10.3; END END A **END ADD1**

LIB Format

- Operating condition
 - Slow, fast, typical
- Pin type
 - Input/output/inout
 - Function
 - Data/clock
 - Capacitance
- Path delay
- □ Timing constraint
 - Setup, hold, mpwh, mpwl, recovery

Gate-Level Netlist

- If designing a chip, IO PADs, power PADs, and Corner PADs should be added before the netlist is imported
- Make sure that there is no "assign" statement and no "*cell*" cell name in the netlist

SDC Constraint

- Clock constraints
- Input delay/ Input drive
- Output delay/ Output load
- □ False path
- Multi-cycle path

IO Constraint

Version: 1	
Pad: CORNER0	NW PCORNERDGZ
Pad: PAD_CLK	Ν
Pad: PAD_HALT	Ν
Pad: CORNER1	NE PCORNERDGZ
Pad: PAD_X1	W
Pad: PAD_X2	W
Pad: CORNER2	SW PCORNERDGZ
Pad: PAD_IOVDD1	S PVDD2DGZ
Pad: PAD_IOVSS1	S PVSS2DGZ
Pad: CORNER3	SE PCORNERDGZ
Pad: PAD_VDD1	E PVDD1DGZ
Pad: PAD_VSS1	E PVSS1DGZ



(*.ioc File)

Advanced Reliable Systems (ARES) Lab.

Decide the NO. of Power/Ground PADs

- □ The following factors are considered:
 - SSO: Simultaneously Switch Outputs
 - SSN: The noise produced by SSO buffers
 - DI: Maximum NO. of copies for one specific kind of IO PAD switching from high to low simultaneously without making ground voltage level higher than 0.8 volt for one ground PAD
 - DF: Driving Factor, DF = 1/DI
 - SDF: Sum of Driving Factor
- □ Suggestion in SSO case:
 - Required NO. of ground PADs = SDF
 - Required NO. of power PADs = SDF/1.1

SDF Example

- □ If a design has 20 PDB02DGZ (2mA) and 10 PDD16DGZ (16mA). Then,
- **SDF** = $20 \times 0.02 + 10 \times 0.3 = 3.4$
- □ In SSO case,
 - NO. of VSS PAD = $3.4 \rightarrow 4$
 - NO. of VDD PAD = $3.4/1.1 = 3.09 \rightarrow 4$

Ю Туре	2mA	4mA	8mA	12mA	16mA	24mA
DF Value	0.02	0.03	0.09	0.18	0.3	0.56

Tips to Reduce the Power/Ground Bounce

- Don't use stronger output buffers than what is necessary
- □ Use slew-rate controlled outputs
- Place power pad near the middle of the output buffer
- Place noise sensitive I/O pads away from SSO I/Os
- Place VDD and VSS pads next to clock input buffer

AUTO PLACE AND ROUTE USING SOC ENCOUNTER

CHIP-Level Netlist

- If your gate-level netlist is generated by "CORE-level synthesis"
 - You should all the "CHIP-level module" in it

module CHIP (I_clk, I_rst, I_ams, I_CSI, I_finj, I_si, I_se, I_scantest, I bist mode, I mem sel, I WEN S, I CS S, I OE S, I DI S, I ADDR S, O cmd done, O BGO, O state addr, O hold state addr, O so, O Q, I tpck, I test si2. O test so2); input [1:0] | finj; input [7:0] I_DI_S; input [7:0] I ADDR S; output [3:0] O_state_addr; output [3:0] O hold state addr; output [7:0] O Q; input I clk, I rst, I ams, I CSI, I si, I se, I scantest, I bist mode, I mem sel, I WEN S, I CS S, I OE S, I tpck, I test si2; output O cmd done, O BGO, O so, O test so2; wire clk, rst, ams, CSI, si, scantest, se, bist mode, mem sel, WEN S, CS S, OE S, cmd done, BGO, so; wire [1:0] finj; wire [7:0] DI_S; wire [7:0] ADDR S; wire [3:0] state addr: wire [3:0] hold state addr; wire [7:0] Q; bist_group bist_group (.clk(clk), .rst(rst), .ams(ams), .CSI(CSI), .finj(finj), .si(si), .scantest(scantest), .se(se), .bist_mode(bist_mode), .mem_sel(mem_sel), .WEN_S(WEN_S), .CS_S(CS_S), .OE_S(OE_S), .DI_S(DI_S), ADDR S(ADDR S), .cmd done(cmd done), .BGO(BGO), .state addr(state addr), .hold state addr(hold state addr), .so(so), .Q(Q), .tpck(tpck), .test si2(test si2), .test so2(test so2)); PDIDGZ PAD clk (.PAD(I clk), .C(clk)); PDIDGZ PAD_rst (.PAD(I_rst), .C(rst)); PDIDGZ PAD_ams (.PAD(I_ams), .C(ams));

CHIP-Level Netlist (Cont')

- If your design has a "Hard Block", you should add an "empty module" for it
 - The module name should be the same as the "cell name" of the Hard Block

module memory_040 input clock; input [7:0] A; input [7:0] D:	7 (O, clock, cen_in, oen_in, wen_in, A, D);				
input cen_in; input oen_in; input wen_in; output [7:0] O; endmodule	(Module Declaration)				
wire [7:0] D; wire [7:0] DI_T; wire [7:0] A; wire [7:0] ADDR_T; wire [7:0] O2;	(Module Reference)				
wire [7:0] Q2; wire [7:0] Q1; C	onnected Wire Name in Verilog				
RA1SHD256x8 RA1SHD256x8 (.Q(Q1), .CLK(dk), .CEN(CEN1), .OEN(n168), .WEN(WEN), .A(A), .D(D));					
WEN), .A(A), .D(D));					
CHIP-Level Timing Constraint



Getting Started

Iinux %>tcsh

Before executing SOC encounter, please change your current location to your working folder "SOC"

For example: cd bisr/encounter/SOC/

unix %> encounter

(Do not run in the background mode !!)

Cade on colEncounter® Digital Implementation SystemBTL-to-GDSIIStructor SystemsConstruction SystemsStructor SystemsStructor Systems<t

Import Design <Design>

Design/Design Import

- Verilog Files: your gate-level netlist
- Tot Cell
- LEF Files (*.lef): including all the LEF files of cell libraries & hard blocks
- □ IO Assignment File: *.ioc

Verilog	Files CHIP us	
	Ton Cell: Auto Assign By User CHIP	
O OA	Top Con. C Hato Hosigh C by Osci. Chin	
	Library:	
	Cell:	
	View:	
OA Referen OA Abstract OA Layout	View Names:	
IO Ass	ignment File: CHIP.ioc	
	nfiguration	
 Analysis Cor 		
 Analysis Cor MMMC View 	Definition File:	

Import Design <Power>

- Power Nets: VDD
- □ Ground Nets: VSS
- **Toggle Rate Scale Factor: 0.9**

Import Design <Save Conf.>

- □ Before OK~
- □ Save your import design to a configuration file

Design Import		Save Input Configuration
Basic Advanced	Look in:	/home/phd/cshou/Documenow_v_sram/encounter/SOC 🔽 🌍 🌍 🀑 📂 🔃 📰
Netlist: Verilog Files: CHIP.vg Top Cell: Auto Assign O By User: CHIP	Computer	EF
Cell:		
Technology/Physical Libraries: LEF Files: n_2thick_tech.lef LEF/tpzn90gv3_91m.lef LEF/SRAM_SP_ADV.vclef OA Reference Libraries: OA Abstract View Names: OA Layout View Names:		
Floorplan IO Assignment File: CHIP.ioc		
Analysis Configuration MMMC View Definition File: Create Analysis Configuration	File <u>n</u> ame: Files of type: In	HIP.conf
OK Save Load Cancel Help		CHIP.conf

Close Encounter

Due to some files can not input from GUI, therefore, we need to setup the files by write commands to configuration file (CHIP.conf)



Linux> vi CHIP.conf

mongy@ares-queen:~/Documents/Research_Document/v_code/bisr_low_v_sram/encour	iter/S
<u>File Edit View Terminal Tabs H</u> elp	

# Generated by: Cadence Encounter 10.13-s272_1	
<pre># 05: Linux x86_64(Host ID ares-queen)</pre>	
# Generated on: Sun Jul 22 12:01:15 2012	
# Design:	

global rda_Input	
<pre>set cwd /home/phd/cshou/Documents/Research_Document/v_code/bisr_low_v_sram/encounter/9</pre>	50C
set rda_Input(import_mode) {-treatUndefinedCellAsBbox 0 -keepEmptyModule 1 }	
set rda_Input(ui_netlist) "CHIP.vg"	
set rda_Input(ui_netlisttype) {Verilog}	
set rda_Input(ui_rtllist) ""	
set rda_Input(ui_ilmdir) ""	
set rda_Input(ui_ilmlist) ""	
<pre>set rda_Input(ui_ilmspef) ""</pre>	
<pre>set rda_Input(ui_fmdir) {}</pre>	
<pre>set rda_Input(ui_settop) {1}</pre>	
<pre>set rda_Input(ui_topcell) {CHIP}</pre>	
set rda_Input(ui_celllib) ""	
<pre>set rda_Input(ui_iolib) ""</pre>	
<pre>set rda_Input(ui_areaiolib) ""</pre>	
set rda_Input(ui_blklib) ""	
<pre>set rda_input(ui_kbox(ib) ""</pre>	
1,1	

Import Design <Design> (cont.)

Due to No GUI, it requires to write the commands to .conf

- □ LIB Files (*.lib):
 - Max Timing Libraries
 - Min Timing Libraries
 - Common Model Libraries

Find a line denoted with

- = 110,1111) \leftarrow 11111 (1111)
- set rda_Input(ui_timelib) "" <= typical timing libraries

Import Design <Timing>

Due to No GUI, it requires to write the commands to .conf

- □ Capacitance Table File
- □ Timing Constraint File: *.sdc
- QX Tech File: FireIce capacitance file
- **QX** Library Directory:

Find a line denoted with

After Initialization

Based on configuration file, the soc encounter shows the blocks



Global Net Connection

Floorplan/Global Net Connections

]	Global Net Connections	
Connection List	Power Ground Connection	
VDD:PIN:*.VDD:Module(Connect	
VDD:NET:VDD:Module()	🔾 🔾 Pin	
VSS:NET:VSS:Module()	🔾 🔾 Tie High	
	O Tie Low	
	Instance Basename: *	
	Pin Name(s): VSS	
	Net Basename: VSS	
	Scope	
G	Single Instance:	
	Under Module:	
	O Under Power Domain:	
	Under Region: IIX: 0.0 IIV: 0.0 urx: 0.0 ury: 0	.0 🗎
	O Apply All	
	T. OLIVIA USS	
	To Global Net: VSS	
	Override prior connection	
	Uerbose Output	
		oloto
	(Add to List) Opdate	elete
Aunte	Canaal Canaal U	

Specify Floorplan



1

0.65

0.047383

479.38 478.8

> 950.0 950.0

> > 80

80

Unit: Micron

Help

Ratio (H/W):

Core to Top:

Specify Scan Chain

encounter %> specifyScanChain ScanChainName

- start {ftname | instPinName}
- start {ftname | instPinName}

encounter %> scantrace

Ex:



Hard Block Placement

□ Move/Resize/Reshape floorplan object

		١Ŋ	NΝ	NΝ	N								1
CORNERO												CORNERI	
PAD CS S					2000 BOO		0 2001					CONNENT.	
PAD WEN S										_			
PAD mem sel													
PAD bist mode													
PAD scantest													
PAD_se												PAD_test_s	i2
PAD_si												PAD_tpclk	
PAD_finj1													
PAD_finj0													
PAD_CSI												PAD_ADDR	_\$7
PAD_ams												PAD_ADDR	SE
PAD_rst		4										PAD_ADDR	SE
PAD_clk												PAD_ADDR	_\$4
										k			
ORNERS	X	$\langle \rangle $	$X \ X \ $	X X	X X	$\ X\ $	$\ X\ $	$ I _{I}$	$\langle \rangle$	\mathbb{N}	$ \chi $	CORNER2	1



Edit Block Halo

Floorplan/Edit Block Halo

Reserve space without standard cell placement





Standard Cell Placement

□ Place/Place



Advanced Reliable Systems (ARES) Lab.

Power Planning – Add Rings

Floorplan/Custom Power Planning/Add Rings

Net(s):	VDD VSS]
Ring Typ	e				
• Core ri	ing(s) conto	ouring			
🖲 Arc	ound core b	ooundary	 Along 	I/O boundary	
Exc	clude selec	ted objects			
O Block I	ring(s) arou	ind			
🖲 Ea	ch block				
O Ea	ch reef				
 Sel 	lected powe	er domain/fend	ces/reefs		
O Ea	ch selected	l block and/or	group of cor	re rows	
O Clu	isters of sel	lected blocks	and/or group	is of core rows	
	With share	ed ring edges			
O User d	efined coor	rdinates:			MouseClick
• Co	ore ring	 Block ri 	ng		
Ring Cor	figuration	-			
	Тор:	Bottom:	Left:	Right:	
Layer:	M9 H >	M9 H 🕨	M8 V >	M8 V 🕨	
Width:	3	3	3	3	
Spacing:	0.805	0.805	0.805	0.805	Update
Offset:	Center i	n channel 🤇	Specify		
	0.00000000	Y	1	1	1

Basic Advanced Via Generation
Set Custom Ring Sides and Extension
Create rectangular ring(s) only Merge with pre-routed rings if within spacing threshold: 0.56 Minimum jog distance: 0.56 Snap wire center to routing grid: None
Wire Group Use wire group Interleaving Number of bits: 15
Reinforcement stripes Spacing: O Width:

Power Planning – Add Block Rings

Floorplan/Custom Power Planning/Add Rings

Basic Advanced Via Generation	Set Custom Ring Sides and Extension
Net(s): VSS VDD	
Ring Type	
Around core boundary Along I/O boundary Exclude selected objects	
Block ring(s) around Each block	
✓ Each reef	
✓ Selected power domain/fences/reefs	
Each selected block and/or group of core rows	
\checkmark Clusters of selected blocks and/or groups of core rows	
With shared ring edges	
↓ User defined coordinates Mouse Click	
◆ Core ring	

Example for Power Rings



PAD Pins

□ Route/SRoute

SRoute				
🔲 Block Pins	⊻ Pad Pins	🔲 Pad Rings	Follow Pins	Secondary Power Pins
Pouting Contro				



Power Planning – Add Stripes

Floorplan/Custom Power Planning/Add Stripes

Basic Advanced Via Generation	
Set Configuration	Basic Advanced Via Generation
Layer: METAL4 Direction: Vertical Vertical I	Stripe Breaking Omit stripes inside block rings Omit stripes over selected blocks/domains
Spacing: 0.28 Update	Target Connection Control Pad/Core ring connection
◆ Set-to-set distance: 100 ↓ Number of sets: 1	Allow jogging Block ring connection Allow jogging
	Merge with block rings if spacing less than: 0.56 Maximum length of same layer jog: 0.56
Stripe Boundary Core ring Pad ring Inner Outer Design boundary Create pins Each selected block/domain/fence All domains Specify area	Layer Control for Target Connections Pad/Core rings Top limit: METAL4 Bottom limit: METAL4 Block rings Top limit: METAL4 Bottom limit: METAL4 Bottom limit: METAL4
First / Last Stripe Start from: ↓ left ◆ right ◆ Relative from core or selected area X from left: 80 X from right: 20	Wire Group Use wire group Interleaving Number of bits: 5

Power Planning – Add Stripes (Cont')



Ex:

Fix Un-Connected Stripes

□ Route/SRoute

Rou	ite							33	
	Block pins		Pad pins		Pad rings		Standard cell pins	Γ	Stripes (unconnected)
		1							
THE OF									
TRADE IN									
		1		for for for				eee	
	. URAR								
	a manage of								
		1				\sim	-		
No.									
	normanian (n. 1911) - no - dia - na characterizza da 2011 - no - dia - na characterizza da 2011 - na - dia - na characterizza da 2011 - dia - dia - dia characterizza da 2011 - dia - dia - dia								
	NUNN	a ta ta ta			********	++++		itititi	
		\mathcal{D}							

Flow Clock Tree Synthesize



Create/Specify/Synthesis Clock Tree Spec.

Clock/Create Clock Tree Spec						
X Create	Clock Tree S	Spec				
Create Clo Bu	ock Tree Spe ffer Footprint:	cification				
Inver	ter Footprint:	clkinv				
🔲 Ignore	Buffer List: Don't Use					
Save Spec T	o: CHIP.ctst	ch				
<u>o</u> ĸ	Apply	Cancel	Help			

Clock/Specify Clock Tree

alaction		
CH	HP.ctstch	D
Apply	Cancel	<u>H</u> elp
	election	CHIP.ctstch

Clock/Synthesis Clock Tree

V CHIF.CISIC	1 - K write	9.6
Eile Edit View	[,] <u>B</u> ookmarks <u>T</u> ools <u>S</u> ettings <u>H</u> elp	
1 1 1 1 1	∄ Q <~ ≫ d D D S S S S S	
# # FirstEncounte #	er(TM) Clock Synthesis Technology File Format	
# MacroMod #MacroModel p <inputcap></inputcap>	lel in <pin> <maxrisedelay> <minrisedelay> <maxfalldelay></maxfalldelay></minrisedelay></maxrisedelay></pin>	<minfalldelay></minfalldelay>
# Special Ro #RouteTypeNa #TopPreferredl #BottomPrefer #PreferredExtra #End	oute Type ume specialRoute .ayer 4 redLayer 3 aSpace 1	
# Regular R #RouteTypeNa #TopPreferredl #BottomPrefer #PreferredExtra #End	oute Type ime regularRoute .ayer 4 redLayer 3 aSpace 1	
# Clock Gro #ClkGroup #+ <clocknam< td=""><td>ə></td><td></td></clocknam<>	ə>	
# # Clock Root # Clock Name # Clock Period	: PAD_olk/C : CLK1 : 20ns	
#AutoCTSRootF Period 20 MaxDelay MinDelay 0 MaxSkew	Pin PAD_clk/C ins 1ns # default value ins # default value 300ps # default value	

(Clock Spec.)

Example for CTS Report

Nr. of Subtrees Nr. of Sinks Nr. of Buffer Nr. of Level (including Max trig. edge delay at Min trig. edge delay at	:1 :99 :5 gates):1 t sink(F): bist_group/bis sink(R): bist_group/me	t/m0/shift_reg_reg_10_/CKN 230.9(ps) mory_0407/clock 176.8(ps)
Rise Phase Delay Fall Phase Delay Trig. Edge Skew Rise Skew Max. Rise Buffer Tran Max. Rise Sink Tran Max. Fall Buffer Tran Min. Rise Buffer Tran Min. Rise Buffer Tran Min. Rise Sink Tran Min. Fall Sink Tran Min. Fall Sink Tran	(Actual) (Rec : 176.8~217.5(ps) : 189.2~230.9(ps) : 54.1(ps) : 40.7(ps) : 41.7(ps) : 58.4(ps) : 58.4(ps) : 177.9(ps) : 165.4(ps) : 23.2(ps) : 23.2(ps) : 97.9(ps) : 92.4(ps)	quired) 0~1000(ps) 0~1000(ps) 300(ps) 400(ps) 400(ps) 400(ps) 400(ps) 0(ps) 0(ps) 0(ps) 0(ps)
***** NO Max Transitio	n Time Violation *****	
***** NO Min Transitior ***** NO Max_Fanout \	n Time Violation ***** Violation *****	

Display Clock Tree

□ Clock/Display/Display Clock Tree

🗙 Display Clock Tree 🔷 🕞 😒	Ex:
Clock Selection All Clock(s) Selected Clock	
Route Selection Pre-Route Clock Route Only Post-Route 	bist_group/memory_0407
Display Selection Display Clock Tree All Level	
 Bottom Level (non-gated clock tree only) Selected Level (non-gated clock tree only) 1 Display Clock Phase Delay Display Min/Max Paths 	
<u>O</u> K <u>A</u> pply <u>C</u> ancel <u>H</u> elp	bist_group/RA1SHD256x8

Power Analysis

Power/Edit Pad Location

Y	÷ 📃 ۱	ayer:	_		
Get Coord		Delete		Add	
uto Fetch Pad	Location				
: VSS				Auto Fe	tch
ad Location Lis	st				
1094.012500	406.235000	M2	PAD Cor	eVSS3	
1094.012500	597.455000	M2	PAD Cor	eVSS4	
230.742500	406.235000	M2	PAD Core	VSS1	_ 1
230.742500	788.675000	M2	PAD Core	VSS2	_ 1
1093.942500	358.430000	M5	PAD Cor	eVDD3	_ 1
1093.942500	549.650000	M5	PAD_Cor	eVDD4	
230.812500	358.430000	M5	PAD_Core	VDD1	
200 012500	740.870000	M5	PAD Core	VDD2	

Power/Edit Net Toggle Probability

– Clock Info — Clock Name:		CLK1		
Clock Rate(MH	z):		50.0	000
Net Toggle Probability:			0.9)0
Get Clock	Edit	Add/Repla	ace	Delete

Power/Power Analysis/Statistical

Ex:

I	**********
I	# The Power Analysis Report for VDD net #
I	
I	
I	power supply. 1.36 v 1 04700.01 mm
I	average power(default): 1.04/04/01 mw
I	average switching power(default): 2.3212e+00 mw
I	average internal power(default): 8.1442e+00 mw
I	average leakage power(default): 4.7600e-03 mw
I	average user specified power(default): 0.0000e+00 mw
I	average power by clock domain category:
I	clock domain(CLK1. 0.9) : 1.0282e+01 mw
I	clock tree power : 4,1149e+00 mw
I	non clock tree nower : 6 1672e+00 mw
I	unclock domain $(0,2)$: 1 8807e-01 mw
I	
I	
I	
I	DTOCK: 3.1001e+00 mw
I	10: 0.0000e+00 mw
I	average power(considered in rail analysis): 1.04/0e+01 mw
I	worst IR drop average analysis: 1.9/18e-03 v
I	number of nodes in rail network: 16645 nodes
I	worst EM:
I	"M1" 5.2000e-02 mA/u
I	"M2" 0.0000e+00 mA/u
I	"M3" 3.9142e-01 mA/u
I	"M4" 3.9142e-01 mA/u
I	"M5" 2.2647e-01 mA/u
I	"V12" 1.4821e-02 mA/cut
I	"V23" 1 4821e-02 mA/cut
I	"V34" 9 7855e-02 mA/cut
I	"V45" 2 8280e-02 mA/cut
I	biggest toggled net: clk 11 NO
I	no of terminal 03
I	total cap, 7 60440 ± 02 ff
1	LULAT CAP: 7.00440+02 TT

(Power Analysis Report)

Advanced Reliable Systems (ARES) Lab.

Example for Rail Analysis of IR-Drop & EM



Power Route

□ Route/SRoute



IO Filler

encounter %> source addloFiller.cmd

PAD hold state addr2		
PAU DOID STATE ADDRI		
PAD hold state addr0		

Nano Route

□ Route/NanoRoute

Mode Global Route Detail Route JDFM	Start Iteration de	efault End Iteration	default	
Concurrent Routing Features	s 🔄 🔲 Insert Diodes	Diode Cell Name	Fill Cells	
Timing Driven	Cong Effort 0	gestion Timing	S.M.A.R.T.	
F SI Driven	Cong Effort normal SI Victim File	gestion SI	6	

NanoRoute/A	ttributes						9	•
♦ Net Type(s):	F Clo	ck Nets	💷 External	Nets 🔲 Critica	al Nets _	Selected Nets		
✓ Net Name(s):								
Skip Antenna	💠 TRI	JE 💠 FAL	.se 🔷 asis	Top Layer	ASIS	Bottom Layer	ASIS	1
Skip Routing	💠 TRI	JE 💠 FAL	.se 🔶 asis	Weight	10	Spacing	1] 1
Avoid Detour	🔶 TRI	JE 💠 FAL	.se 💠 Asis	Shield Net(s)	ASIS			
SI Prevention	💠 TRI	JE 💠 FAL	.se 🔶 asis	Nondefault Rule	ASIS			
SI Post Route Fix	🔷 TRI	JE 💠 FAl	.se 🔷 asis	Pattern	ASIS	±		

Example for Nano Route



Cell Filler

Place/Filler/Add Filler

🗙 Add Filler			
Cell Name(s) FILL	1 FILL 16 FILL 2	FIL Select	\triangleright
Prefix FILLER			
Fill Boundary			
🔲 Fill Area Dra	aw		
llx.		lly	
urx		ury	
ок	Cancel	Help	
			R
🗙 Select Filler C	iells		
Selectable Cells I	.ist —	Cells L	ist
FILL1	ĥ	FILL1	
FILL2		FILL2	
FILL32	A	FILL32	
FILL4 FILL64		FILL4	
FILL8	<u>D</u> e	FILL8	
	4		7
		<u> </u>	12
	Ū	ose	
	2		

Ex:



Save Design

- □ Design/Save/Netlist → *.v
- □ Timing/Calculate Delay → *.sdf
- □ Design/Save/DEF → *.def
 - SELECT "Save Scan"

Bounding PAD

- unix %> chmod 755 addbonding.pl
- □ unix %> /usr/bin/perl addbonding.pl CHIP.def
- encounter %> source bondPads.cmd





□ Design/Save/GDS → *.gds
LAB

- □ 利用 SOC encounter 將 gate-level netlist 檔轉換為 layout 的 GDS 檔
- □ 實驗報告內容:
- □ 1.實驗目的
- □ 2.分別附上編輯完後的.vg檔.sdc檔.ioc檔
- □ 3.最後請附上.gds的結果,並確定無任何的violation。