Dept. of Electrical Engineering
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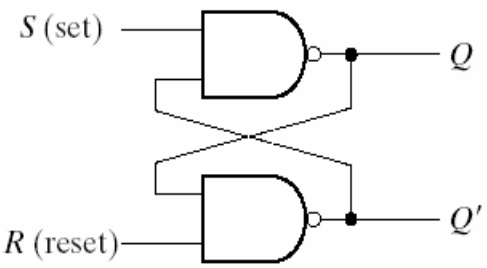
CAD for VLSI Design

Homework #2
(Due: Apr. 16)

1. For the SR latch shown right, please determine the values of Q and Q' with their corresponding time after every change from 0 to 20ns. Assume the delay time of each NAND gate is 1ns and the initial values of Q and Q' are 0 and 1 respectively. The input patterns for (S,R) = (1,1) @ 0ns; (0,1) @ 5ns; (0,0) @ 10ns; and (1,1) @ 15ns.



2. Please apply the K-L algorithm and show the step-by-step solutions to find a balanced bipartition of the circuit shown right.