

Digital System Design (EE4022)

Course Time / Location: Tuesday 15:00-16:50 (E1-124), Thursday 13:00-13:50 (E1-124)

Lab Time: Tuesday 10:00-11:50, Thursday 13:00-14:50 (choose one)

Instructor: Chien-Nan Liu (劉建男) **Email:** jimmy@ee.ncu.edu.tw

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Office Hours: Wednesday 14:00-15:00; other time by appointment only.

Teaching Assistant:

- to be announced on the course website ...

Prerequisites: Introduction to digital systems

Text Book: M. Morris Mano, “Digital Design”, 3rd Edition, Prentice Hall Inc., 2002.
ISBN 0-13-062121-8.

Reference: 1. Douglas J. Smith, “HDL Chip Design”, Doone Publications, Madison, AL, USA, 1997. ISBN 0-9651934-3-8.
2. M. Morris Mano, and Charles R. Kime, “Logic and Computer Design Fundamentals”, 2nd Edition updated, Prentice Hall Inc., 2001. ISBN: 0-13-032406-X.

Course Contents:

- Introduction to HDL-based design methodology (1 week)
- Asynchronous sequential logic (2 weeks)
- Language fundamentals -- Verilog HDL (2 weeks)
- Verilog simulation (1 week)
- FPGA synthesis using Verilog (1 week)
- Modeling combinational logic circuits (1 week)
- Modeling sequential elements (1 week)
- Modeling finite state machines (1 week)
- Modeling digital systems (1 week)
- Introduction to HDL synthesis (1 week)
- Timing issues in digital designs (1 week)
- Final project (2 weeks)

Grading:

Lab: 10%, Homework: 25%, Final Project: 20%, Midterm: 25%, On-Line Test: 20%

On-Line Resources: Lecture notes, homeworks / tests, sample solutions, grading information, and other course-related materials are available at <http://www.ee.ncu.edu.tw/~jimmy/courses/DSD06>

Academic Honesty: Cheating is very uncivilized behavior and is to be avoided at all cost. Oral discussion about homeworks is not considered cheating. Copying someone else’s homeworks / tests or part of a homework / test is cheating. If cheating is discovered, all students involved will receive no credit for the homework / test and possibly get an F grade for the course.