Dept. of Electrical Engineering
National Central University

Chien-Nan Liu
September 14, 2017

Design and Verification Methodology for SoC (EE513)

Time / Location: Thursday 09:00-11:50 (E1-110)

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Office Hours: Wednesday 14:00-15:00; other time by appointment only.

Teaching Assistant:

- 曾華逸, office: E1-359 (ext:34577), Email: w29252647@gmail.com
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Prerequisites: Computer programming, Introduction to digital systems and VLSI design

Reference Books:

- 王駿發, 王朝欽, 李聰, 李昆忠, 黃穎聰, 董蘭榮, 謝明得, "系統單晶片概論 SOC", McGraw-Hill, 2006.
- Michael Keating and Pierre Bricaud, "Reusable Methodology Manual for System-on-a-chip Designs", 2nd Edition, Kluwer Academic Publishers, 1999.
- Prakash Rashinkar, Peter Paterson, and Leena Singh, "System-on-a-chip Verification – Methodology and Techniques", Kluwer Academic Publishers, 2001.

Course Contents:

- Introduction to SoC design and verification (1 week)
- Reusable design methodology (1 week)
- System specification and modeling (2 weeks)
  - Introduction to system modeling (3hrs)
  - SystemC™ overview (3hrs)
- Verification methodology for SoC (1 week)
- Coverage-driven functional verification methodology (1 week)
- Static verification techniques (2 weeks)
  - HDL lint checking (2hrs)
  - Formal verification (2hrs)
  - Static timing analysis (STA) (2hrs)
- Low-power design methodology (2 weeks)
  - Power estimation overview (3hrs)
  - System-level low-power design techniques (3hrs)
- Analog/mixed-signal system simulation (3 weeks)
  - Introduction to AMS behavior modeling (3hrs)
  - Verilog-A overview (3hrs)
  - Case study of AMS behavior modeling (3hrs)
- Automatic analog design methodology (2 weeks)
  - Introduction to analog design automation (3hrs)
  - Automated robust design optimization for analog circuits (3hrs)

Grading:

Projects: 60%, Exams: 40%

On-Line Resources: Lecture notes are available at NCU LMS system (https://lms.ncu.edu.tw). Other course-related materials are available at http://www.ee.ncu.edu.tw/~jimmy/courses/DVM17