Dept. of Electrical Engineering
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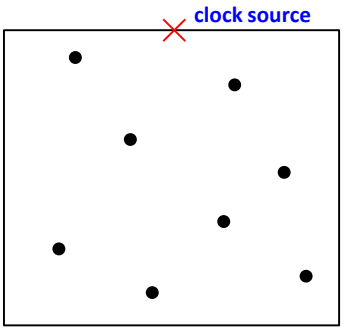
Introduction to Electronic Design Automation (EE4026)

Homework #4
(Due: May 28)

1. Assume the solid dots are the clock pins in a chip that should be connected to the clock source at the chip boundary. Please use the geometric matching algorithm to find a clock tree in which each path from the clock source to a clock pin has similar wire length. Please redraw the rough routing result on your answer sheet. (Exact measurement is not required.)



2. Given the following Verilog code, show the correct synthesized gate-level network for it. (MUX, FAs, latches, flip-flops and tri-state buffers can be expressed as a block)

```
module Prob2 (s, in, clk, out);
   input s, in, clk;
   output out;
   reg a, b, x, y, z;

   assign out = z ? 1'bz : y;

   always @(s or in) begin
      a = 0;
      if (s) a = in + 1;
      else b = in;
   end

   always @(posedge clk) begin
      x = a;
      y = b & x;
      z = 1`b0;
   end
endmdule
```