Dept. of Electrical Engineering
National Central University

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Introduction to Electronic Design Automation (EE4026)

Homework #6

(Due: ------)

1. Given the following gate-level netlist and three faults labeled in it.
   (a) Please show the details for each net to demonstrate how to perform parallel fault simulation and determine the tested faults.
   (b) For the untested faults in (a), please choose one as the target for D-algorithm and find out the test pattern that can test this fault.
   (c) Assume the target fault is I/0. Please use PODEM algorithm to find out the test pattern that can test this fault.