# Programming Assignment 3-4:
# Static Timing Analyzer

**Problem Descriptions:**

Given a gate-level netlist, implement the three steps below to show the longest and shortest delay times and their corresponding paths.

**Delay Calculation:**

Step1: Build the delay graph according to the given netlist.

Step2: Calculate the delay of each node in the graph according to the topological order.

Step3: Output the longest and shortest delays and their corresponding paths.

**Input/Output Format:**

The input format is a spice-liked format that describes the connection between gates. An example of this format and its corresponding netlist are shown in Figure 1. Each node in the netlist, including the primary inputs and the primary outputs, is given a unique number, which is a positive integer and greater than zero. The nodes of primary inputs and primary outputs are declared by the keyword **IN** and **OUT** respectively. The supported gate types are **INV, AND, NAND, OR, NOR, XOR,** and **XNOR**. For each gate, the first number represents its output node, and the numbers followed by the gate type are its input nodes. Except the gate type **INV**, all other gate types support any numbers of input. Finally, the netlist is finished by the keyword **END**. In this format, all the lines begin with a "**!**" are viewed as the comment lines and should be skipped. Most importantly, all the bolded keywords are **case-sensitive**. Because the netlist format is the same with HW1, you can use the netlist parser provided in HW1 directly

```
! An example of gate–level netlist
IN    1   2   3
 4  INV   1
 5  INV   2
 6  NAND  4   5
 7  INV   5
 8  NOR   3   4
 9  INV   6
10  XOR   6   7
11  AND   7   8
12  XNOR  9  10
13  OR    8   9   10
OUT  11  12  13
END
```

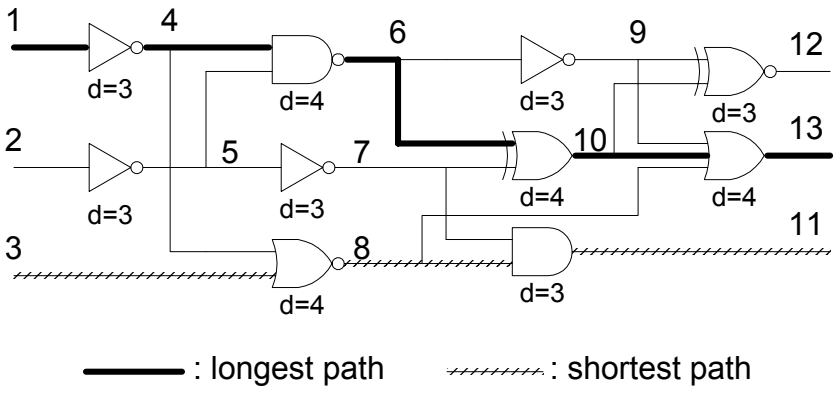


Figure 1 : An example of the gate-level netlist and its corresponding descriptions.

For easier implementation, the delay time of each gate is set as the sum of the numbers of its inputs and fanouts. For example, an inverter with two fanouts has delay 3 and a three-input OR gate with one fanout has delay 4. According to this delay information, the running results of the example shown in Figure 1 are shown in Figure 2. About the test circuits, please use the same three circuits provided in HW1.

```
Longest delay = 15, the path is:
   Input 1
   Gate  4
   Gate  6
   Gate  10
   Gate  13

Shortest delay = 7, the path is:
   Input 3
   Gate  8
   Gate  11
```

Figure 2 : The results of the delay calculator with the example shown in Figure 1.

**Requirement:**

The program must be able to receive commands in following format:

```
%    a.out    netlist_file
```

You must **output the longest and shortest delays and their corresponding paths** as shown in Figure 2. Your grade depends on the correctness and runtime of your program. You may first compress all of the source code and execution file and then email your homework to TA before the deadline (please specify your student ID in the subject). The implementation details and your comments about this homework should be written in a simple **report** and mailed to TA together.