Programming Assignment 5-2:
Chip Floorplanning/Placement with Hard Macros

Problem Descriptions:

Given a set of rectangular macros and nets among these macros, place all these macros within a specified rectangular bounding box. The main objective is to minimize the total wire length estimated by the semi-perimeter method. The second objective is to minimize the chip area.

Input format:

The input consists of two files. The first file contains a given bounding box with its height and width, and a list of macro names and their height and width. Here gives the format of the first file:

```
.chip_bbox    (width, height)
// the lower-left corner of this bounding box is (0, 0)
.macro    macro_name macro_width macro_height
.macro    macro_name macro_width macro_height
... More macros which are free to rotate
```

The format of the second file (netlist) is as follows:

```
.net    net_name macro_name1 macro_name2 …
.net    net_name macro_name1 macro_name2 …
… More nets
// one line defines a net
// for example, if net N1 connect macro A, B, and C, the definition is
// .net    N1    A    B    C
```

Output format:

The output report consists of three parts: (1) coordinate for each macro, (2) total wire length estimated by the semi-perimeter method, and (3) area (it may be smaller than chip bounding box). The format of the report file *problem1.rpt* is as follows:

```
.macro    macro_name (x1, y1) (x2, y2)
.macro    macro_name (x1, y1) (x2, y2)
// (x1, y1): lower-left corner, (x2, y2): upper-right corner
… More macros
.mst    total_wire_length
.area    chip_area
// area = (max_x2 – min_x1) * (max_y2 – min_y1)
```

Grading:

Your grade depends on the correctness, and runtime of your program. You may first compress all of the source code and execution file and then email your homework to TA before the deadline (please specify your student ID in the subject). The implementation details and your comments about this homework should be written in a simple report and mailed to TA together.