Effect of Thermal Management on the Performance of VCSELs

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***Abstract*— This study investigated the effect of thermal management on the performance of vertical-cavity surface-emitting lasers (VCSELs). It was found that the thickness of silicon substrate, which can serve as the submount for VCSEL packages, has a strong influence on the thermal dissipation of on-chip laser sources, and eventually impacts on their output characteristics. Moreover, the improvements in optical characteristics of the on-chip VCSELs were the best heat dissipation through thinning silicon substrates to 50-μm thickness combined with electroplated Cu with 100-μm thickness. In addition, this study also performed COMSOL simulations. The simulation results were consistent with experimental results.**

***Index Terms*— COMSOL simulations, heat dissipation, thermal management, vertical-cavity surface-emitting lasers (VCSELs).**

I. Introduction

THE vertical-cavity surface-emitting lasers (VCSELs) were developed more than 30 years ago and were first introduced in the commercial level [1]–[3]. VCSELs possess many unique features, such as wafer-level testing, small packaging capability, low-power consumption, optical beam quality, high operating speed, easy coupling with optical fibers, small cavity volume, and single-mode ultralow threshold current operations [3]–[5]. Due to the innovative applications based on VCSELs, the demand for VCSELs has increased rapidly in recent years. They can not only serve as the light source in optical interconnect (OI) networks using multimode optical fibers, but also they can also be included in various consumer applications, such as laser mice, laser printers, and sensors [6]–[10]. Moreover, using VCSELs as building blocks in large-scale computer systems using parallel OIs has become increasingly important for optical computer applications. There are driver/receiver electronics, optoelectronic (OE) device arrays, and optical systems for efficient fiber coupling in parallel modules. The key component is the light source which must satisfy the challenging and often conflicting goals of high-speed, low-power dissipation, and low cost. In general, VCSELs are used as the light source and are always required to operate with high power.

Normally, the structures of VCSELs with 850-nm wavelength are grown on GaAs substrates. The thermal conductivity of GaAs substrates is only 55 W/mK. The thermal conductivities of Si and Cu substrates are 135 and 400 W/mK, respectively. Obviously, GaAs substrate is not a good heat sink. Moreover, sustained high-speed performance of VCSELs when under high-temperature operations is also an important challenge because the optics transceiver modules (VCSELs with photodiodes) must be packaged as close as possible to the electronic integrated circuits (ICs), which also generate a significant amount of heat during high-speed operations [11]–[13]. It is thus vital to have a VCSEL light source with a good heat sink, which ensures the desired high data rate (>50 Gbit/s per lane) in the next generation of OI channels application.

In order to satisfy the demand for the growth of high performance, power dissipation of ICs generally accounts for the major portion of energy budgets in IC technology nowadays [14]. Heating of the laser sources during operation places a major bottleneck for efficient implementation of silicon photonics [15]. Generated heat during operation shifts the peak wavelength and thus reduces the efficiency significantly [16]. So, it is important to facilitate heat dissipation from an active region of laser diodes to ambience. Currently, effective heat dissipation is the main packaging design issue for all of the photonic applications [17]–[19]. Even though researchers in the world have been working on many complex heat sink designs, the majority of these designs add to the cost of the overall designs by having complex steps in the process [20], [21]. Designing cost-effective heat sinks for III–V VCSELs, operating in the infrared (IR) range ($\lambda \sim$ 845 nm) was the primary motivation of our present work. In the case of on-chip laser sources, laser chips are bonded to the silicon substrate directly [22]. Because the thermal resistance of a material depends on its thickness [23], the thickness of the substrate was reduced by either lapping or it was etched into the trench structure, before bonding to the laser source. To reduce the overall thermal resistance, copper (having high thermal conductivity) was electroplated on the backside of silicon [24]. Performances of the VCSELs bonded to these different heat sinks were measured. Reduced operating voltage, thermal resistance, and variation in peak emission wavelength were obtained experimentally. The output optical

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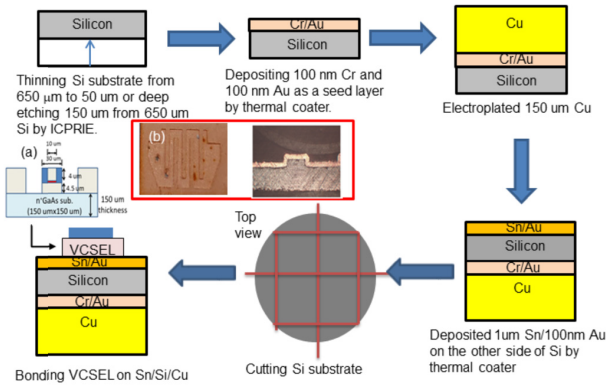

Fig. 1. Schematic flowchart of experimental steps. Inset (a) is the heat source structure and (b) is the deep etching 150 μm from 650-μm Si by ICPRIE and after Cu electroplating.

power and quality factors were also evaluated. For better insight, the temperature of on-chip VCSELs with different heat sink structures was also simulated by COMSOL software to enable a comparison of experimental results to be undertaken.

II. Experimental Details

Fig. 1 depicts the schematic flowchart of the experimental steps in this study. Two samples of Si substrate with a thickness of 650-μm were prepared. One was by inductive-coupled plasma reactive ion etching (ICPRIE) and the other was by lapping, which resulted in the 650-μm substrate with 150-μm trench and thicknesses of 50 μm, respectively. Next, the metals Cr and Au with 100-nm thickness were deposited on the backside of Si by a thermal evaporation system. Here, Cr acts as an adhesion layer, and Au plays the role of a seed layer for electroplating Cu. To improve the thermal conductivity, Cu with 100-μm thickness was electroplated on the backside. Cu was chosen as the heat sinking material due to its high thermal conductivity. Finally, Sn and Au metal layers with the thickness of 1 μm and 100 nm, respectively, were deposited on the top side of the silicon. The wafer was then diced into pieces. Then, VCSEL with 10 $\pm$ 1 μm aperture size and 845-nm wavelength chip shown in the inset (a) of Fig. 1 was bonded to the Si top surface with Sn/Au layers using ultrasonic bonding at a temperature of 280 °C. The VCSEL structure was p-type distributed Bragg reflector (DRB) layers with 28 pairs ($Al_{0.9}Ga_{0.1}As/Al_{0.1}Ga_{0.9}As$), active layers with 3 pairs layers ($In_{0.02}Ga_{0.98}As/Al_{0.12}Ga_{0.88}As$), and n-type DRB layers with 34 pairs ($Al_{0.9}Ga_{0.1}As/Al_{0.1}Ga_{0.9}As$) grown on GaAs substrate. Finally, all the samples were bonded to the circuit board using silver paste before measurements. Optical output power, operating voltage, quality factor, and thermal resistance of the VCSELs were bonded onto Si with a 650-μm thickness (labeled A). Si with a 650-μm thickness was combined with the 150-μm Cu trench (labeled B) and Si with a 50-μm thickness (labeled C) was measured. For reference, stand-alone VCSEL (labeled D) was also measured after bonding with silver paste to the circuit board directly.

III. Results and Discussion

In order to understand the effect of the Si substrate thickness on the VCSEL operating temperatures, COMSOL software was used to simulate the effect of the heat sink design on the VCSEL operating temperatures. The VCSEL source was taken into consideration as a heat source where emitted heat energy at a rate of 2.5 $\times$ 10^8 W/m^2 created by the 10-μm

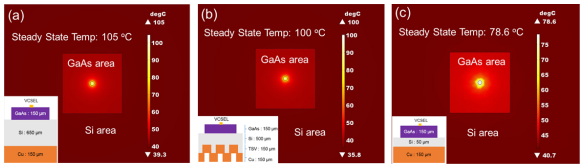

Fig. 2. COMSOL simulation results for heat dissipation from the samples at steady-state (a) sample A, (b) sample B, and (c) sample C. Steady-state temperatures for all samples are mentioned in the figures.

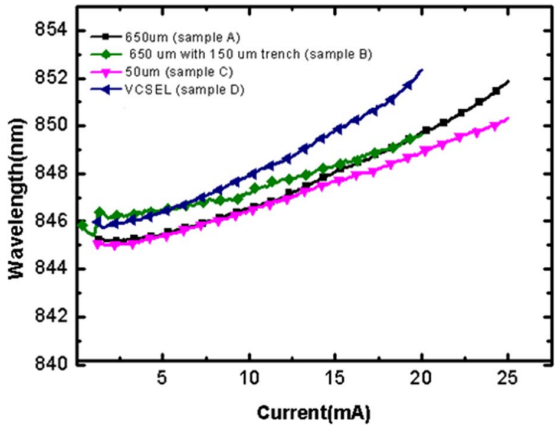

Fig. 3. Peak wavelength as a function of the injection current for samples A–D.

aperture (lasing area), then heat conducted to GaAs substrate with 150-μm thickness and 150 μm $\times$ 150 μm area. The heat source was shown in the inset of Fig. 1(a). An ambient temperature of 25 °C was used. Here, 45 mW was assumed the worse operation condition for the simulation. The simulation results of operating temperatures at a steady state for the above three structures are shown in Fig. 2. The temperatures at a steady state are 105 °C, 100 °C, and 78.6 °C for samples A, B, and C, shown in Fig. 2(a)–(c), respectively. The temperature of sample B can be reduced by about 5 °C lower than that of sample A. Nevertheless, sample C which had the thinnest thickness of silicon substrate resulted in the lowest operating temperature (78.6 °C). Thermal resistance of a material was defined as the inability to dissipate heat during an operation. The thermal resistance of the stack ($R_{\text{effective}}$), used in the samples can be written as

$$R_{\text{effective}} = \frac{X_{\text{VCSEL}}}{A \cdot K_{\text{VCSEL}}} + \frac{X_{\text{Si}}}{A \cdot K_{\text{Si}}} + \frac{X_{\text{Cu}}}{A \cdot K_{\text{Cu}}} \quad (1)$$

where X_{VCSEL}, X_{Si}, and X_{Cu} are the thicknesses of VCSELs, Si, and Cu, respectively. A was the cross-sectional area of the sample. K_{VCSEL}, K_{Si}, and K_{Cu} were the thermal conductivities of VCSELs, Si, and Cu, respectively. It can be deduced from the above relation, thermal resistances of different layers were additive and were directly proportional to the thickness of respective layers. Thus, reducing silicon thickness by lapping resulted in the reduction of thermal resistance, which resulted in reducing the operating temperature.

Fig. 3 shows the peak emission wavelength from the samples as a function of the injection current. The $\Delta\lambda/\Delta I$ (nm/mA) was 0.26, 0.189, 0.23, and 0.34 for samples A, B, C, and D, respectively. Obviously, sample D presented the largest $\Delta\lambda/\Delta I$. The temperature of the device could increase during operation resulted from the joule heating. It could cause red-shift in the peak wavelength for all the samples [25], [26].

Fig. 4(a) and (b) shows the forward current as a function of voltage curves and semilog scale leakage current as a function

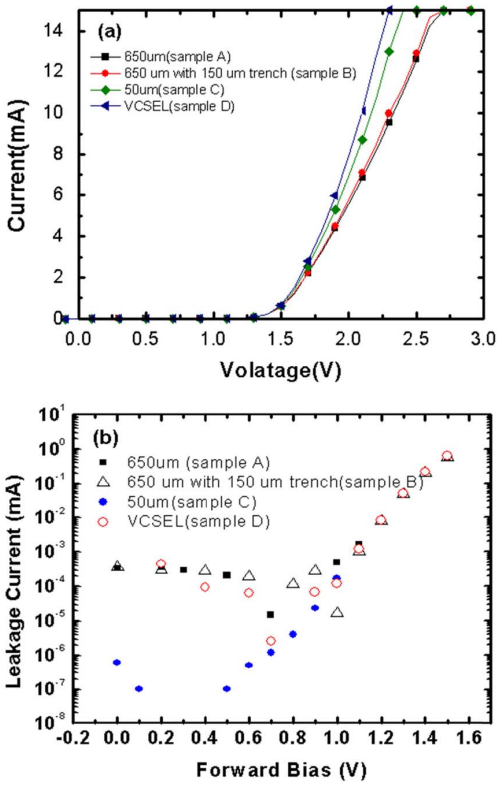

Fig. 4. (a) Current versus voltage curves. (b) Semilog scale leakage current as a function of voltage for samples A–D.

of small forward voltage for these four samples, respectively. It was found that increasing forward bias, slopes of current values with respect to applied voltage are different for different samples. The differential resistance (at 6 mA) of VCSELs with samples A, B, C, and D was 80.06, 75.15, 60.32, and 45.03 Ω, respectively. These phenomena can be explained with the following relation of the current through VCSEL and applied voltage [27]

$$I = I_0\left(\exp\left(\frac{q(V - I \cdot R_s)}{\mathrm{KT}}\right) - 1\right). \tag{2}$$

Here, V is the applied voltage, R_s is the series resistance, I_0 is the reverse saturation current, K is the Boltzmann's constant, T is the operating temperature, and q is the electronic charge. Series resistance R_s is contributed from the bulk and contact resistance of VCSEL, both of which increase with temperature [28]. At high forward bias, series resistance plays a major role in limiting the total current, which is determined from the slope of the $I - V$ curve, shown in Fig. 4(a). Larger R_s thus limits the current at high forward bias according to (2). As was expected, increasing series resistance of the samples at high forward bias resulting from high temperature due to larger thermal resistance for the sample with thick silicon substrate. However, current from the stand-alone VCSEL (sample D) showed the highest value after turn-on, shown in Fig. 4(b), which can also be explained by (2). Reverse saturation current I_0 increased as a strong function of temperature [29], [30]. Hence, there is a competition between an increment in I_0 and a rise in R_s to make an impact on current I. In the case of sample D, operating temperature was so high that I was the highest of all values of forward bias due to the increment in I_0; whereas, in the case of other samples, temperatures were not so high, letting the effect of R_s take over, as discussed above and keeping the current values lower.

TABLE I
OPERATING VOLTAGE (AT 6 mA) OF SAMPLES A–D

Sample	A	B	C	D
Operating voltage (V) @ 6 mA	2.03	2.01	1.94	1.90

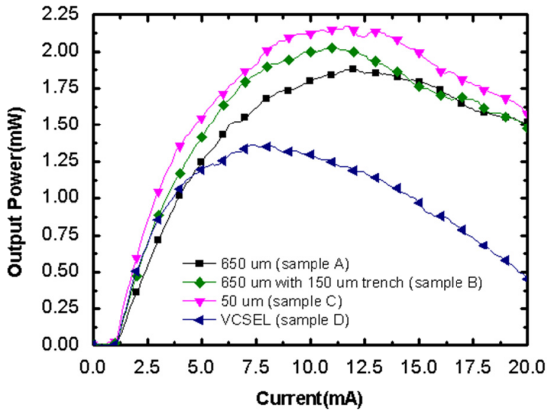

Fig. 5. Output optical power as function of input current for samples A–D.

TABLE II
COMPARISON OF THERMAL RESISTANCE OF SAMPLES A–D

Sample	A	B	C	D
ΔW_{heat} (mW)	34.813	38.106	37.621	33.595
ΔT (K)	47.16	52.6	48.16	68.16
$R_{thermal}$ (K/mW)	1.38	1.35	1.28	2.02

Table I shows the operating voltages under an injection current of 6 mA for all samples. The operation voltage of samples A, B, C, and D was 2.03, 2.01, 1.94, and 1.90 V, respectively. This operating voltage can be written as $V = V_f + V_{Rs}$, where V_f is the forward bias across the VCSEL and $V_{Rs} = I_d.R_s$, is the voltage drop across series resistance R_s. With an increase in operating temperature, V_f decreases due to enhanced intrinsic carrier concentration and less separation between electron and hole Fermi levels. The V_{Rs} increased as R_s increases at a high operating temperature. Hence, the total voltage V increases with an increase in Si thickness due to a high operating temperature. The temperature tendency agreed with the simulation by COMSOL. It is worthy to note that the operating voltage is the lowest for sample D. The higher voltage could be caused by the added resistance of the Si substrate.

Fig. 5 depicts the optical output power as a function of injection current for samples A, B, C, and D. The maximum output power of samples A, B, C, and D was 1.82, 2.01, 2.17, and 1.36 mW, respectively. All the VCSELs presented increasing output power and then decreasing as the current increased. It is worthy to mention that sample D showed the lowest output power (1.36 mW) and early decreasing output power at an applied current of ~7.5 mA. In contrast, the output power was the highest (2.17 mW) for sample C and it saturated up to 12.5 mA. The inputting electrical power when provided to the VCSELs was converted into optical power and heat dissipation, with both the components competing against each other. Joule heating at a high input current was increased and also increased the series resistance. As heat generation increased, it hindered the increase of optical power. With a high input current, generated heat energy was so excessive

that output power started to decline, as was prominent in the case of stand-alone VCSEL. This is also consistent with our earlier findings about samples with a thinner silicon substrate presenting a better heat dissipation ability. To get an idea about heat generation in all of the samples during operation, we measured thermal resistance (R_{Thermal}), which is defined as a change in temperature (ΔT) in the structure per unit heat energy (ΔW_{heat}) that flows through the structure in unit time. Here, $\Delta W_{\text{heat}} = \Delta(I_{\text{input}} \cdot V_{\text{input}} - L_{\text{output}})$. In the above relation, I_{input} and V_{input} are input current and voltage, respectively. L_{output} is the optical output power. For measuring R_{Thermal} input current of 0 and 15 mA are taken into consideration to measure the values of ΔT and ΔW_{heat}, and shown in Table II. As can be expected, R_{Thermal} was the highest for sample D, due to poor thermal conductivity of silver paste. R_{Thermal} decreased after bonding to silicon and copper; thinning of silicon substrate by lapping resulted in the lowest thermal resistance.

IV. Conclusion

The authors have demonstrated the design and fabrication of the heat sinks of an on-chip laser source by bonding III–V VCSEL devices to the silicon substrate and electroplating a copper layer on the backside. As evidenced from the simulation and experiments, although Cu trench structure can improve the thermal dissipation, the thickness of silicon still plays a key role in the effectiveness of heat sinks. As silicon thickness decreased, thermal resistance of the overall structure reduced, thus enhancing heat dissipation from the active region. Improvement in the thermal dissipation of the VCSELs package resulted in the enhancement of optical and electrical response of the VCSELs. Samples with thinner silicon substrate showed less thermal resistance, higher optical output power, less series resistance during operation, lesser variation in wavelength with a change in input current, and higher quality factors. COMSOL simulations have shown an increase in the operating temperature for samples with thicker silicon at a steady state, thus explaining the reason behind our experimental observations. Characteristics of the stand-alone VCSEL demonstrated the highest operating temperature among all the samples due to poor thermal conductance of the silver paste, when it was bonded to the circuit board. We have demonstrated that the heat dissipation of an on-chip laser source can be improved by thinning silicon substrate's thickness, thus proving to be a very promising and cost-effective methodology that could be used toward enhancing the operational efficiency of network on chip (NoC).

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