A high speed and high responsivity photodiode in standard CMOS technology

Wei-Kuo Huang, Yu-Chang Liu and Yue-Ming Hsin

***Abstract*—This work investigates a new Si photodiode (PD) by standard Complementary Metal Oxide Semiconductor (CMOS) process. The basic structure of the proposed Si PD is formed by multiple *p*-*n* diodes with shallow trench isolation (STI) oxide in between *p*- and *n*-region from Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS technology. The proposed PD demonstrates a responsivity of 0.37 A/W at zero bias (λ=823nm). At reverse bias (V_R) of 14.3 V, the fabricated PD exhibits a high responsivity of 0.74 A/W, a -3 dB electrical bandwidth of 1.6 GHz, and an eye diagram at 3.5 Gb/s.**

***Index Terms*—Si, CMOS, Photodiode.**

I. Introduction

For long distance communication, high-speed fiber-optic links have replaced electrical interconnections. Nowadays, photodetectors for long-haul optical communication are mainly implemented in expensive III-V technologies such as GaAs, and InP based devices. But for short distance communication such as board-to-board and chip-to-chip, the cost is crucial and hence the long-haul solutions can not be used. To enable cost-effective implementation of optical short distance interconnect, the standard Silicon (Si) technology compatible photodiode is a good, low-cost approach for general 850-nm vertical cavity surface emitting laser (VCSEL) transmitter. Furthermore, the high-peed CMOS transimpedance amplifier (TIA) and limiting amplifier (LA) are available and can be monolithically integrated with Si photodiode to form an all-Si optical receiver [1].

However, the low absorption coefficient of Si leads to a low quantum efficiency-bandwidth product. This imposes severe limitations on the receiver architecture and performance. A high quantum efficiency-bandwidth product can be achieved by operating photodiode (PD) in the avalanche regime and fabricating PD on silicon-on-insulator (SOI) substrate [2] [3] [4] [5]. The use of SOI substrates can improve the diffusion response and reduce the parasitic capacitance. However, in order to maintain a low cost process and integrate with available 10 Gb/s transimpedance amplifier, limiting amplifier and signal process circuits, it is worth exploring photodetectors fabricated using standard Complementary Metal Oxide Semiconductor (CMOS) process. Table I shows a comparison of published results in standard CMOS PDs on bulk Si substrates. In reference [6], the receiver circuit is complex and designed for compensating the low speed PD. In reference [7] and [8], the differential photodetectors consist of shaded diodes and illuminated diodes. And the cancellation of the partial diffusion photocurrent in the substrate is realized by subtraction of the signal from the illuminated and shaded diodes. The size of the photodetector is large and the resulted responsivity and speed are low.

In this study, we present a high speed and high responsivity photodiode which is implemented in a standard 0.18 μm CMOS technology. The fabricated PD demonstrates a high responsivity of 0.74 A/W and data rate of 3.5 Gb/s, which is well suitable for 2.5 Gb/s optical communication application. This is, to our knowledge, the most fast standard CMOS process PD ever reported except on SOI substrate.

Table I
Comparison of Si PDs using standard CMOS process

Reference	This Work	[6]	[7]	[8]
Process	0.18 μm CMOS Technology	0.18 μm CMOS Technology	0.18 μm CMOS Technology	0.18 μm CMOS Technology
PD Size	50×50 μm^2	50×50 μm^2	80×80 μm^2	100×100 μm^2
PD Bandwidth	**1.6 GHz**	5 MHz	N.A.	1.1 GHz
PD Responsivity	**0.74 A/W**	N.A.	N.A.	0.02 A/W
PD Capacitance	**0.345 pF**	1.6 pF	N.A.	0.416 pF
Wavelength	850 nm	850 nm	850 nm	850 nm
Data Rate	**3.5 Gb/s**	3 Gb/s	500 Mb/s	2 Gb/s

II. Photodetector Design

Figure 1 shows a 3-D schematic structure of the proposed PD. A standard 0.18 μm CMOS process from Taiwan Semiconductor Manufacturing Company (TSMC) is used in this design without process modifications. The *n*-well, *p*-well, shallow trench isolation (STI) oxide, and source/drain implant (*S*/*D* implant) from standard process are used to implement the multiple *p*-*n* diodes in this PD design. The *p*-well and *n*-well are standard processes for forming *n*-MOSFET and *p*-MOSFET in CMOS process. The *S*/*D* implants for *n*-MOSFET and *p*-MOSFET are used for *n*- and *p*-type ohmic contacts, respectively. And the STI oxide is used for forming isolation regions between active devices.

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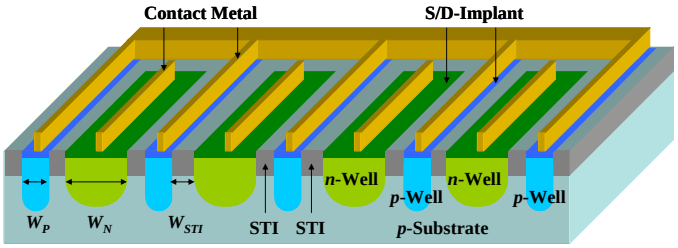


Fig. 1 A 3-D schematic structure of the proposed PD.

The *p*-well together with *p*-substrate and *n*-well form the basic p^+-*p*-*n* avalanche structure. In addition, the standard STI oxide is also implemented in between wells to reduce surface leakage and enhance breakdown characteristics. In this new design, the *p*-well forms deeper and higher *p*-type doping. At suitable reverse bias, the *n*-well and *p*-substrate region are depleted and converted into a wide absorption region. By using STI oxide, it not only improves the breakdown voltage but also extends the depletion region. Therefore, the fully depleted region is wider than published Si PD using *p*-substrate as *p*-region only [6] [7]. Accordingly, it would improve the responsivity.

The total active area of this PD is 50×50 μm^2, which consists of seven *p*-*n* diodes. For each *p*-*n* diode, the width for *p*-well (W_P), *n*-well (W_N), STI oxide (W_{STI}), and contact metal strip is 1.95, 3.45, 0.36 and 0.45 μm, respectively. The distance that the generated carriers drift is determined by the width of each *p*-*n* diode and thus affects the drift time directly. In this design, the width of each well and STI oxide is minimized and limited by design rules.

III. Experimental Results and Discussion

The DC characteristic of fabricated PD is similar to a standard Si *p*-*n* junction diode with turn-on voltage of 0.8 V (at 1 mA) and breakdown voltage of 15 V (at 100μA). Figure 2 shows the measured dark current (I_{DARK}), photocurrent and responsivity for the proposed PD. The photocurrent and responsivity are measured by the 823 nm wavelength laser with optical power of 150 μW. From Fig. 2, a responsivity of 0.37 A/W at zero bias is obtained and attributed to the enlarged absorption region. At V_R of 14.3 V (I_{DARK} < 0.1 μA), a higher responsivity of 0.74 A/W is observed from impact ionization.

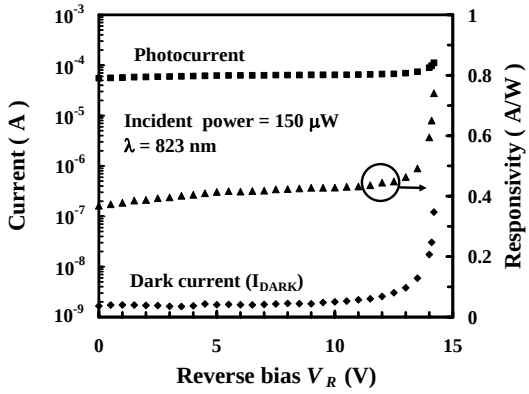


Fig. 2 The measured dark current, photocurrent and responsivity for a 50×50 μm^2 PD. The photocurrent is measured by an 823 nm wavelength laser with optical power of 150 μW.

To investigate the bandwidth of the PD, an 850nm light-wave measurement system is set up. The PD is biased through a bias-tee, which in turn is connected to Agilent E4448A spectrum analyzer. An 850 nm 2.5 Gb/s VCSEL modulated directly by Agilent E8257D signal generator is used as the light source. Then the frequency response of PD at each bias is recorded. Fig. 3 shows the -3 dB electrical bandwidth and extracted PD capacitance (C_{PD}) versus different V_R. The higher bandwidth is obtained while V_R is increased to 10 V, which is due to the higher electric field intensity in moving carriers and the increased depletion depth. Because the depletion width is increased, more carriers would drift in the electric field instead of diffusing. At V_R of 12 V, the bandwidth is increased slightly due to the small change from depletion region. However, at V_R of 14.3 V (avalanche region), large number of carriers is generated. The proportion of carriers in drift to carriers in diffusion is significantly increased and a higher bandwidth is observed. The maximum bandwidth of 1.6 GHz at V_R of 14.3 V is obtained and the normalized frequency response is shown in Fig. 4.

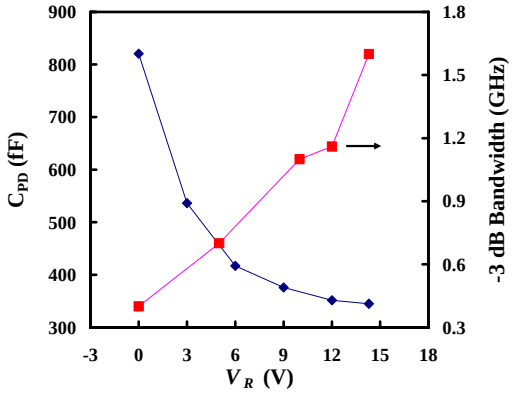


Fig. 3 The -3 dB electrical bandwidth and extracted capacitance (C_{PD}) versus reverse bias (V_R) of the proposed PD.

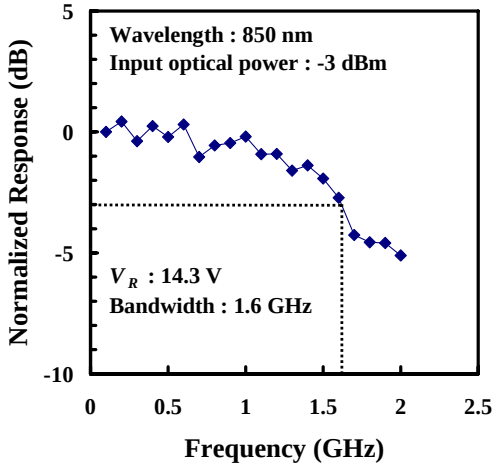
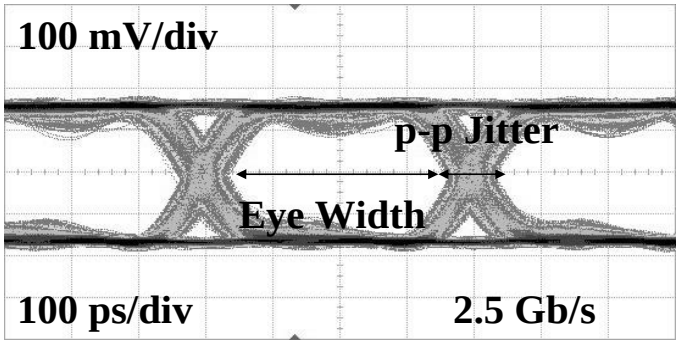


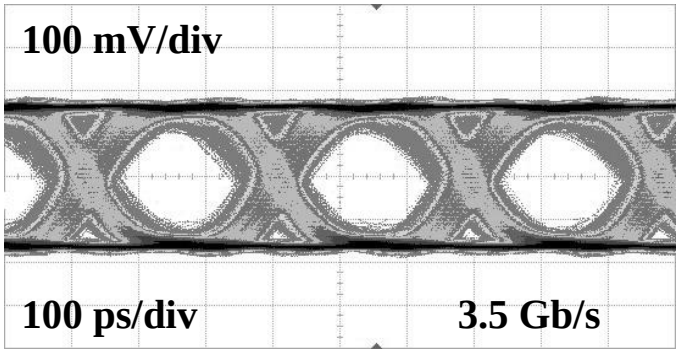
Fig. 4 Normalized frequency response of the proposed PD at V_R of 14.3 V.

In the measurement setup of eye diagram, an 850 nm directly modulated VCSEL is used as the light source. And the output of PD is wire connected to an amplifier with a transimpedance

gain of 48 dBΩ and a -3 dB bandwidth of 2.7 GHz to transform and amplify the output signal. Fig. 5(a) shows the eye diagram at 2.5 Gb/s with incident power of -3 dBm, while PD is biased at V_R of 14.3 V. The eye diagrams at data rate of 3.5 Gb/s is also demonstrated in Fig. 5(b) to illustrate the capability of the proposed PD. Due to the limitation of the instruments, the measured mean values of the peak-to-peak jitter and eye width at data rate of 2.5 Gb/s under different input optical power using Agilent DSO80604B oscilloscope histogram were used indicate the sensitivity.



(a)



(b)

Fig. 5 Measured eye diagrams at data rates of (a) 2.5 Gb/s ,(b) 3.5 Gb/s

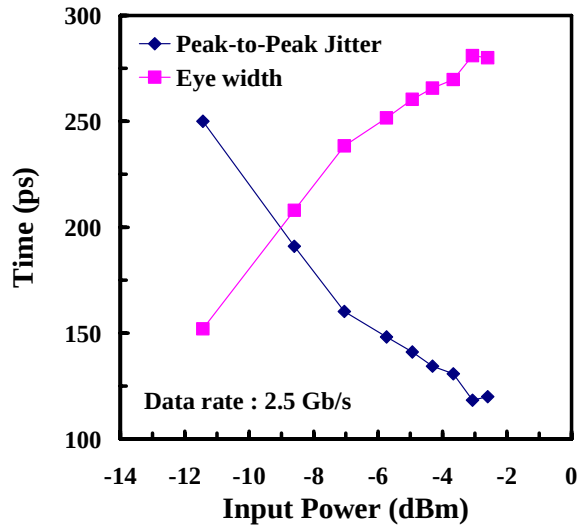


Fig. 6 Measured peak-to-peak jitter and eye width at data rate of 2.5 Gb/s under different input power intensity.

Furthermore, the *RC*-limited -3 dB bandwidth of this device is 5.2 GHz, which is higher than 1.6 GHz from light-wave measurement. Therefore the response time is primarily limited by the carrier transit time in the absorption region. The improvement in PD structure is possible to further decrease the response time to be used in standard CMOS for high-speed 850-nm Optical Communication.

IV. Conclusion

In this study, a new high-speed and high-responsivity PD with multiple *p-n* diodes structure by standard TSMC 0.18 μm CMOS technology is presented. A wider depletion region is achieved by the designed *p*-well together with *p*-substrate and STI oxide constructs. Accordingly; proposed Si PD shows a high responsivity of 0.37 A/W at zero bias. At reverse bias of 14.3 V, PD demonstrates a high responsivity of 0.74 A/W, a -3dB bandwidth of 1.6 GHz, and an eye diagram at 3.5 Gb/s. Additionally, this high gain-bandwidth product PD releases the design issue of the pre-amplifier in receiver circuits.

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